

DATA SHEET

PCK3807A

1:10 LVTTL clock distribution device

Product data sheet
Supersedes data of 2003 Jun 27

2004 Aug 27

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PCK3807A

DESCRIPTION

This low skew clock driver offers 1:10 fan-out. The large fan out from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. The PCK3807A offers low capacitance inputs with hysteresis for improved noise margins. Multiple power and grounds reduce noise. Typical applications are clock and signal distribution.

The PCK3807A operates from a single 2.5 V or 3.3 V supply voltage and over the full industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

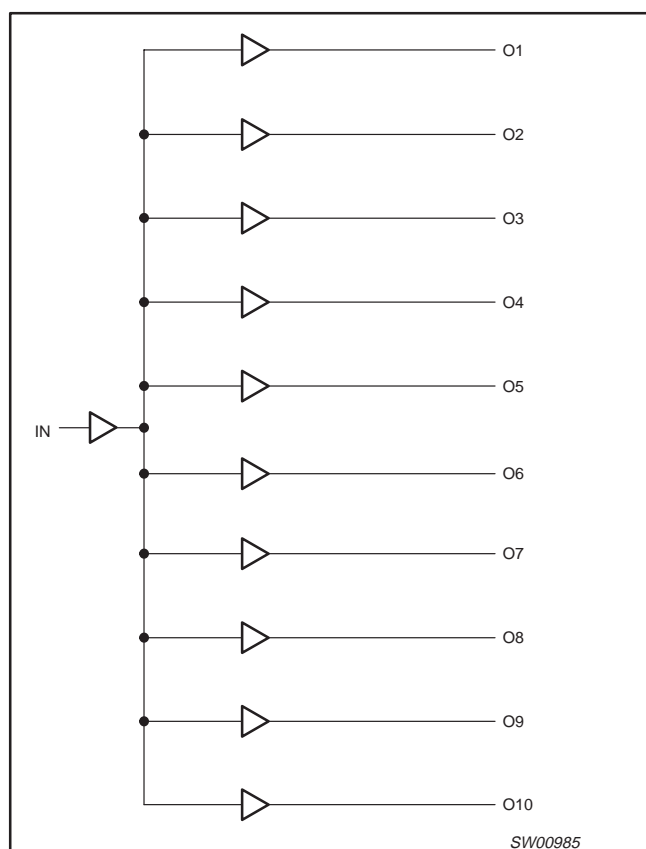
FEATURES

- Low output skew < 120 ps (max)
- Very low duty cycle distortion < 200 ps (max) for $V_{\text{CC}} = 2.5\text{ V}$
- High speed: propagation delay < 3.5 ns (max)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- 1:10 fanout
- Maximum output rise and fall times < 1.5 ns
- Low input capacitance: 2.5 pF typical
- $V_{\text{CC}} = 2.3\text{ V}$ to 3.6 V
- Overvoltage tolerance on inputs
- Available in SSOP, TSSOP, SO and QSOP packages
- >150 MHz operation

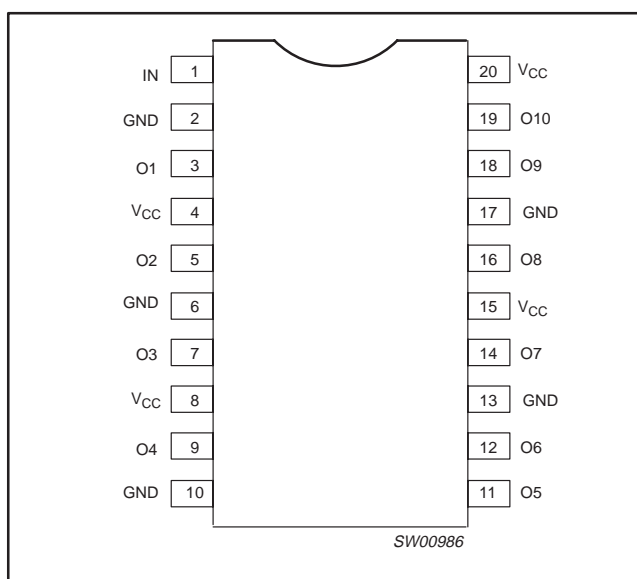
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | DRAWING NUMBER |
|----------------------------|--|------------|----------------|
| 20-Pin Plastic SO | -40°C to $+85^{\circ}\text{C}$ | PCK3807AD | SOT163-1 |
| 20-Pin Plastic SSOP | -40°C to $+85^{\circ}\text{C}$ | PCK3807ADB | SOT339-1 |
| 20-Pin Plastic TSSOP | -40°C to $+85^{\circ}\text{C}$ | PCK3807APW | SOT360-1 |
| 20-Pin Plastic SSOP (QSOP) | -40°C to $+85^{\circ}\text{C}$ | PCK3807ADS | SOT724-1 |

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

| Symbol | Pin | Description |
|-----------------|------------------------------------|----------------|
| IN | 1 | Clock input |
| O1 to O10 | 3, 5, 7, 9, 11, 12, 14, 16, 18, 19 | Clock outputs |
| GND | 2, 10, 13, 17 | Ground |
| V _{CC} | 20 | Supply voltage |

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ABSOLUTE MAXIMUM RATINGS¹

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|---------------------|--------------------------------------|------|-----------------------|------|
| V_{TERM}^2 | Terminal voltage with respect to GND | -0.5 | +4.6 | V |
| V_{TERM}^3 | Terminal voltage with respect to GND | -0.5 | +7 | V |
| V_{TERM}^4 | Terminal voltage with respect to GND | -0.5 | $V_{\text{CC}} + 0.5$ | V |
| T_{stg} | Storage temperature | -65 | +150 | °C |
| I_{O} | DC output current | -60 | +60 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminal.
- Outputs terminals.

CAPACITANCE

 $T_{\text{amb}} = +25\text{ °C}$, $f = 1.0\text{ MHz}$

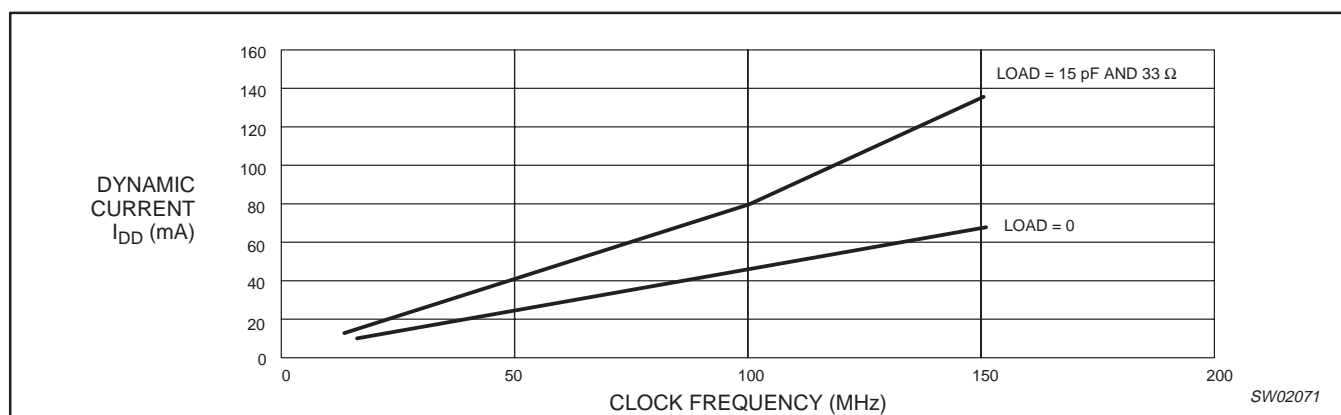
| SYMBOL | PARAMETER | CONDITIONS | TYP | MAX | UNIT |
|--------|--------------------|-------------------------------|-----|-----|------|
| C_i | Input capacitance | $V_{\text{IN}} = 0\text{ V}$ | 2.5 | 4 | pF |
| C_o | Output capacitance | $V_{\text{OUT}} = 0\text{ V}$ | 5.5 | 6 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|------------------|--------------------------------------|--------|-----|------|
| | | MIN | MAX | |
| V_{CC} | DC supply voltage | 2.3 | 3.6 | V |
| f_{IN} | Input signal frequency | 0 | 150 | MHz |
| T_{amb} | Operating free-air temperature range | -40 | +85 | °C |
| C_L | Output capacitance load | — | 50 | pF |

Figure 1. Dynamic current vs. clock frequency, $V_{\text{CC}} = 3.3\text{ V}$

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POWER SUPPLY CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|--|--|---|-----|------|------|---------------|
| ΔI_{CC} | Quiescent power supply current, TTL inputs HIGH | $V_{CC} = \max$; $V_{IN} = V_{CC} - 0.6 \text{ V}$ | | – | 3 | 30 | μA |
| I_{CCD} | Dynamic power supply current | $V_{CC} = 2.7 \text{ V}$ Input toggling 50% duty cycle $V_{IN} = V_{CC}$ or GND | Outputs open | – | 0.31 | 0.45 | mA/MHz |
| | | | 15 pF and 33 Ω load | – | 1.0 | – | |
| | | $V_{CC} = 3.6 \text{ V}$ | Outputs open | – | 0.5 | 0.75 | |
| | | | 15 pF and 33 Ω load | – | 1.5 | – | |
| I_C | Total power supply current Dynamic power supply current | $V_{CC} = 2.7 \text{ V}$ Input toggling 50% duty cycle Outputs open | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ $f_i = 50 \text{ MHz}$ | – | 15.5 | 22.8 | mA |
| | | | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ $f_i = 150 \text{ MHz}$ | – | 50 | 75 | |
| | | $V_{CC} = 3.6 \text{ V}$ | $f_i = 50 \text{ MHz}$ | – | 25 | 37 | |
| | | | $f_i = 150 \text{ MHz}$ | – | 75 | 115 | |

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3 \text{ V}$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = V_{CC} - 0.6 \text{ V}$).
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_i)$
 I_{CC} = Quiescent Current (I_{CCL} , I_{CCH} and I_{CCZ})
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.6 \text{ V}$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_i = Input Frequency
All currents are in milliamps and all frequencies are in MHz

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGET_{amb} = -40 °C to +85 °C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise specified

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | MIN | TYP | MAX | UNIT |
|--------------------------------------|---------------------------------------|---|-----------------------|------|------|------|
| V _{IH} | HIGH-level input voltage (Input pins) | V _{CC} = 3.0 V to 3.6 V | 2 | – | 5.5 | V |
| | HIGH-level input voltage (I/O pins) | V _{CC} = 2.3 V to 2.7 V | 1.7 | – | 3.6 | |
| V _{IL} | LOW-level input voltage (Input pins) | V _{CC} = 3.0 V to 3.6 V | –0.5 | – | 0.8 | V |
| | LOW-level input voltage (I/O pins) | V _{CC} = 2.3 V to 2.7 V | –0.5 | – | 0.7 | |
| I _{IH} | HIGH-level input current (Input pins) | V _{CC} = Max V _I = 5.5 V | – | – | ± 1 | µA |
| | HIGH-level input current (I/O pins) | | – | – | ± 1 | |
| I _{IL} | LOW-level input current (Input pins) | V _{CC} = Max V _I = GND | – | – | ± 1 | µA |
| | LOW-level input current (I/O pins) | | – | – | ± 1 | |
| V _{IK} | Clamp diode voltage | V _{CC} = Min; I _{IN} = –18 mA | – | –0.7 | –1.0 | V |
| I _{ODH} | HIGH-level input current | V _{CC} = 3.3 V; V _{IN} = V _{IH} or V _{IL} ; V _O = 1.5 V ³ | –36 | –120 | –150 | mA |
| I _{ODL} | LOW-level input current | V _{CC} = 3.3 V; V _{IN} = V _{IH} or V _{IL} ; V _O = 1.5 V ³ | 50 | 150 | 200 | mA |
| V _{OH} | HIGH-level output voltage | V _{CC} = 2.3 V to 3.6 V I _{OH} = –0.1 mA | V _{CC} – 0.2 | – | – | V |
| | | V _{CC} = 2.3 V I _{OH} = –8 mA | 1.9 | – | – | |
| | | V _{CC} = 3.0 V I _{OH} = –8 mA | 2.4 ⁶ | 3 | – | |
| V _{OL} | LOW-level output voltage | V _{CC} = 2.3 V to 3.6 V I _{OL} = 0.1 mA | – | – | 0.2 | V |
| | | V _{CC} = 2.3 V I _{OL} = 8 mA | – | – | 0.3 | |
| | | V _{CC} = 3.0 V I _{OL} = 16 mA | – | 0.2 | 0.4 | |
| | | V _{CC} = 3.0 V I _{OL} = 24 mA | – | 0.3 | 0.5 | |
| I _{OFF} | Input power off leakage | V _{CC} = 0 V; V _{IN} = 4.5 V | – | – | ± 1 | µA |
| I _{OS} | Short circuit current ⁵ | V _{CC} = Max; V _O = GND ⁴ | 0 | –155 | –240 | mA |
| V _{hys} | Input hysteresis | – | – | 150 | – | mV |
| I _{CCL} I _{CCH} | Quiescent power supply current | V _{CC} = Max V _{IN} = GND or V _{CC} | – | 0.1 | 10 | µA |

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3 V, +25 °C ambient.
- Duration of the test should not exceed one second.
- Not more than one output shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} – 0.6 V at rated current.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE – INDUSTRIAL^{3,4}T_{amb} = –40 °C to +85 °C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS ¹ | 2.5 V ± 0.2 V | | 3.3 V ± 0.3 V | | UNIT |
|--------------------------------------|--|--|------------------|------|------------------|------|------|
| | | | MIN ² | MAX | MIN ² | MAX | |
| t _{PLH} t _{PHL} | Propagation delay | 50 Ω to V _{CC} /2; C _L = 10 pF (See Figure 2) | 1.5 | 2.7 | 1.3 | 2.5 | ns |
| t _R | Output rise time | or | – | 1.0 | – | 1.0 | ns |
| t _F | Output fall time | | – | 1.0 | – | 1.0 | ns |
| t _{SK(o)} | Output skew: skew between outputs of same package (same transition) | 50 Ω AC termination; C _L = 10 pF (See Figure 3); | – | 0.12 | – | 0.12 | ns |
| t _{SK(p)} | Pulse skew: skew between opposite transitions of same output (t _{PHL} –t _{PLH}) | f ≤ 150 MHz; Outputs connected in groups of two | – | 0.3 | – | 0.45 | ns |
| t _{SK(t)} | Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade | | – | 0.6 | – | 0.6 | ns |
| t _{PLH} t _{PHL} | Propagation delay | 50 Ω to V _{CC} /2; C _L = 22 pF (See Figure 2) | 1.5 | 3.5 | 1.5 | 3 | ns |
| t _R | Output rise time | or | – | 1.0 | – | 1.0 | ns |
| t _F | Output fall time | | – | 1.0 | – | 1.0 | ns |
| t _{SK(o)} | Output skew: skew between outputs of same package (same transition) | 50 Ω AC termination; C _L = 22 pF (See Figure 3); | – | 0.12 | – | 0.12 | ns |
| t _{SK(p)} | Pulse skew: skew between opposite transitions of same output (t _{PHL} –t _{PLH}) | f ≤ 150 MHz; Outputs connected in groups of two | – | 0.3 | – | 0.45 | ns |
| t _{SK(t)} | Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade | | – | 0.6 | – | 0.6 | ns |
| t _{PLH} t _{PHL} | Propagation delay | C _L = 30 pF; f ≤ 67 MHz (See Figure 4) | 1.5 | 4.0 | 1.5 | 4 | ns |
| t _R | Output rise time | | – | 1.0 | – | 1.0 | ns |
| t _F | Output fall time | | – | 1.0 | – | 1.0 | ns |
| t _{SK(o)} | Output skew: skew between outputs of same package (same transition) | | – | 0.35 | – | 0.35 | ns |
| t _{SK(p)} | Pulse skew: skew between opposite transitions of same output (t _{PHL} –t _{PLH}) | | – | 0.35 | – | 0.35 | ns |
| t _{SK(t)} | Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade | | – | 1.0 | – | 0.75 | ns |
| t _{jitter} | RMS jitter | | – | 1.0 | – | 1.0 | ps |
| f _{MAX} | Maximum output frequency | Functional to 400 MHz | – | 400 | – | 400 | MHz |
| t _{PLH} t _{PHL} | Propagation delay | C _L = 50 pF; f ≤ 40 MHz (See Figure 5) | 1.5 | 4.5 | 1.5 | 4.0 | ns |
| t _R | Output rise time | | – | 1.5 | – | 1.5 | ns |
| t _F | Output fall time | | – | 1.5 | – | 1.5 | ns |
| t _{SK(o)} | Output skew: skew between outputs of same package (same transition) | | – | 0.35 | – | 0.35 | ns |
| t _{SK(p)} | Pulse skew: skew between opposite transitions of same output (t _{PHL} –t _{PLH}) | | – | 0.75 | – | 0.75 | ns |
| t _{SK(t)} | Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade | | – | 1 | – | 0.75 | ns |

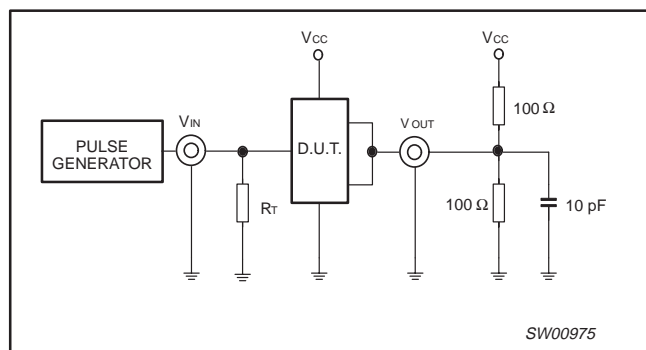
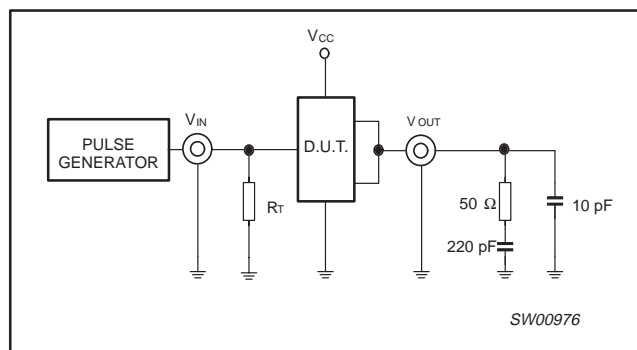
NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- t_{PLH}, t_{PHL}, t_{SK(t)} are production tested. All other parameters guaranteed but not production tested.
- Propagation delay range indicated by Min and Max limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

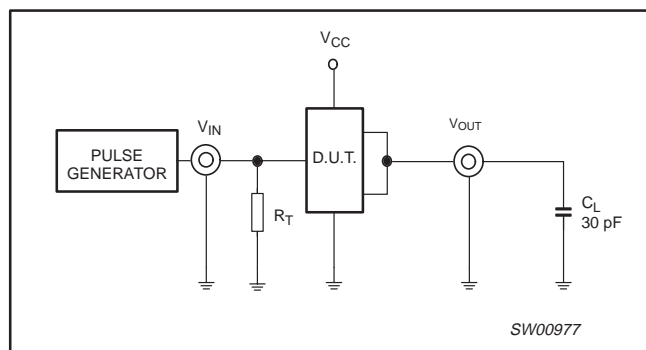
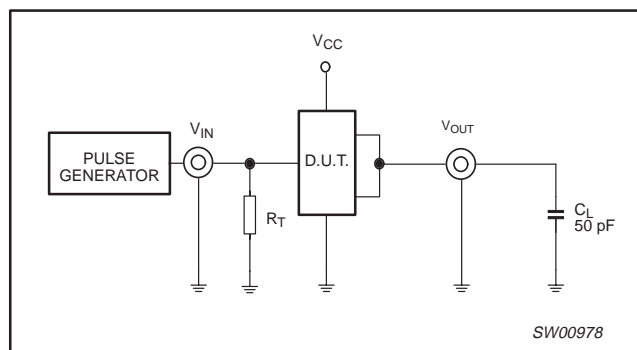
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TEST CIRCUITS

Figure 2. $Z_O = 50\ \Omega$ TO $V_{CC}/2$, $C_L = 10\ \text{pF}$ 

The capacitor value for ac termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

Figure 3. $Z_O = 50\ \Omega$ AC termination, $C_L = 10\ \text{pF}$ Figure 4. $C_L = 30\ \text{pF}$ circuitFigure 5. $C_L = 50\ \text{pF}$ circuit

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TIMING DIAGRAMS

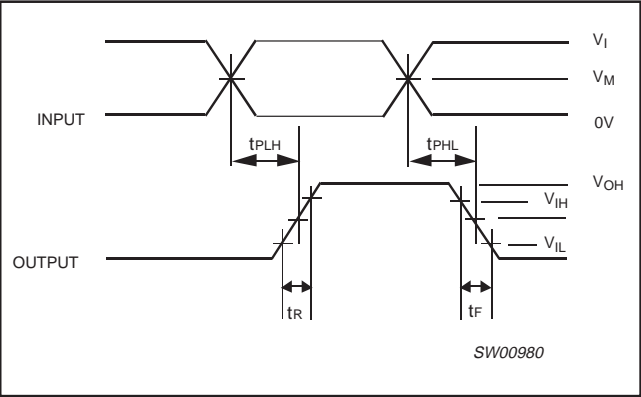


Figure 6. Package delay (see Table 1)

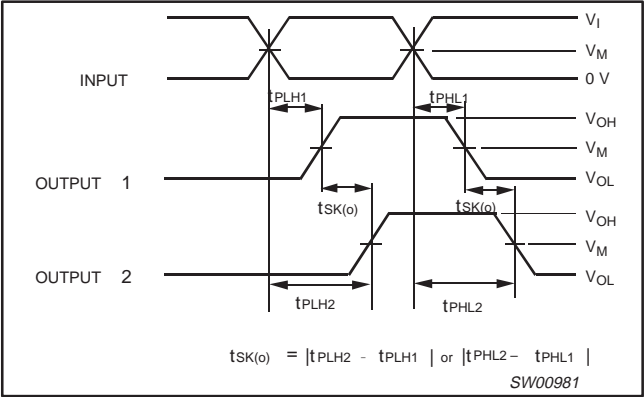


Figure 7. Output skew – $t_{SK(O)}$ (see Table 1)

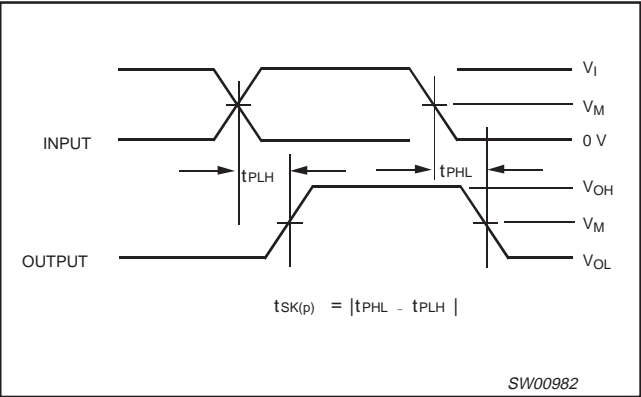


Figure 8. Pulse skew – $t_{SK(p)}$ (see Table 1)

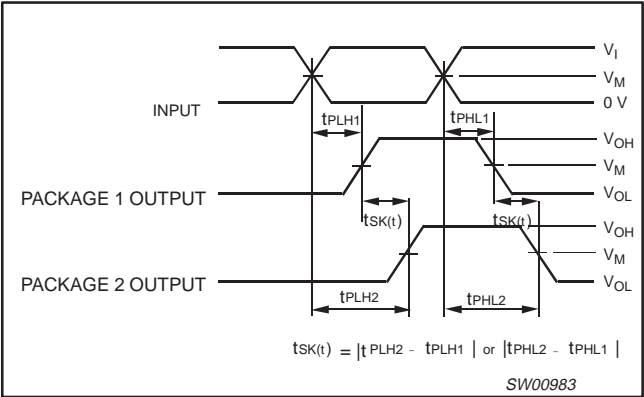


Figure 9. Package skew – $t_{SK(y)}$ (see Table 1)

Table 1. Reference levels

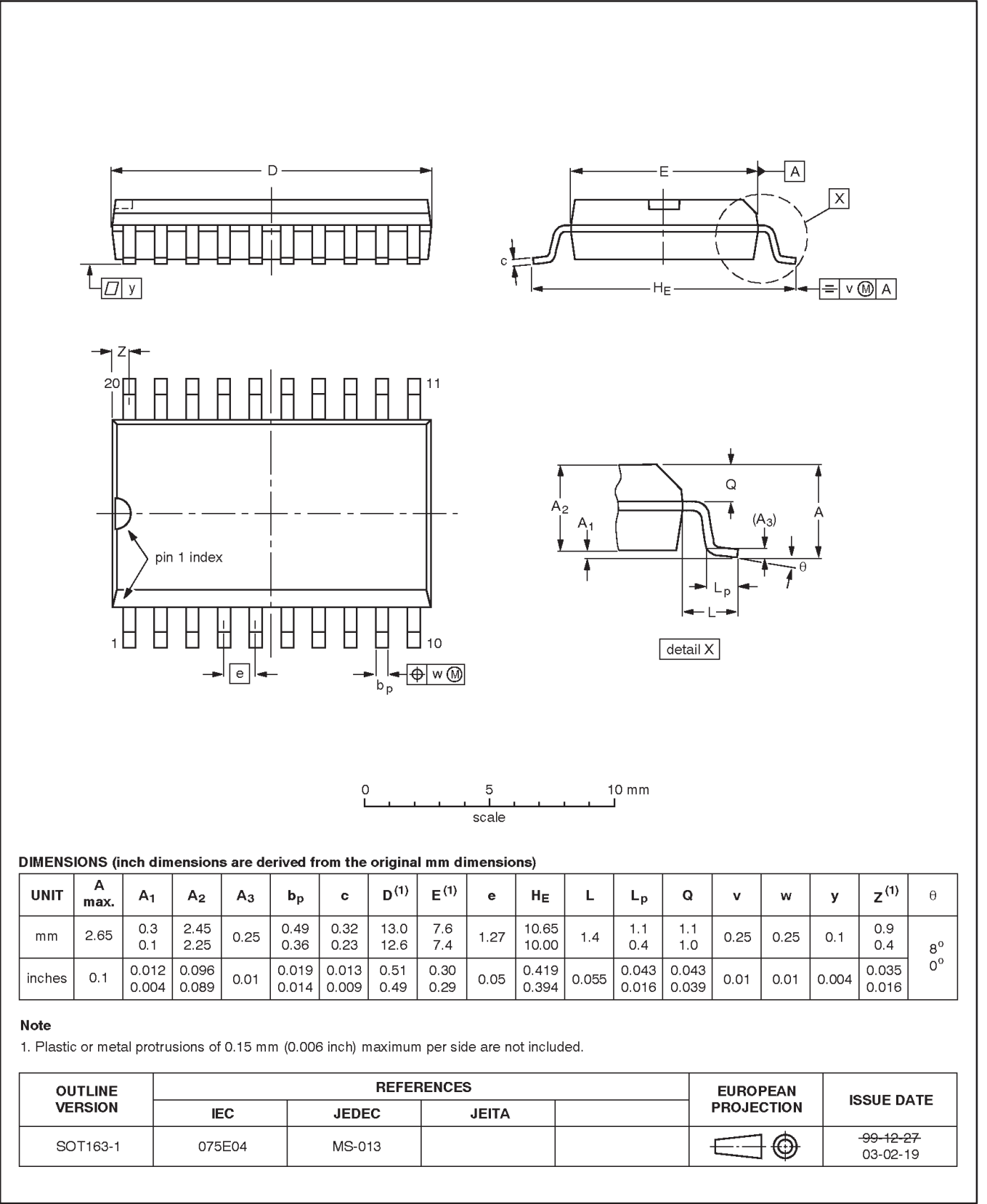
| Reference level | V_I | V_M |
|------------------------------|----------|------------|
| For $V_{CC} = 3.3 \pm 0.3$ V | 3.0 V | 1.5 V |
| For $V_{CC} = 2.5 \pm 0.2$ V | V_{CC} | $V_{CC}/2$ |

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

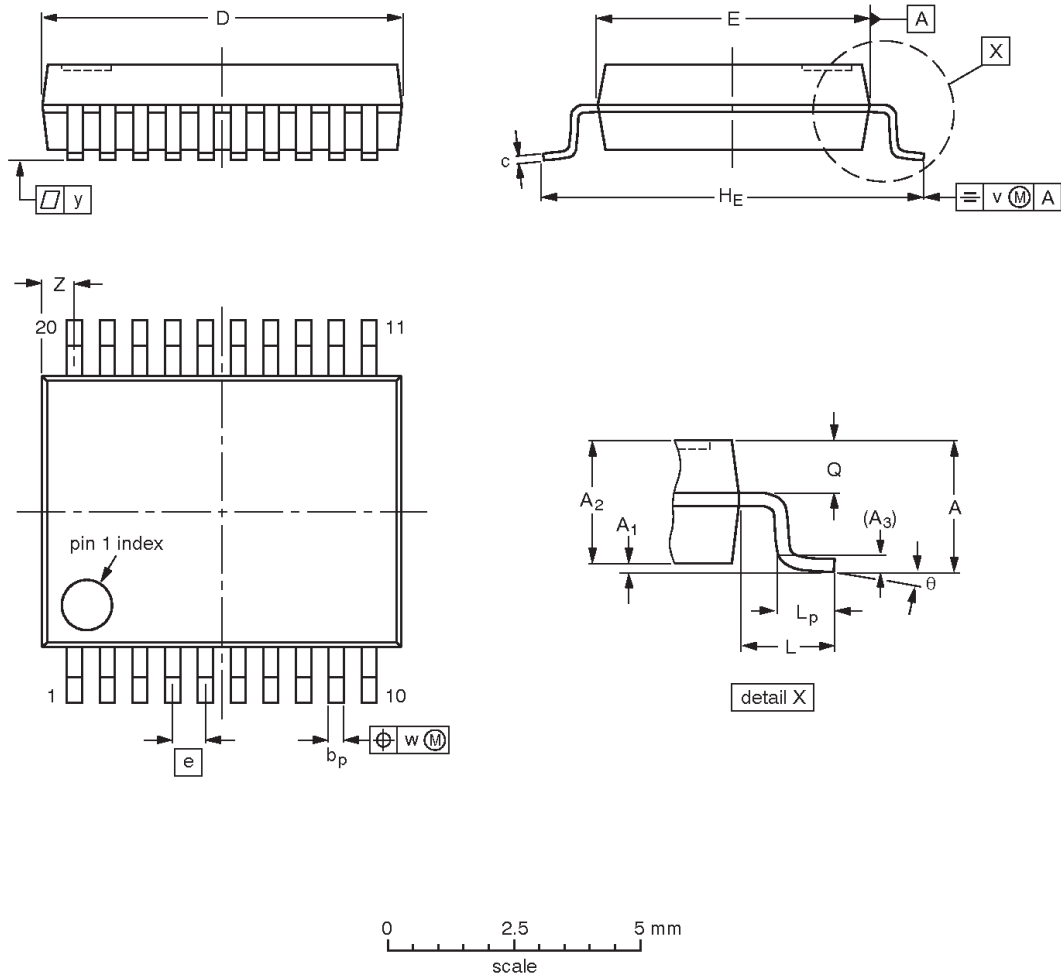


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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | HE | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|-----------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 7.4 7.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 0.9 0.5 | 8° 0° |

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

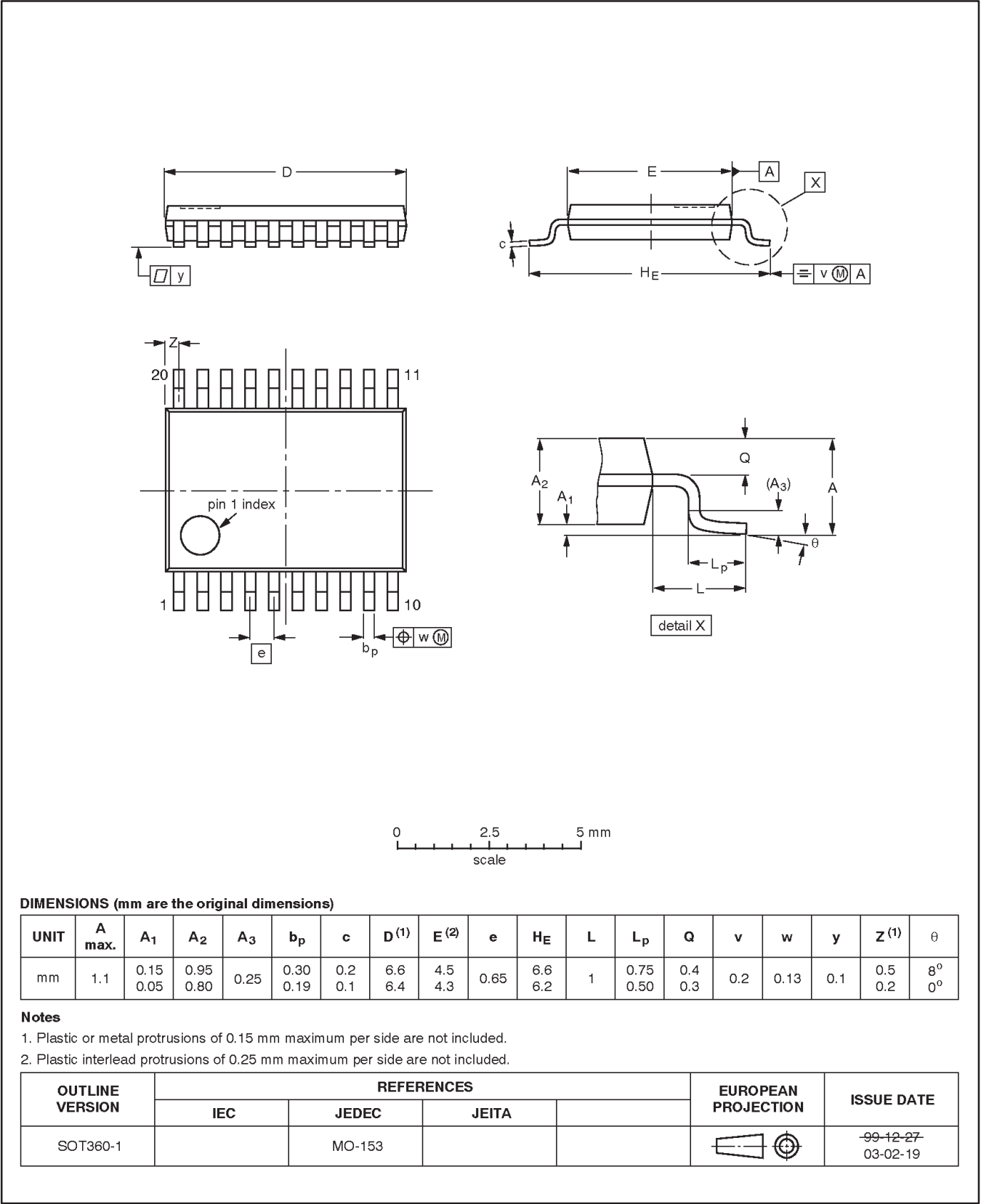
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|------------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT339-1 | | MO-150 | | | | 99-12-27 03-02-19 |

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

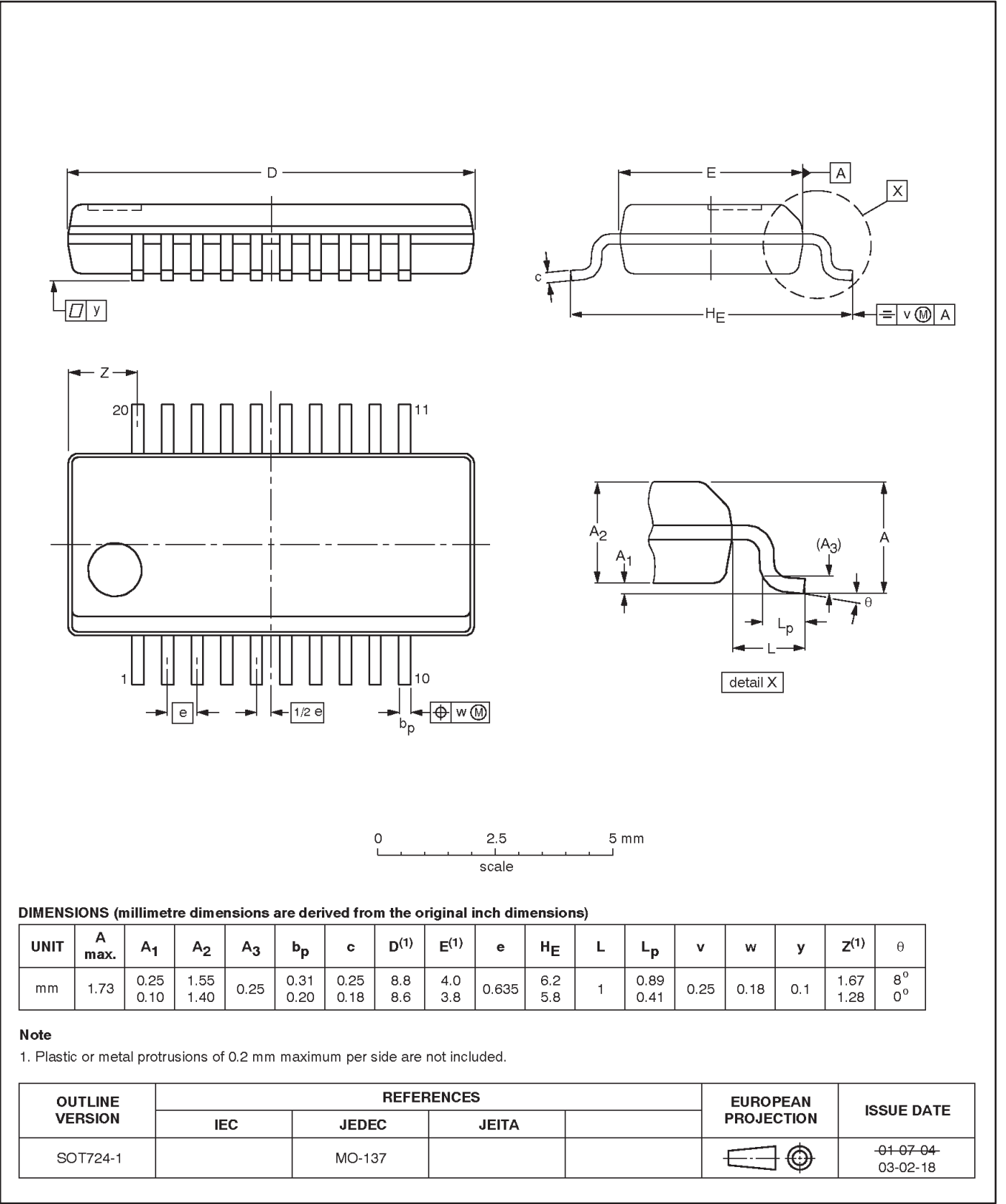


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SSOP20: plastic shrink small outline package; 20 leads;
body width 3.9 mm; lead pitch 0.635 mm

SOT724-1



1:10 LVTTTL clock distribution device

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REVISION HISTORY

| Rev | Date | Description |
|-----|----------|--|
| _2 | 20040827 | Product data sheet (9397 750 14007). Supersedes data of 2003 Jun 27 (9397 750 11683). Modifications: <ul style="list-style-type: none"> Recommended Operating Conditions table on page 3: change V_{CC} Min. limit from 2.5 V to 2.3 V. |
| _1 | 20030627 | Product data (9397 750 11683); ECN 853-2431 30019 dated 18 June 2003. Initial version |

Data sheet status

| Level | Data sheet status ^[1] | Product status ^{[2] [3]} | Definitions |
|-------|----------------------------------|-----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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