Micro Linear

ML4621, ML4622

Data Quantizer

GENERAL DESCRIPTION

The ML4621 and ML4622 Data Quantizers are low noise, wideband, bipolar monolithic ICs designed specifically for signal recovery applications in fiberoptic receiver systems. They contain a two stage wideband limiting amplifier which is capable of accepting an input signal as low as 2mV with a 55dB dynamic range. This high level of sensitivity is achieved by using a DC restoration feedback loop which nulls any offset voltage produced in the limiting amplifier.

The output stage is a high speed comparator circuit with both TTL and ECL outputs. An enable pin is included for added control.

The Minimum Signal Discriminator circuit provides a Link Monitor function with a user selectable reference voltage. This circuit monitors the peaks of the input signal and provides a logic level output indicating when the input falls below an acceptable level. This output can be used to disable the Quantizer and/or drive an LED, providing a visible link status.

The ML4621 is the most flexible Quantizer because of the additional nodes made available and a slightly higher bandwidth. The ML4622 is a reduced pin count version of the ML4621 with a slighly lower bandwidth and burst mode receive ability.

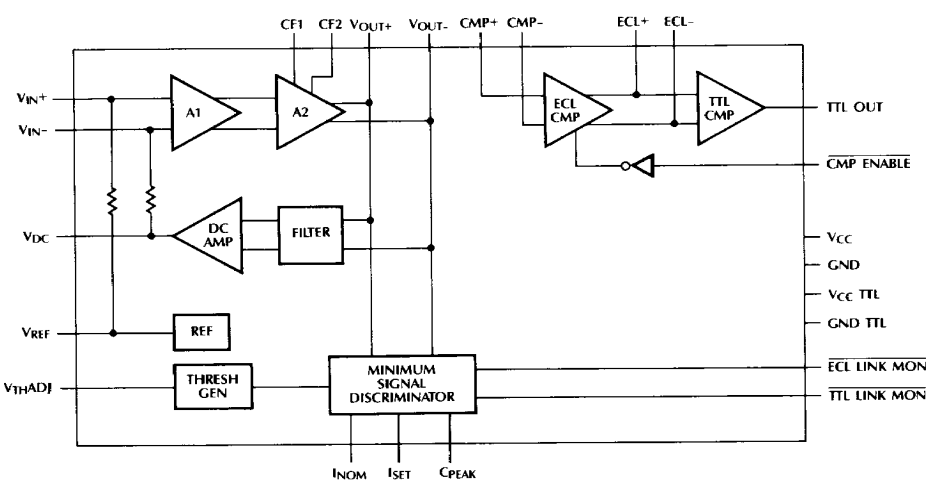
FEATURES

- 50MHz minimum bandwidth (ML4621) for data rates of up to 100MBd
- 40MHz minimum bandwidth (ML4622) for data rates up to 80MBd
- Can be powered by either +5V providing TTL level outputs or -5.2V providing ECL levels
- Low noise design:
  25μV RMS over 50MHz noise bandwidth
- Adjustable Link Monitor function
- Wide 55dB input dynamic range
- 10ns minimum input pulse
- Low power design
- Available in 16-pin SOIC (Narrow) or DIP (ML4622), 24-pin Skinny DIP (ML4621) and 28-pin PLCC (ML4621)

APPLICATIONS

- IEEE 802.3 FOIRL Receiver
- IEEE 802.5 4 and 16 Mbps Fiber Optic Token Ring
- IEEE 802.4 Fiber Optic Token Bus
- Fiber Optic Data Communications and Telecommunications Receivers

ML4621 BLOCK DIAGRAM



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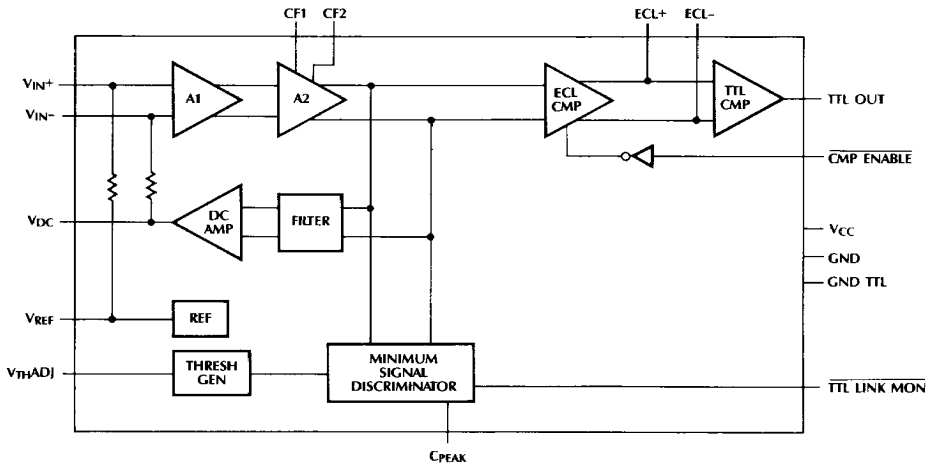
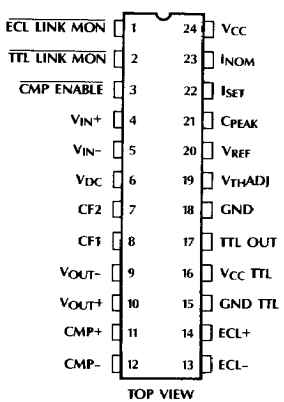
ML4622 BLOCK DIAGRAM

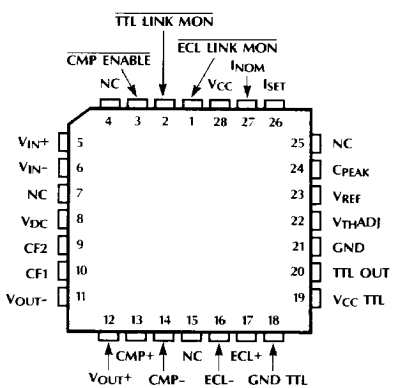


PIN CONNECTIONS

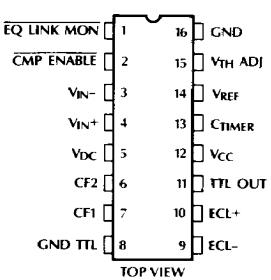
ML4621
24-Pin Skinny DIP



ML4621
28-Pin PCC



ML4622
16-Pin DIP or SOIC (Narrow)



PIN DESCRIPTION

NAME	FUNCTION
$\overline{\text{ECL LINK MON}}$	ECL Link Monitor output. Signal is low when the V_{IN}+, V_{IN}– inputs exceed the minimum threshold, which is set by a voltage on the V_{TH}ADJ pin. Signal is high when the input signal level is below the threshold.
$\overline{\text{TTL LINK MON}}$	TTL Link Monitor output. Same logic function as ECL LINK MON. Capable of driving a 10mA LED indicator. This pin normally tied to CMP ENABLE.
$\overline{\text{CMP ENABLE}}$	A low voltage at this TTL input pin enables both the ECL and the TTL outputs. A high TTL voltage disables the comparator output with ECL+ high, ECL– low, and TTL OUT high.
V_{IN}–	This input pin should be capacitively coupled to the input source or to ground. (The input resistance is approximately 8kΩ.)
V_{IN}+	This input pin should be capacitively coupled to the input source or to ground. (The input resistance is approximately 8kΩ.)
CMP–	This comparator input pin is an open base configuration which relies on the DC bias of the amplifier output to establish the proper DC operating voltage. This voltage should be reestablished if filtering is implemented between V_{OUT}– and CMP–.
ECL–	The ECL comparator negative output.
ECL+	The ECL comparator positive output.
GND TTL	The negative supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
V_{CC} TTL	The positive supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
TTL OUT	TTL data output. (Totem pole type output stage.)

NAME	FUNCTION
V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
CF2	A capacitor from this pin to ground controls the maximum bandwidth of the amplifier to accommodate lower operating frequencies.
CF1	The capacitor on this pin should match the one on CF2.
V_{OUT}–	The negative output of the amplifier, which is normally tied to CMP–.
V_{OUT}+	The positive output of the amplifier, which is normally tied to CMP+.
CMP+	This comparator input pin is an open base configuration which relies on the DC bias of the amplifier output to establish the proper DC operating voltage. This voltage should be reestablished if filtering is implemented between V_{OUT}+ and CMP+.
GND	Negative supply. Connect to –5.2V for ECL operation, or to ground for TTL operation.
V_{TH}ADJ	This input pin sets the minimum amplitude of the input signal required to cause the link monitors to go low.
V_{REF}	A 2.5V reference with respect to GND.
C_{PEAK}	A capacitor from this pin to ground determines the Link Monitor response time.
I_{SET}	Current into an internal diode connected between this pin and GND is turned around and pulled from C_{PEAK}. This pin is normally connected to I_{NOM}.
I_{NOM}	Sets a current of approx. 125μA when connected to I_{SET}.
V_{CC}	Positive supply. Connect to ground for ECL operation, or to 5V for TTL operation.

ABSOLUTE MAXIMUM RATINGS

V_{CC} - GND ..... –0.3 to +7.0
V_{CC} TTL - GND TTL ..... –0.3 to +7.0
Inputs/Output GND ..... –0.3 to V_{CC} +0.3
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 sec.) ..... +260°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ML4621 ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{CC1}	V_{CC} Supply Current		65	100	mA	V_{CC} TTL = GND TTL = V_{CC}
I_{CC2}	V_{CC} Supply Current (TTL Out Enabled)		70	110	mA	V_{CC} TTL = V_{CC} GND TTL = GND
$I_{V_{REF}}$	V_{REF} Output Current	-5.0		0.5	mA	
V_{REF}	Reference Voltage	2.45	2.55	2.65	V	
A_V	Amplifier Gain A1 A2		75		V/V	V_{IN} = 5mV
V_{IN}	Input Signal Range	2		1400	mV_{P-P}	
V_{TH}ADJ Range	External Voltage at V_{TH}ADJ to set V_{TH}	1		2.5	V	
V_{OS}	Input Offset		3		mV	V_{DC} = V_{REF} (DC loop inactive)
E_N	Input Referred Noise		25		μV	50MHz BW
BW	3dB Bandwidth	50	65		MHz	
V_{IN} PW	Min Input Pulsewidth		10		ns	
R_{IN}	Input Resistance		8		kΩ	V_{IN}+, V_{IN}–
t_{PD} AMP	Amplifier Propagation Delay	4		8	ns	From V_{IN}+, V_{IN}– to V_{OUT}+, V_{OUT}– V_{IN} = $10mV_{P-P}$
t_{PD} ECL	ECL Comparator Propagation Delay	4		8	ns	From CMP+, CMP– to ECL+, ECL– V_{IN} = $10mV_{P-P}$
t_{PD} TTL	TTL Comparator Propagation Delay	4		8	ns	From ECL+, ECL– to TTL OUT V_{IN} = $10mV_{P-P}$
$R_{V_{TH}ADJ}$	Input Resistance of V_{TH}ADJ		6.8		kΩ	
$I_{V_{OUT}}$	Output Current of V_{OUT}+ and V_{OUT}–			3	mA	
I_{CMP}	Leakage Current of CMP+ and CMP–		25		μA	
VCM_{CMP}	Common Mode Range of CMP+ and CMP–	GND + 2.0		V_{CC} – 1.0	V	
ECL V_{OH}	Output High Voltage at ECL+, ECL–	3.94		4.30	V	With 200Ω load tied to V_{CC} – 2V T_A = 25°C
ECL V_{OL}	Output Low Voltage at ECL+, ECL–	3.11		3.38	V	With 200Ω load tied to V_{CC} – 2V T_A = 25°C
A_V ECL	ECL CMP Gain		100		V/V	
TTL V_{OH}		2.4			V	V_{CC} TTL = 5V, I_{OH} = –50μA
TTL V_{OL}				0.4	V	V_{CC} TTL = 5V, I_{OL} = 2mA
TTL V_{IH}		2.0			V	
TTL V_{IL}				0.8	V	
TTL I_{IH}		-50		50	μA	V_{IH} = 2.4V
TTL I_{IL}		-1.6		0	mA	V_{IH} = 0.4V
I_{NOM}			125		μA	I_{NOM} = I_{SET}

ML4622 ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{CC1}	V_{CC} Supply Current (TTL Output Disabled)		25	40	mA	GND TTL = V_{CC}
I_{CC2}	V_{CC} Supply Current (TTL Output Enabled)		45	65	mA	GND TTL = GND
V_{REF}	Reference Voltage	2.45	2.55	2.65	V	
$I_{V_{REF}}$	V_{REF} Output Current	–5.0		0.5	mA	
A_V	Amplifier Gain A1 A2		75		V/V	V_{IN} = 5mV
V_{IN}	Input Signal Range	2		1400	mV_{P-P}	
V_{TH}ADJ Range	External Voltage at V_{TH}ADJ to set V_{TH}	0		2.5	V	
V_{OS}	Input Offset		3		mV	V_{DC} = V_{REF} (DC loop inactive)
E_N	Input Referred Noise		25		μV	50MHz BW
BW	3dB Bandwidth	40	55		MHz	
V_{IN} PW	Min Input Pulsewidth		10		ns	
R_{IN}	Input Resistance		5		kΩ	V_{IN}+, V_{IN}–
$I_{V_{TH}ADJ}$	Input Bias Current of V_{TH}ADJ	–40		40	μA	
t_{PDTTL}	Propagation Delay	12		24	ns	From V_{IN}+, V_{IN}– to TTL Out V_{IN} = $10mV_{P-P}$
t_{PDECL}	Propagation Delay	8		16	ns	From V_{IN}+, V_{IN}– to ECL+, ECL– V_{IN} = $10mV_{P-P}$
TTL V_{OH}		2.4			V	V_{CC} TTL = 5V, I_{OH} = –50μA
TTL V_{OL}				0.5	V	V_{CC} TTL = 5V, I_{OL} = 2mA
TTL V_{IH}		2.0			V	
TTL V_{IL}				0.8	V	
TTL I_{IH}		–50		50	μA	V_{IH} = 2.4V
TTL I_{IL}		–1.6		0	mA	V_{IH} = 0.4V

FUNCTIONAL DESCRIPTION

AMPLIFIER

The Quantizers have a two stage limiting amplifier with an input common mode range of (GND + 1.8V) to (V_{CC} - 1.5V). Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.9V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with a 3dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi\ 8000\ C} \text{ (ML4621)} \quad (1)$$

$$f_L = \frac{1}{2\pi\ 5000\ C} \text{ (ML4622)}$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to V_{CC} as shown in figure 1. The high corner frequency can also be adjusted by attaching capacitors to CF1 and CF2. The equation for adjusting this corner is

$$f_H = \frac{1}{2\pi\ 425\ C} \quad (2)$$

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in figure 2. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. An external capacitor at V_{DC} is used to store the offset voltage. Although the value of this capacitor is non-critical, the pole it creates can effect the stability of the feedback loop. To avoid stability problems using the ML4621, the

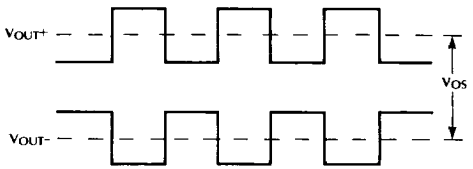


Figure 2.

value of this capacitor should be at least 100 times smaller than the input coupling capacitors. On the ML4622 the input coupling capacitors should be 100 times smaller than the V_{DC} capacitor.

On the ML4621, the output of the amplifier is isolated from the comparator and made available to the user. This allows the user to add circuitry between the amplifier and the comparator for wave shaping and other signal conditioning as desired.

COMPARATOR

Two types of comparators are employed in the output section of these Quantizers. The high speed ECL comparator is used to provide the ECL level outputs and in turn drives the TTL comparator. The enable pin, CMP ENABLE, is provided to control the ECL comparator. When CMP ENABLE is low the comparators function normally. When it's high, it forces ECL+ high, ECL- low, and TTL OUT high. On the ML4622 when CMP ENABLE is high, it forces ECL+ low, ECL- high, and TTL OUT low. The CMP ENABLE pin can be controlled with TTL level signals when the Quantizer is powered by 5V and ground.

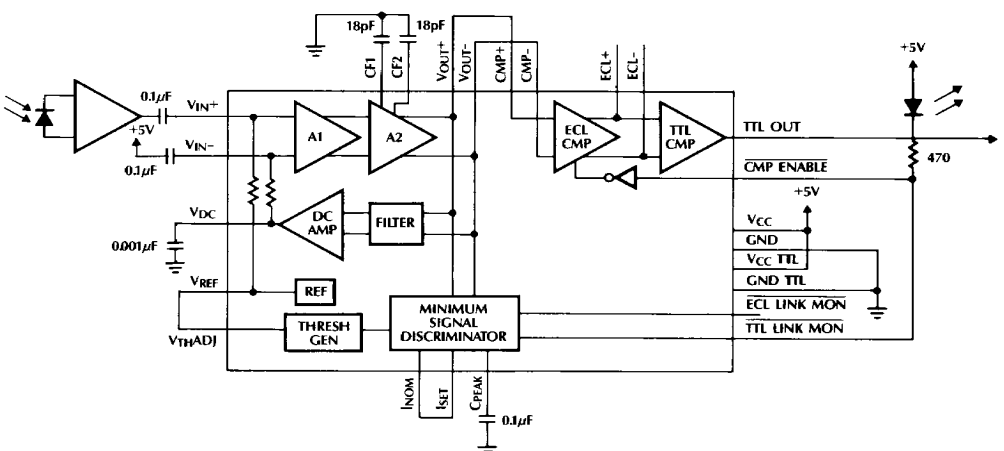


Figure 1. The ML4621 Configured for 20MHz Bandwidth with TTL Output

LINK MONITOR (ML4621)

This function is implemented by the Minimum Signal Discriminator and the Threshold Generator circuits. The purpose of this function is to monitor the input signal and provide a status signal indicating when the input falls below a preset voltage level. This is done by peak detecting the output of the amplifier section and comparing this level with the voltage at $V_{TH}ADJ$.

The equation which determines the droop rate of the peak detector is

$$\frac{dV}{dt} = \frac{I_{ISET}}{C} \quad (3)$$

In this equation C is the peak capacitor at C_{PEAK}. On the ML4621 the droop rate of the peak detector can be adjusted two ways:

1) By adjusting the value of the peak capacitor at C_{PEAK}.
2) By adjusting the charge current into the peak capacitor at I_{SET}.

The charge current, I_{ISET}, can be controlled externally by connecting a resistor, R_{EXT}, between I_{ISET} and V_{CC}. I_{ISET} will then be

$$I_{ISET} = \frac{V_{CC} - 0.7}{R_{EXT} + 1700} \quad (4)$$

For convenience, an on-chip current source of 125μA is available by connecting I_{NOM} to I_{SET}.

The Threshold Generator level shifts the reference voltage at $V_{TH}ADJ$ through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum *peak* voltage at the input which will trigger the Link Monitor) is:

$$V_{TH}ADJ = 600V_{TH} + 0.7 \quad (5)$$

The on-chip reference voltage, V_{REF}, can be tied directly to $V_{TH}ADJ$ to set the threshold level. This will set the minimum input signal on the ML4621 at about 3mV (peak).

A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in figure 3.

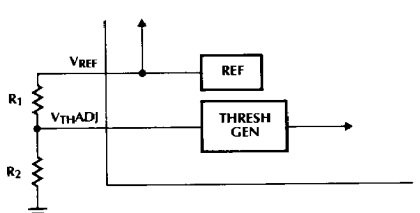


Figure 3.

Since the ML4621 has a relatively low input impedance of 6.8K and is offset by one diode drop, the equation which accounts for the load and offset is:

$$V_{TH}ADJ = \frac{R_2(6800V_{REF} + 0.7R_1)}{6800(R_1 + R_2) + R_1R_2} \quad (8)$$

LINK MONITOR (ML4622)

The ML4622 Link Monitor circuit operates slightly different than the ML4621. Instead of using the droop rate of the peak detector to determine the time for the link monitor to shut off, the ML4622 uses both a threshold detector to measure the peaks and a timer to measure the time between the peaks.

The equation which determines the time between peaks is:

$$\frac{C_{PEAK} \times R_{PEAK}}{4.3}$$

where $500\Omega < R_{PEAK} < 200k\Omega$ and R_{PEAK} is in parallel with C_{PEAK}

The threshold generator level shifts the reference voltage at $V_{TH}ADJ$ through a circuit that has a temperature coefficient matching the limiting amplifier. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum peak voltage at the input which will trigger the Link Monitor) is:

$$V_{TH}ADJ = 800\ V_{TH}$$

The on-chip reference voltage, V_{REF}, can be tied directly to $V_{TH}ADJ$ to set the threshold level. This will set the minimum input signal to about 6.5mV peak.

A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in figure 3.

THRESHOLD ADJUSTMENT EXAMPLE

If you are using the ML4621 and you want the Link Monitor to trigger when the received optical power goes below 1μW (–30dBm), you first need to calculate the resultant voltage at $V_{IN}+$ and $V_{IN}-$. If you are using the Hewlett-Packard HFBR-24X6 Fiberoptic Receiver with a responsitivity of 8mV/μW, the peak-to-peak voltage would be:

$$1\mu W \times 8mV/\mu W = 8mV_{P-P} \quad (9)$$

So the Link Monitor should trigger at some point slightly lower than 4mV peak, say 3mV. Setting V_{TH} in equation 5 to 3mV and solving for $V_{TH}ADJ$ yields:

$$V_{TH}ADJ = 600(.003) + 0.7 = 2.5V$$

This is a convenient value since the reference voltage supplied by the Quantizer, V_{REF}, is 2.5V.

The Link Monitor has about 0.4mV (peak) hysteresis built-in. The ML4622 has about 1dB hysteresis built-in. More hysteresis can be induced by connecting a resistor between TTL LINK MON and $V_{TH}ADJ$ creating a positive feedback loop.

Refer to Micro Linear's Application Note 6 for more detail.

BURST MODE

In some fiber optic links, the idle signal is DC, or of a frequency that is substantially different from the data. For these links, a faster response time of the DC loop and the Link Monitor is required.

The ML4622 has been designed to accommodate these two requirements. The input coupling capacitors can be relatively small and still maintain stability. The smaller the input coupling capacitors are, the faster the DC loop response time is. The Link Monitor is also enhanced to have a faster response time.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4621CP	0°C to +70°C	MOLDED DIP
ML4621CQ	0°C to +70°C	MOLDED PCC
ML4622CP	0°C to +70°C	MOLDED DIP
ML4622CS	0°C to +70°C	MOLDED SOIC