Universal Active ORing Controller IC

Description

The PI2003 ***Cool-ORing®*** solution is a universal high-speed Active ORing controller IC designed for use with N-channel MOSFETs and is optimized for -48V redundant power system architectures. The PI2003 *Cool-ORing* controller enables an extremely low power loss solution with fast dynamic response to input power fault conditions, critical for high availability systems. The PI2003 controls single or parallel MOSFETs to address Active ORing applications protecting against power source failures. The PI2003 is optimized for -48V low-side Active ORing applications. An internal VC shunt regulator enables biasing of the controller directly from -48V (GND).

The gate drive output turns the MOSFET on during normal steady state operation, while achieving high-speed turn-off during input power source fault conditions, that cause reverse current flow, with auto-reset once the fault clears. The MOSFET drain-to-source voltage is monitored to detect normal forward, excessive forward, light load and reverse current flow. The PI2003 provides an active low fault flag output to the system during excessive forward current, reverse current and light load.

Typical Applications:

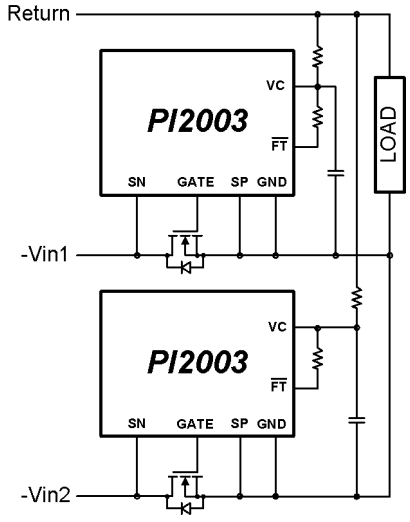


Figure 1: PI2003 Low-Side Active ORing

Features

- Optimized for -48V ORing applications
- Fast Dynamic Response to Power Source failures, with 160ns reverse current turn-off delay time
- 4A gate discharge current
- Accurate MOSFET drain-to-source voltage sensing to indicate system level fault conditions
- Low quiescent current enables biasing directly from -48V (GND).
- 100V for 100ms operation in low side applications
- Active low fault flag output

Applications

- Low-side -48Vbus Active ORing
- N+1 Redundant Power Systems
- Servers & High End Computing
- Telecom Systems
- High current Active ORing

Package Information

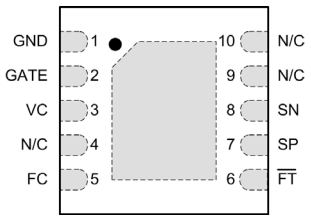
The PI2003 is offered in the following packages:

- 10 Lead 3mm x 3mm DFN package
- 8 Lead SOIC package

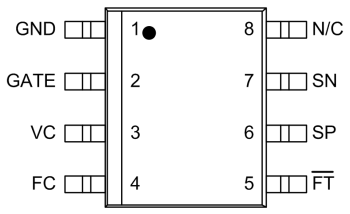
Pin Description

Pin Name	Pin Number		Description
	10 Lead DFN	8 Lead SOIC	
GND	1	1	**Ground:** This pin is ground for the gate driver and control circuitry.
GATE	2	2	**Gate Drive Output:** This pin drives the gate of the external N-channel MOSFET. Under normal operating conditions, the GATE pin pulls high to VC-0.5V. The controller turns the gate off during a reverse current fault that exceeds the reverse voltage threshold.
VC	3	3	**Controller Input Supply:** This pin is the supply pin for the control circuitry and gate driver. Connect a 1µF capacitor between VC pin and the GND pin. Voltage on this pin is limited to 11V by an internal shunt regulator. For high voltage auxiliary supply applications connect a shunt resistor between VC and the auxiliary supply.
FC	5	4	**Fault Clamp Input:** Connect the $\overline{FT}$ pin to FC when it is pulled by a resistor to a voltage higher than the VC pin to clamp it to VC plus a diode. Leave this pin open if unused.
$\overline{FT}$	6	5	**Fault State Output:** This open collector pin pulls low when a fault occurs. Fault logic inputs are VC Under-Voltage, Reverse Current, Forward Over-Current, and light load. Leave this pin open if unused.
SP	7	6	**Positive Sense Input & Clamp:** Connect SP pin to the Source pin of the external N-channel MOSFET close to the GND pin. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.
SN	8	7	**Negative Sense Input & Clamp:** Connect SN to the Drain pin of the external N-channel MOSFET. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.

Package Pin-Outs



10 Lead DFN (3mm x 3mm)
Top view



8 Lead SOIC (5mm x 6mm)
Top view

Absolute Maximum Ratings

VC	-0.3V to 17.3V / 40mA
SP	-0.3V to 8.0V / 10mA
FC, $\overline{FT}$	-0.3V to 17.3V / 10mA
GATE	-0.3V to 17.3V / 5A
SN (Continuous)	-0.3V to 80V / 10mA
SN (100ms Pulse)	100V / 10mA
GND	-0.3V / 5A peak
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 150°C
Lead Temperature (Soldering, 20 sec)	250°C
ESD Rating	2kV HBM

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =9.5V, C_{Vc} = 1uF, C_{GATE} = 4nF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VC Supply						
Operating Supply Range (3)	V_{VC-GND}	8.5		9.5	V	No VC limiting Resistors
Quiescent Current	I_{VC}		1.5	2.0	mA	Normal Operating Condition, No Faults,
VC Clamp Voltage	V_{VC-CLM}	10	11	12	V	I_{VC} = 3mA
VC Clamp Shunt Resistance	R_{VC}			10	Ω	Delta I_{VC}=10mA
VC Under-Voltage Rising Threshold	V_{VCUVR}		7.15	8.5	V	
VC Under-Voltage Falling Threshold	V_{VCUVF}	6.0	7.00		V	
VC Under-Voltage Hysteresis	$V_{VCUV-HS}$		150		mV	
FAULT						
Fault Output Low Voltage	V_{FTL}		0.2	0.5	V	I_{FT} = 4mA, VC > 4.5V
Fault Output High Leakage Current	I_{FT-LC}			10	µA	V_{FT}=14V
Fault Delay Time	t_{FT-DEL}	20	40	60	µs	
Fault Clamp (FC to VC)	V_{FC-VC}		0.7	1.2	V	I_{DC} ≤ 5mA

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =9.5V, C_{Vc} = 1uF, C_{GATE} = 4nF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
DIFFERENTIAL AMPLIFIER AND COMPARATORS						
Common Mode Input Voltage	V_{CM}	-0.1		1	V	SP to GND, SN to GND
Differential Operating Input Voltage	V_{SP-SN}	-50		200	mV	SP-SN
SP Input Bias Current	I_{SP}	-8	-1		µA	SP=SN=1V
SN Input Bias Current	I_{SN}	-8	-1		µA	SP=SN=1V
SN Leakage Current	I_{SN}		7	9	mA	V_{SN} = 80V,SP =0V
Reverse Comparator Off Threshold	V_{RVS-TH}	-9	-6	-3	mV	SP=SN=1V
Reverse Comparator Hysteresis	V_{RVS-HS}		3		mV	SP=SN=1V
Reverse Fault to Gate Turn-off Delay Time	t_{RVS-MS}		160	190	ns	V_{SP-SN} = ± 50mV step to 90% of V_G max, V_{BK}=0 (minimum blanking)
Forward Comparator On Threshold	V_{FWD-TH}	3	6	9	mV	
Forward Comparator Hysteresis	V_{FWD-HS}		-3		mV	
Forward Over-Current Comparator Threshold	V_{OC-TH}	135	150	165	mV	
Forward Over-Current Comparator Hysteresis	V_{OC-HS}		-15		mV	
GATE DRIVER						
Gate Source Current	I_{G-SC}		-150	-60	µA	V_G = 1V, Normal Operating Conditions, No Faults
Pull Down Peak Current(1)	I_{G-PD}	1.5	4.0		A	
Pull-down Gate Resistance (1)	R_{G-PD}		0.3		Ω	V_G = 1.5V @ 25°C
AC Gate Pull-down Voltage(1)	V_{G-PD}			0.2	V	
DC Gate Pull-down Voltage to GND	V_{G-PD}		0.8	1.2	V	I_G=100mA, in reverse fault
Gate Voltage @ VC UVLO	V_{G-UVLO}		0.7	1	V	I_G =10µA, 4.5V<VC<7.5V
Gate Voltage High	V_G	VC-0.5V	VC-0.25V		V	
Gate Fault Condition Clear; % of VC(1)	V_{VC-G}		50		%	
Gate Fall Time	t_{G-F}		10	15	ns	90% to 10% of V_G max.

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Refer to the *Auxiliary Power Supply* section in the *Application Information* for details on the VC requirement to meet the MOSFET Vgs requirement.

Functional Description:

The PI2003 *Cool-ORing* controller IC is designed to drive single or paralleled N-channel MOSFETs in Active ORing applications, and optimized for -48V applications. The PI2003 used with an external MOSFET can function as an ideal ORing diode in low side of a redundant power system, significantly reducing power dissipation and eliminating the need for heatsinking.

An N-channel MOSFET in the conduction path offers extremely low on-resistance resulting in a dramatic reduction of power dissipation versus the performance of a diode used in conventional ORing applications. This can allow for the elimination of complex heat sinking and other thermal management requirements. While the gate remains above the gate threshold voltage it will allow current to flow in the forward and reverse direction. Ideal ORing applications do not allow for reverse current flow, so the controller detect reverse current caused by input power source failures and turn off the the MOSFET as quickly as possible. Once the gate voltage falls below the gate threshold, the MOSFET is off and the body diode will be reverse biased preventing reverse current flow and subsequent excessive voltage droop on the redundant bus. During forward over-current conditions the controller maintains gate drive to keep the MOSFET forward drop and power dissipation as low as possible.
While conventional ORing solutions using diodes offer no protection against forward over-current conditions. The PI2003 will provide an active-low fault flag to the system via the $\overline{FT}$ pin. The fault flag is also issued during the reverse current condition, and light load or shorted MOSFET conditions.

Differential Amplifier:
The PI2003 integrates a high-speed low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high accuracy. The amplifier output is connected to three comparators: Reverse comparator, Forward comparator, and Forward over-current comparator.

Reverse Current Comparator: RVS

The reverse current comparator provides the most critical function in the controller, detecting negative voltage caused by reverse current. When the SN pin is 6mV higher than the SP pin, the reverse comparator will enable the gate discharge circuit and turn off the MOSFETs in typically 160ns.

The reverse comparator has typically 3mV of hysteresis referenced to SP-SN.

Forward Voltage Comparator: FWD

The FWD comparator detects when a forward current condition exists and SP is 6mV(typical) positive with respect to SN. When SP-SN is less than 6mV, the FWD comparator will assert the Fault flag to report a fault condition indicative of a light load or "load not present" condition or possible shorted MOSFET.

Forward Over Current Comparator: FOC

The FOC comparator indicates an excessive forward current condition when SP is 150mV(typical) higher than SN. When the GATE output voltage is greater than 50% of the VC voltage and SP-SN is higher than 150mV, the PI2003 will initiate a fault condition via the $\overline{FT}$ pin.

VC and Internal Voltage Regulator:
The PI2003 has a separate input (VC) that provides power to the control circuitry and the gate driver. An internal regulator clamps the VC voltage ($V_{VC\text{-}CLM}$) to 11V.

VC may be tied to a voltage higher than $V_{VC\text{-}CLM}$ through a resistor to limit VC current.

The internal regulator circuit has a comparator to monitor VC voltage and initiates a FAULT condition when VC is lower than the VC Under-Voltage Threshold, 7.15V

Gate Driver:
The gate driver (GATE) output is configured to drive an external N-channel MOSFET. In the high state, the gate driver applies a 150µA current source to the MOSFET gate limited to the VC voltage.

When a reverse current fault is initiated, the gate driver pulls the GATE pin low and discharges the FET gate with 4 Apeak capability.

When the input source voltage is applied before the MOSFET is fully enhanced, a voltage greater than the Forward Over Current (FOC) Threshold may be present across the MOSFET. To avoid an erroneous FOC detection, a VGS detector blanks the FOC and FWD comparators from initiating a fault, until the GATE pin reaches 50% of VC pin voltage.

Fault:

The fault circuit output is an open collector with 40µs delay to prevent any false triggering. The $\overline{FT}$ pin will be pulled low when any of the following faults occur:

- Reverse current
- Forward Over-Current and V_G > ½ VC
- Forward Low-Current and V_G > ½ VC

- VC pin Under-Voltage

Reverse current is the only fault condition that initiates gate turn-off of the MOSFET (as well as a fault flag signal). Forward Over-Current and Forward Low-Current fault conditions issue a fault flag signal to the $\overline{FT}$ pin, but do not affect the gate of the MOSFET. The $\overline{FT}$ pin serves as an indicator that a fault condition may be present. This information can be reported to a Host to signal that some system level maintenance may be required. The $\overline{FT}$ pin can be connected to VC pin or system logic bias voltage via a current limiting resistor.

When pulling up $\overline{FT}$ to an unregulated voltage connect FC to $\overline{FT}$. FC will clamp $\overline{FT}$ voltage to one diode drop above VC. This current will return to ground through the internal shunt.

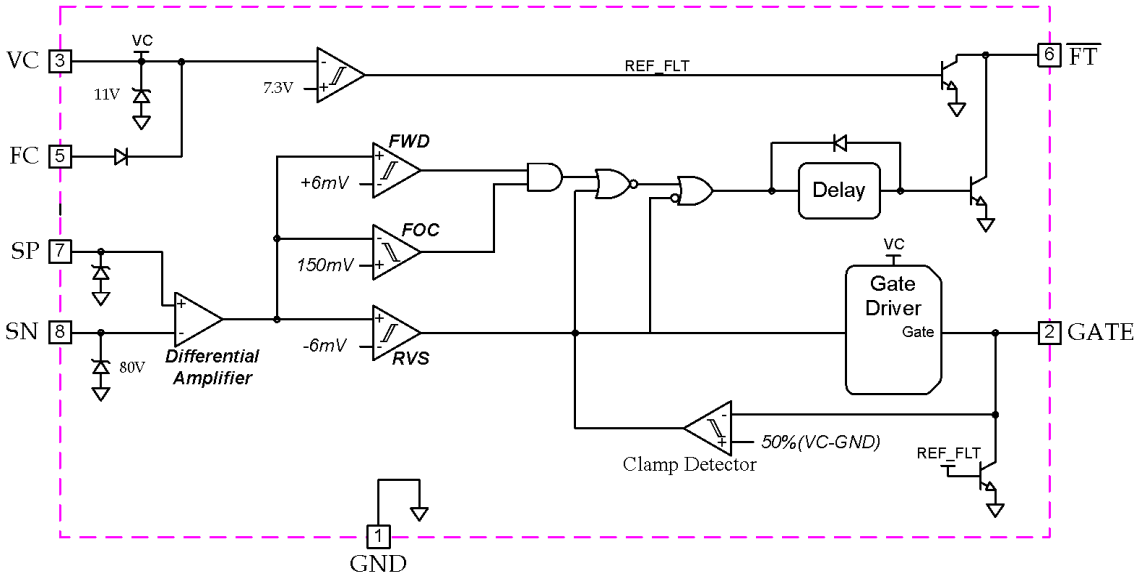


Figure 2: PI2003 Controller Internal Block Diagram (10 Lead DFN package pin out shown)

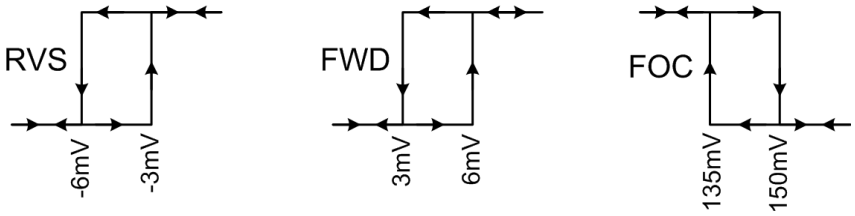


Figure 3: Comparator hysteresis, values are for reference only, please refer to the electrical specifications

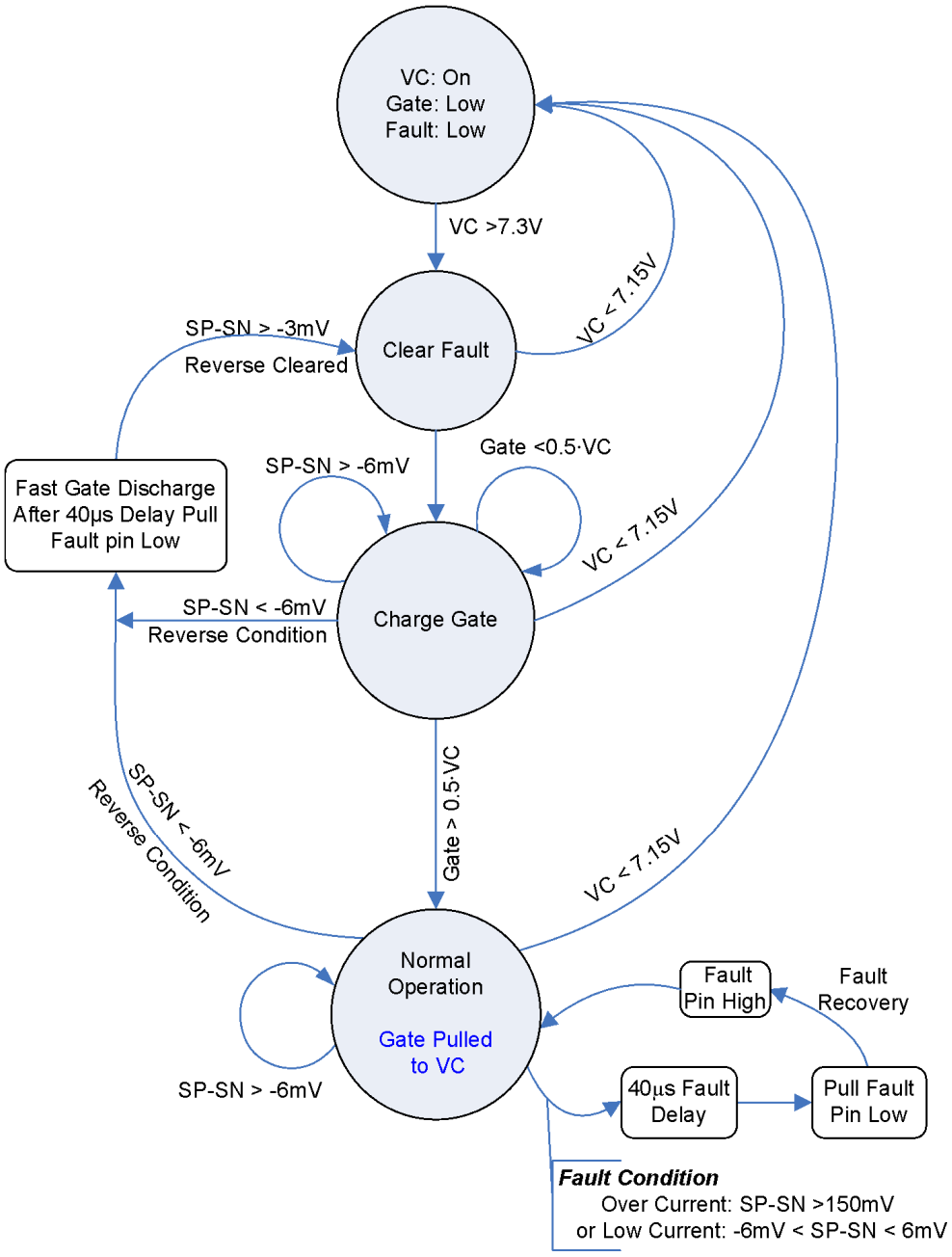
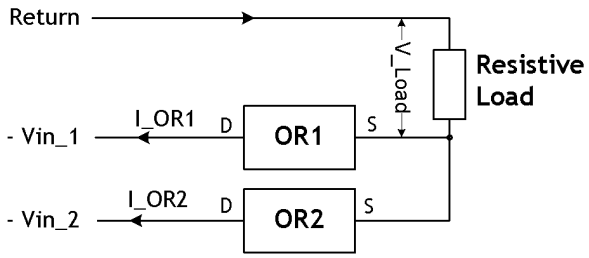


Figure 4: PI2003 State Diagram



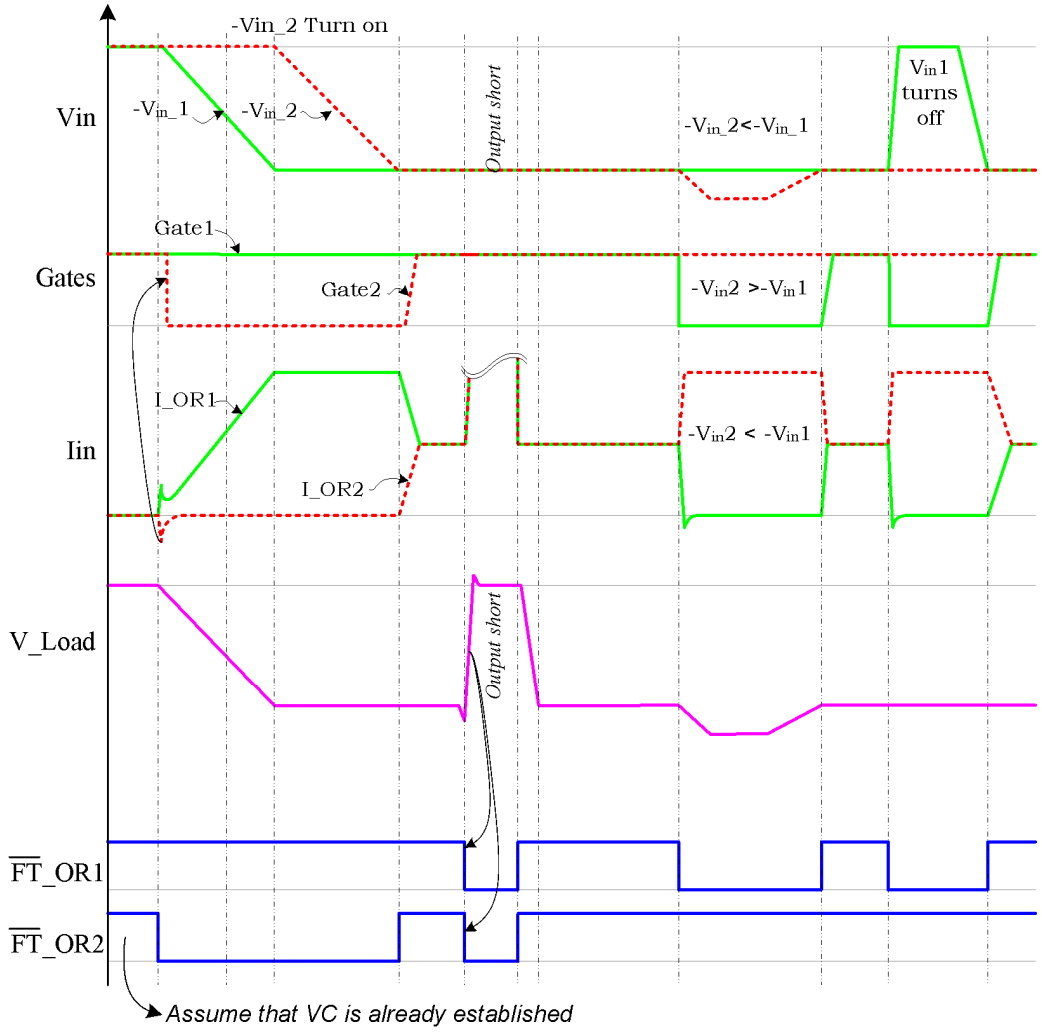


Figure 5: Timing diagram for two PI2003 controllers in a low side Active ORing application

Typical Characteristics:

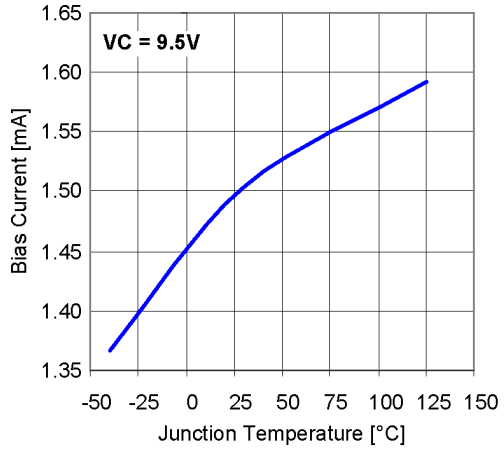


Figure 6: Controller bias current vs. temperature

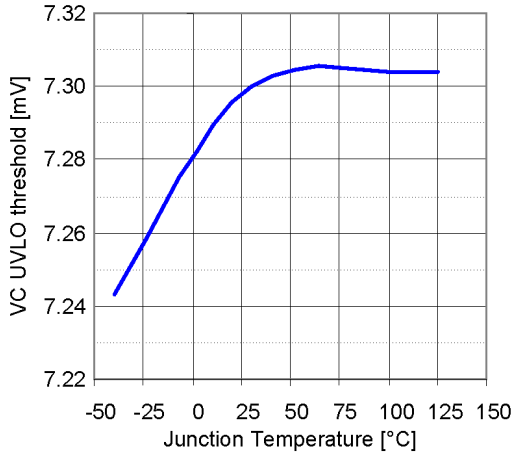


Figure 7: VC UVLO threshold vs. temperature

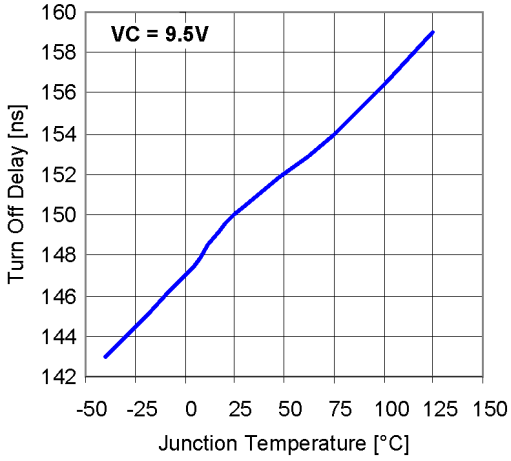


Figure 8: Reverse condition gate turn-off delay time vs. temperature.

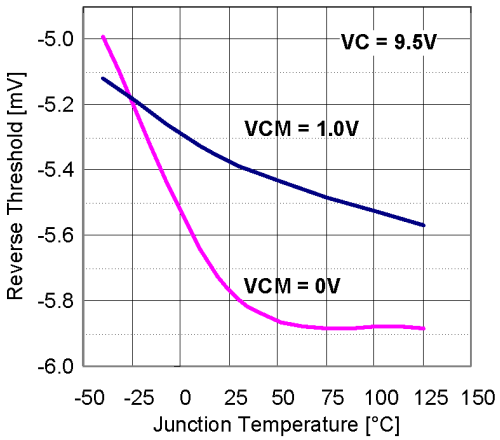


Figure 9: Reverse comparator threshold vs. temperature. ***VCM:*** *Common Mode Voltage*.

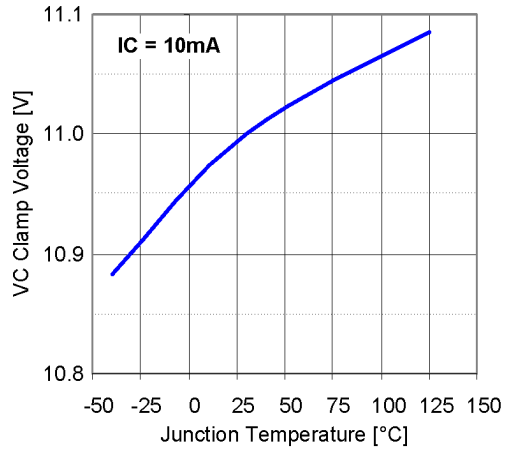


Figure 10: VC clamp voltage vs. temperature.

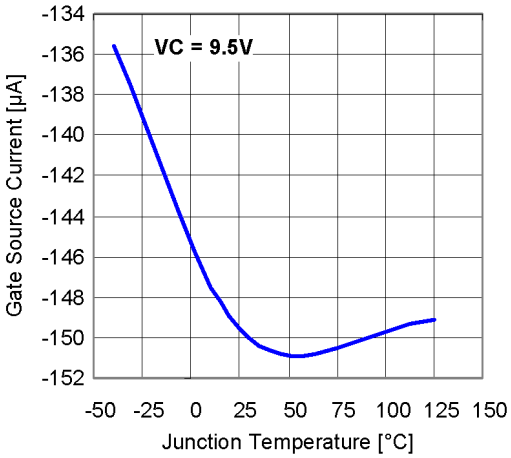


Figure 11: Gate output source current vs. temperature

Application Information:

The PI2003 is designed to replace ORing diodes in high current redundant power architectures. Replacing a traditional diode with a PI2003 controller IC and a low on-state resistance N-channel MOSFET will result in significant power dissipation reduction as well as board space reduction, efficiency improvement and additional protection features. This section describes in detail the procedure to follow when designing with the PI2003 Active ORing controller and N-Channel MOSFETs. The following is a low side Active ORing design example.

Fault Indication:

$\overline{FT}$ output pin is an open collector output and should be pulled up to the logic voltage or to the controller VC via a resistor (10KΩ). Also the $\overline{FT}$ output can be pulled with a current limiting resistor directly to an unregulated voltage source, such as the return of a -48V bus. In this condition connect the $\overline{FT}$ pin to the FC pin for clamping.

Also the $\overline{FT}$ pin can be used to drive an LED or opto-coupler device. The circuit in figure 12a shows a PI2003 configuration for an LED/opto-coupler that will turn on during a fault condition. The FC connection protects the $\overline{FT}$ pin if the LED is open.

Use the circuit in figure 12b to turn on the LED/opto-coupler when there is no fault and to turn off during a fault condition.

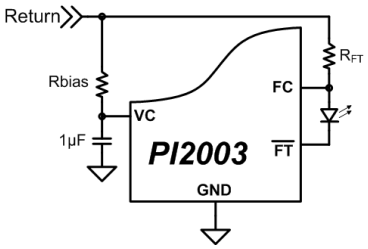


Figure 12a: Fault circuit where the LED turns on during a fault.

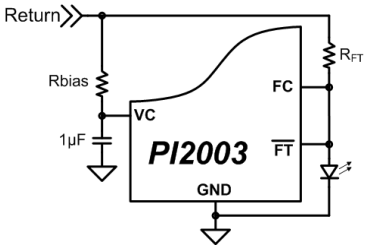


Figure 12b: Fault circuit where the LED turns off during a fault.

VC Power Source:

The PI2003 VC input voltage should be higher than the required gate-to-source voltage (Vgs) to fully enhance the MOSFET. The maximum gate to VC voltage loss (headroom), VHD_{VC-G} is 0.5V.

VHD_{VC-G} specification is the *Gate Voltage High* (V_G) in the Gate Driver section under the Electrical Specification.

If the bus voltage is higher than 11V then a bias resistor (Rbias) is required, and should be connected between the PI2003 VC pin and supply. The resistor is selected based on the input voltage range.

$$Rbias = \frac{Vbus_{\min} - VC_{clamp}}{IC_{\max}}$$

Rbias maximum power dissipation:

$$Pd_{Rbias} = \frac{(Vbus_{\max} - VC_{clamp})^2}{Rbias}$$

$Rbias$ maximum power dissipation is at maximum input voltage and minimum clamp voltage (11V).

Where:

$Vbus_{\min}$: V(bus) minimum voltage

$Vbus_{\max}$: V(bus) maximum voltage

VC_{Clamp} : Controller clamp voltage, 11V

$IC_{\max}$: Controller maximum bias current (2.0mA)

Note: If the $\overline{FT}$ pin is connected to the VC pin via a resistor (R_{FT}), the $\overline{FT}$ sink current (I_{FT}) during a fault condition should be added to the maximum bias current $IC_{\max}$ in the above equations.

The $\overline{FT}$ pin sink current during a fault can be calculated using the following approximate equation:

$$I_{FT} = \frac{VC_{clampMax}}{R_{FT}}$$

N-Channel MOSFET Selection:

There are several factors that affect the MOSFET selection including cost, on-state resistance (Rds(on)), current rating, power dissipation, thermal conductivity, drain-to-source breakdown voltage (BVdss), gate-to-source voltage rating (Vgs), and gate threshold voltage ($Vgs_{(TH)}$).

The first step is to select suitable MOSFETs based on the BVdss requirement for the application. The BVdss voltage rating should be higher than the applied Vin voltage plus expected transient voltages. Stray parasitic inductance in the circuit can also contribute to significant transient voltage conditions, particularly during MOSFET turn-off after a reverse

current fault has been detected. In Active ORing applications when one of the input power sources is shorted, a large reverse current is sourced from the circuit output through the MOSFET. Depending on the output impedance of the system, the reverse current may reach over 60A in some conditions before the MOSFET is turned off. Such high current conditions will store energy even in a small parasitic element. For example, a 1nH parasitic inductance with 60A reverse current will store 1.8µJ (½Li^2). When the MOSFET is turned off, the stored energy will be released and will produce high negative voltage ringing at the MOSFET source. This event will create a high voltage difference across the drain and source of the MOSFET.

The MOSFET current rating and maximum power dissipation are closely related. Generally the lower the MOSFET Rds(on), the higher the current capability and the lower the resultant power dissipation. This leads to reduced thermal management overhead, but will ultimately be higher cost compared to higher Rds(on) parts. It is important to understand the primary design goal objectives for the application in order to effectively trade off the performance of one MOSFET versus another.

Power dissipation in active ORing circuits is derived from the total source current and the on-state resistance of the selected MOSFET.

MOSFET power dissipation:

$$Pd_{MOSFET} = Is^2 * Rds(on)$$

Where :
Is : Source Current
Rds(on) : MOSFET on-state resistance

Note:
In the calculation use Rds(on) at maximum MOSFET temperature because Rds(on) is temperature dependent. Refer to the normalized Rds(on) curves in the MOSFET manufacturers datasheet. Some MOSFET Rds(on) values may increase by 50% at 125°C compared to values at 25°C.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$Trise_{MOSFET} = Rth_{JA} * Pd_{MOSFET} = Rth_{JA} * Is^2 * Rds(on),$$

Where:
Rth_{JA}: Junction-to-Ambient thermal resistance

Rds(on) and PI2003 sensing:

The PI2003 senses the MOSFET source-to-drain voltage drop via the SP and SN pins to determine the status of the current through the MOSFET. When the MOSFET is fully enhanced, its source-to-drain voltage is equal to the MOSFET on-state resistance multiplied by the source current, V_{SD} = Rds(on)*Is. The reverse current threshold is set for -6mV and when the differential voltage between the SP & SN pins is more negative than -6mV, i.e. SP-SN≤-6mV, the PI2003 detects a reverse current fault condition and pulls the MOSFET gate pin low, thus turning off the MOSFET and preventing further reverse current. The reverse current fault protection disconnects the power source fault condition from the redundant bus, and allows the system to keep running.

Under normal conditions the GATE pin output voltage will rail to the VC voltage minus 0.5V, where the VC output is regulated to 11V typically to support any MOSFET with a Vgs rating of ±12V or greater. A Vgs rating ≥ 12V is very common for industry standard N-Channel MOSFETs.

Typical application Example 1:

Requirement:

Redundant Bus Voltage = -48V (-36V to -60V, 100V for 100ms transient)

Load Current = 5A load (assume through each redundant path)

Maximum Ambient Temperature = 60°C

Solution:

A single PI2003 with a suitable MOSFET for each redundant -48V power source should be used and configured as shown in figure 13. The VC is biased from the return line through a bias resistor.

Select a suitable N-Channel MOSFET: Select the N-Channel MOSFET with voltage rating higher than the input voltage, Vin, plus any expected transient voltages, with a low Rds(on) that is capable of supporting the full load current with margin. For instance, a 100V rated MOSFET with 10A current capability is suitable. An exemplary MOSFET having these characteristic is Si4486EY from Vishay Siliconix.

From Si4486EY datasheet:

- N-Channel MOSFET
- V_{DS}= 100V
- I_D = 23A continuous drain current at 125°C
- $V_{GS(MAX)} = \pm 20V$
- $R_{\theta JA}$= 50°C/W
- $R_{DS(on)}$=20mΩ typical at V_{GS}=10V, T_J=25°C

Reverse current threshold is:

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{20m\Omega} = -300mA$$

Power dissipation:

Rds(on) is 25mΩ maximum at 25°C and will increase as the temperature increases. Add 40°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 100°C (60°C + 40°C) Rds(on) will increase by 63%.

$Rds(on) = 25m\Omega * 1.63 = 41m\Omega$ maximum at 100°C

Maximum Junction temperature

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 41m\Omega\right) = 111°C$$

Recalculate based on calculated Junction temperature, 115°C.

At 115°C Rds(on) will increase by 72%.

$Rds(on) = 25m\Omega * 1.72 = 43m\Omega$ maximum at 115°C

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 43m\Omega\right) = 113°C$$

$\overline{FT}$ **pin**: Connect the $\overline{FT}$ pin to to the logic power supply or to the VC pin via a resistor (R_{FT}). Make R_{FT} large (120KΩ) to lower $\overline{FT}$ sink current.

$$I_{FT-Sink} = \frac{VC}{R_{FT}} = \frac{11.0V}{120K\Omega} = 92\mu A$$

VC: Connect each controller to the return path with a separate bias resistor, Rbias.

$$Rbias = \frac{Vbus_{\min} - VC_{clampMax}}{IC_{\max} + I_{FT-Sink}}$$

$Rbias = \frac{36V - 12V}{2.0mA + 0.092mA} = 11.47K\Omega$, or 11.5KΩ, 1%

$Rbias$ maximum power dissipation is at maximum input voltage and minimum clamp voltage.

$$Pd_{Rbias} = \frac{(Vbus_{\max} - VC_{clampMIN})^2}{Rbias} = \frac{(60V - 12V)^2}{11.5K\Omega} = 200mW$$

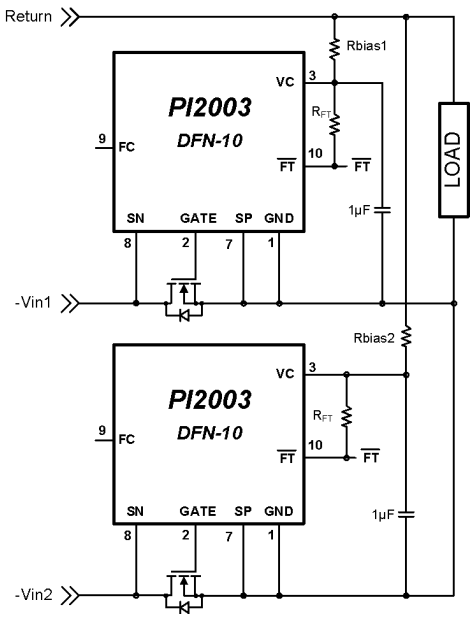


Figure 13: PI2003 in low side -48V application.

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for a DFN PI2003 and SO-8/PowerPak MOSFET is shown in Figure 14:

- It is best to connect the gate of the MOSFET to the GATE pin of the controller with a short and wide trace.
- Connections from the SP and SN pins to the MOSFET source and drain pins respectively should be as short as possible
- The VC bypass capacitor (C1 and C2) should be located as close as possible to the VC and GND pins. Place the PI2003 and VC bypass capacitor on the same layer of the board.
- Connect all MOSFET source pins together with a wide trace to reduce trace parasitics and to accommodate the high current input. Similarly, connect all MOSFET Drain pins together with a wide trace to accommodate the high current output.

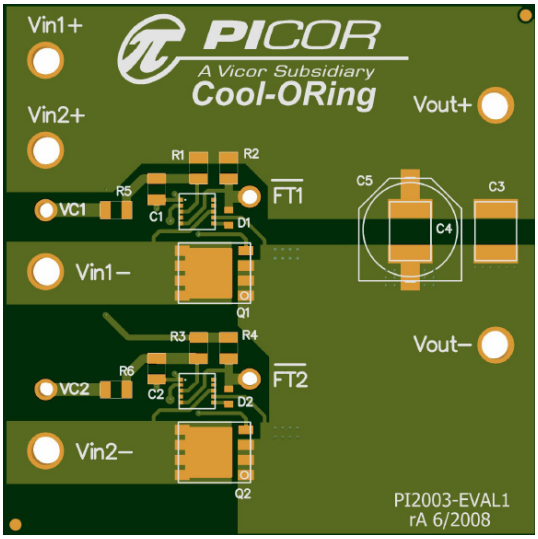


Figure 14: PI2003 and MOSFET layout example

Figure 24: PI2003 Mounted on PI2003-EVAL1

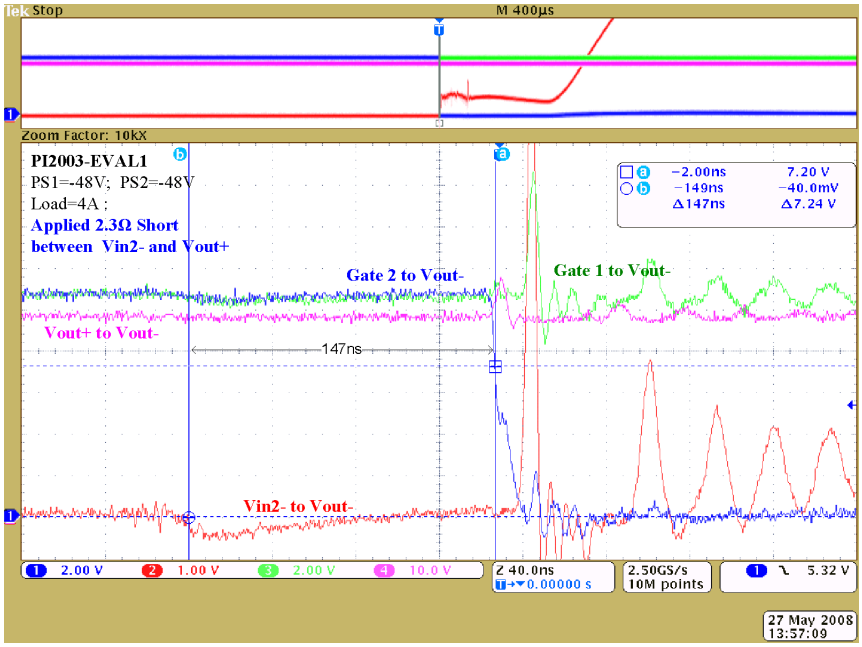
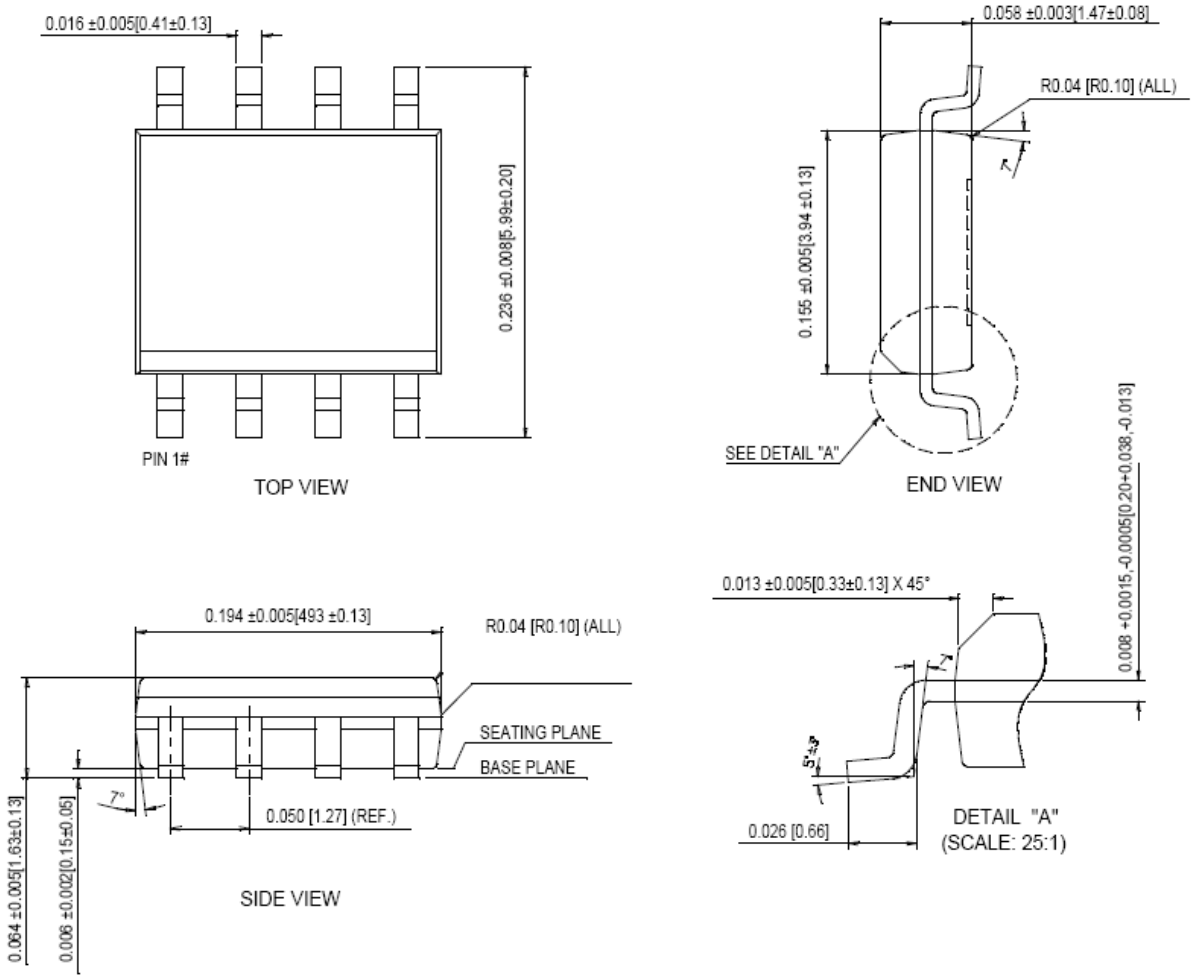


Figure 25: PI2003-EVAL1 performance under an input short

Please visit www.picorpower.com for information on PI2003-EVAL1

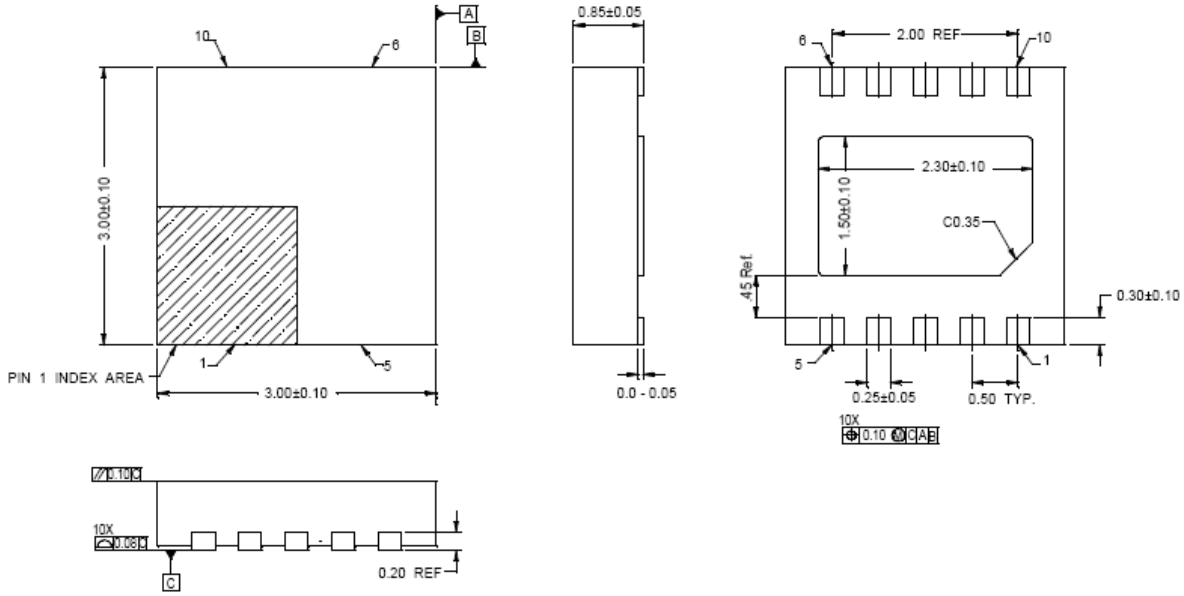
Package Drawings
8 Lead SOIC



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN INCHES [MM]
2. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 [0.15] PER SIDE
3. FORMED LEADS SHALL BE PLANAR WITH REPECT TO ONE ANOTHER WITHIN 0.003 [0.08] AT SEATING PLANE
4. GENERAL ANGLE TOLERANCES TO BE +/-2"
5. GENERAL TOLERANCES TO BE +/- 0.005 [0.13]
6. THIS POD COMPLIES TO MS-012 ISSUE C

Package Drawings
10 Lead DFN



NOTES :

1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity does not exceed .05mm
3. Package is variation of JEDEC MO-229
4. Warpage does not exceed .05mm

Ordering Information

Part Number	Package	Transport Media
PI2003-00-QEIG	3mm x 3mm 10 Lead DFN	T&R
PI2003-00-SOIG	8 Lead SOIC	T&R

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