

CYPRESS
SEMICONDUCTOR

PRELIMINARY

T-46-23-14

CY7C108

CY7C109

131,072 x 8 Static R/W RAM

Features

- High speed
— $t_{AA} = 25$ ns
- CMOS for optimum speed/power
- Low active power
— 825 mW
- Low standby power
— 165 mW
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{OE}$ options

Functional Description

The CY7C108 and CY7C109 are high-performance CMOS static RAMs organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable ($\overline{CE}_2$), an active LOW output enable ($\overline{OE}$), and three-state drivers. Both devices have an automatic power-down feature that reduces power consumption by more than 70% when deselected.

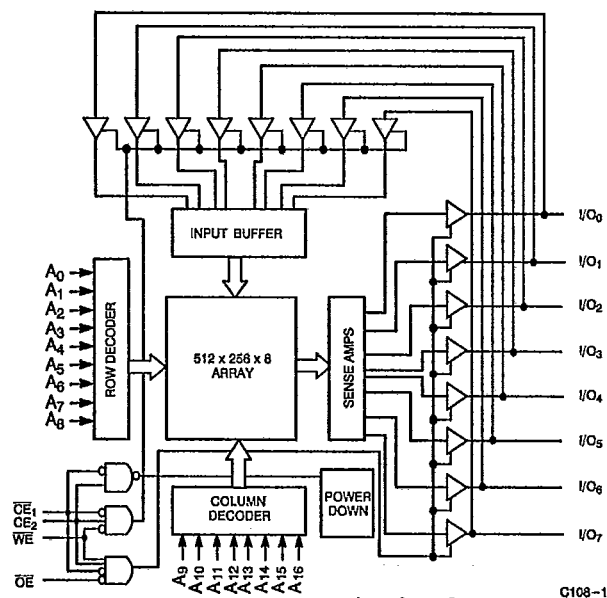
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two ($\overline{CE}_2$) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two ($\overline{CE}_2$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

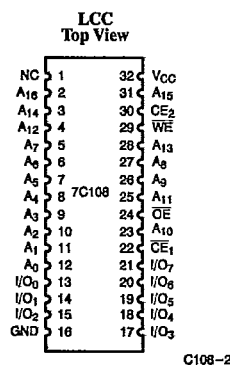
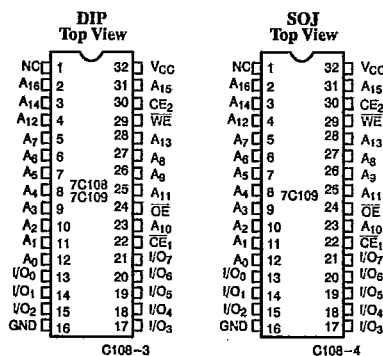
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $\overline{CE}_2$ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, $\overline{CE}_2$ HIGH, and $\overline{WE}$ LOW).

The CY7C108 is available in a 32-pin rectangular leadless chip carrier and standard 600-mil-wide cerDIPs. The CY7C109 is available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configurations





PRELIMINARY

CY7C108

CY7C109

Selection Guide

T-46-23-14

		7C108-25 7C109-25	7C108-35 7C109-35	7C108-45 7C109-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	150	125	115
	Military	150	125	115
Maximum Standby Current (mA)	Commercial	30	25	25
	Military	35	30	30



SRAMs

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to + 150°C

Ambient Temperature with

Power Applied - 55°C to + 125°C

Supply Voltage on V_{CC} Relative to GND^[1] - 0.5V to + 7.0V

DC Voltage Applied to Outputs

in High Z State^[1] - 0.5V to + 7.0VDC Input Voltage^[1] - 0.5V to + 7.0V

Current into Outputs (Low) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military	- 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameters	Description	Test Conditions	7C108-25 7C109-25		7C108-35 7C109-35		7C108-45 7C109-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	150		125		115	mA
			Mil	150		125		115	
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	30		25		25	mA
			Mil	35		30		30	
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	10		10		10	mA
			Mil	10		10		10	

Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	10	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	12	pF

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.2. T_A is the "instant on" case temperature.

3. See the last page of this specification for Group A subgroup testing information.

4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

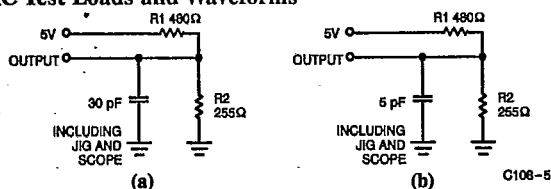
5. Tested initially and after any design or process changes that may affect these parameters.



PRELIMINARY

T-46-23-14

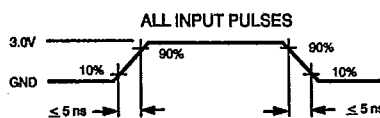
AC Test Loads and Waveforms



Equivalent to: **THÉVENIN EQUIVALENT**

167Ω

OUTPUT ○ ———— ○ 1.73V



C108--B

Switching Characteristics^[2,6] Over the Operating Range

Parameters	Description	7C108–25 7C109–25		7C108–35 7C109–35		7C108–45 7C109–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		35		45		ns
t _{AA}	Address to Data Valid		25		35		45	ns
t _{OHA}	Data Hold from Address Change	5		5		5		ns
t _{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE ₂ HIGH to Data Valid		25		35		45	ns
t _{DOE}	OE LOW to Data Valid		10		15		20	ns
t _{LZOE}	OE LOW to Low Z	0		0		0		ns
t _{HZOE}	OE HIGH to High Z ^[7]		10		15		20	ns
t _{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE ₂ HIGH to Low Z ^[8]	5		5		5		ns
t _{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE ₂ LOW to High Z ^[7,8]		10		15		20	ns
t _{PU}	$\overline{CE}_1$ LOW to Power-Up, CE ₂ HIGH to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE ₂ LOW to Power-Down		25		35		45	ns
WRITE CYCLE ^[9,10]								
t _{WC}	Write Cycle Time	25		35		45		ns
t _{SCE}	$\overline{CE}_1$ LOW to Write End, CE ₂ HIGH to Write End	20		25		30		ns
t _{AW}	Address Set-Up to Write End	20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t _{SD}	Data Set-Up to Write End	15		20		25		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[7]	5		5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[7,8]		10		15		20	ns

Notes:

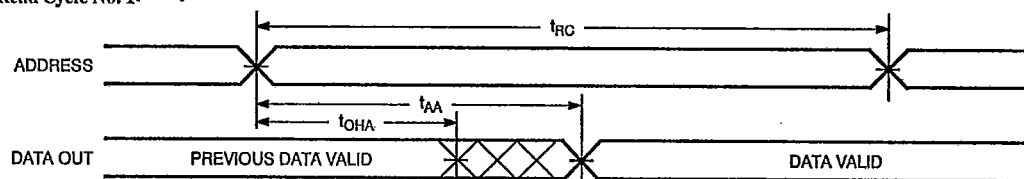
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$, $\overline{LOW}$, $\overline{CE_2}$ HIGH, and $\overline{WE}$ LOW. $\overline{CE_1}$ and $\overline{WE}$ must be LOW and $\overline{CE_2}$ HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .



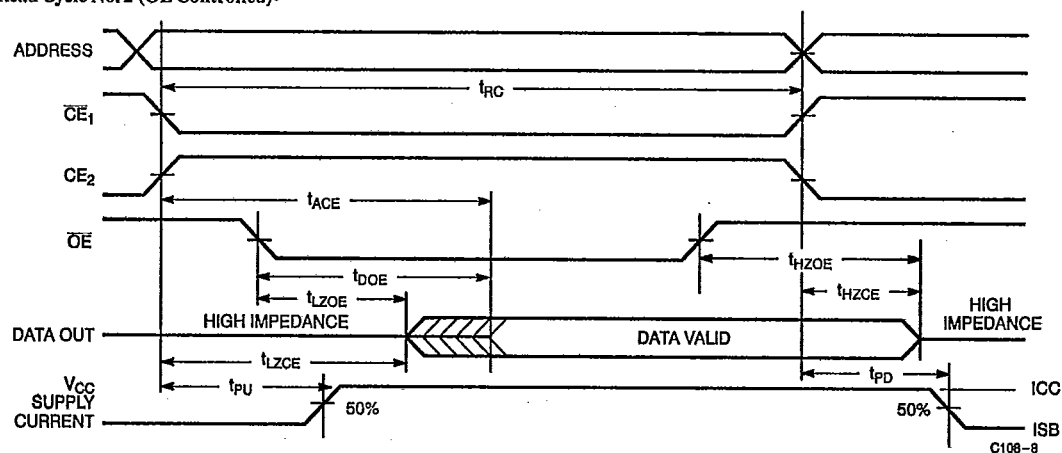
PRELIMINARY

CY7C108
CY7C109

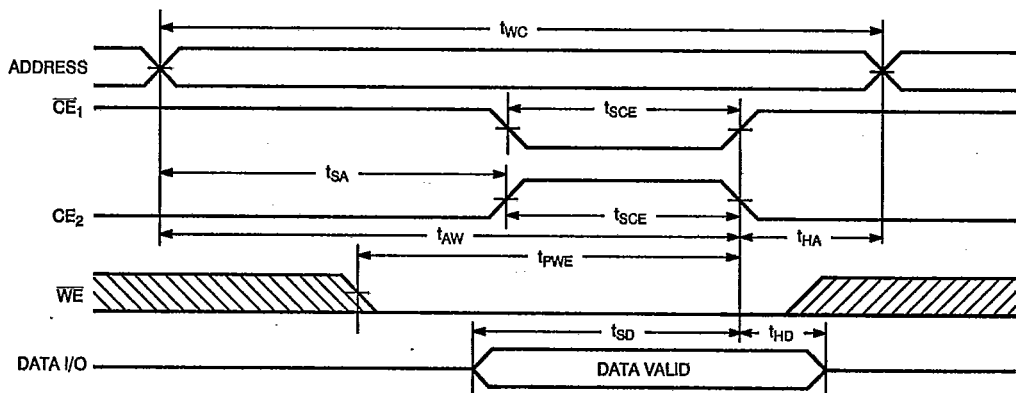
Switching Waveforms

Read Cycle No. 1^[11, 12]

C108-7

Read Cycle No. 2 ($\overline{OE}$ Controlled)^[11, 13]

C108-8

Write Cycle No. 1 ($\overline{CE}_1$ or $\overline{CE}_2$ Controlled)^[14, 15]

C108-9

Notes:

11. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IH}$.12. $\overline{WE}$ is HIGH for read cycle.13. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and $\overline{CE}_2$ transition HIGH.14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.15. If $\overline{CE}_1$ goes HIGH or $\overline{CE}_2$ goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.



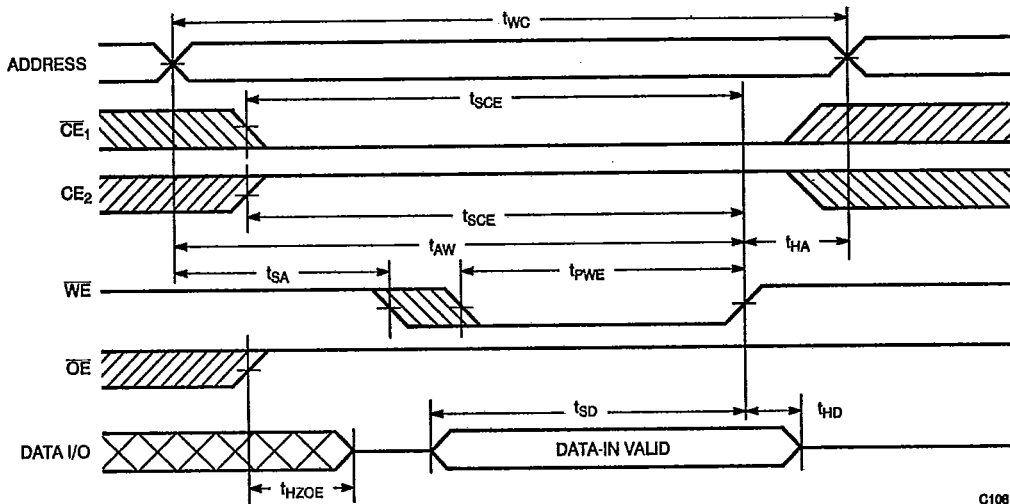
PRELIMINARY

CY7C108

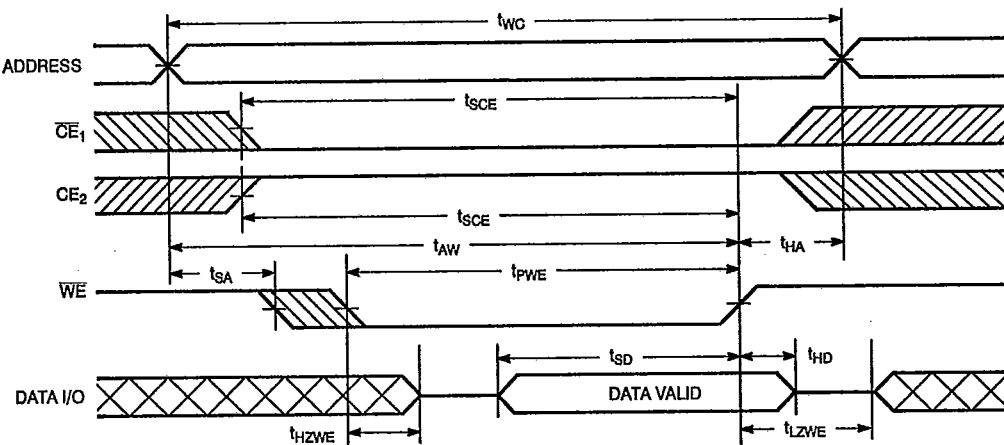
CY7C109

Switching Waveforms

T-46-23-14

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)^[14,15]

C108-10

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)^[10, 15]

C108-11



PRELIMINARY

CY7C108

CY7C109

Truth Table

T-46-23-14

CE ₁	CE ₂	OE	WE	I/O ₀ - I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I _{SB})
X	L	X	X	High Z	Power-Down	Standby (I _{SB})
L	H	L	H	Data Out	Read	Active (I _{CC})
L	H	X	L	Data In	Write	Active (I _{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})



SRAMS

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C108-25DC	D50	Commercial
	CY7C108-25LC	L75	
	CY7C108-25DMB	D50	Military
	CY7C108-25LMB	L75	
35	CY7C108-35DC	D50	Commercial
	CY7C108-35LC	L75	
	CY7C108-35DMB	D50	Military
	CY7C108-35LMB	L75	
45	CY7C108-45DC	D50	Commercial
	CY7C108-45LC	L75	
	CY7C108-45DMB	D50	Military
	CY7C108-45LMB	L75	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C109-25DC	D46	Commercial
	CY7C109-25PC	P43	
	CY7C109-25VC	V33	Military
	CY7C109-25DMB	D46	
35	CY7C109-35DC	D46	Commercial
	CY7C109-35PC	P43	
	CY7C109-35VC	V33	Military
	CY7C109-35DMB	D46	
45	CY7C109-45DC	D46	Commercial
	CY7C109-45PC	P43	
	CY7C109-45VC	V33	Military
	CY7C109-45DMB	D46	



PRELIMINARY

CY7C108

CY7C109

MILITARY SPECIFICATIONS

Group A Subgroup Testing

T-46-23-14

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Document #: 38-00140-C