INTERSIL

ICM7224 (LCD)
ICM7225 (LED)
4½ Digit Counter/ Decoder/Drivers

FEATURES

- **High frequency counting - guaranteed 15MHz, typically 25MHz at 5V**
- **Low power operation - less than 100μW quiescent**
- **Store and Reset inputs permit operation as frequency or period counter**
- **True count inhibit disables first counter stage**
- **Carry output for cascading four-digit blocks**
- **Schmitt-trigger on the count input allows operation in noisy environments or with slowly changing inputs**
- **Leading zero blanking input and output for correct leading zero blanking with cascaded devices**
- **LCD devices provide complete onboard oscillator and divider chain to generate backplane frequency, or backplane driver may be disabled allowing segments to be slaved to a master backplane signal**
- **LED devices provide Brightness input which can function digitally as a display enable or with a single potentiometer as a continuous display brightness control**

GENERAL DESCRIPTION

The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The count input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry, which allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The carry output allows the counter to be cascaded, while the leading zero blanking input and output allows correct leading zero blanking between four-decade blocks. The backplane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display. In LED systems, the brightness input to several ICM7225 devices may be ganged to one potentiometer.

The ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic package.

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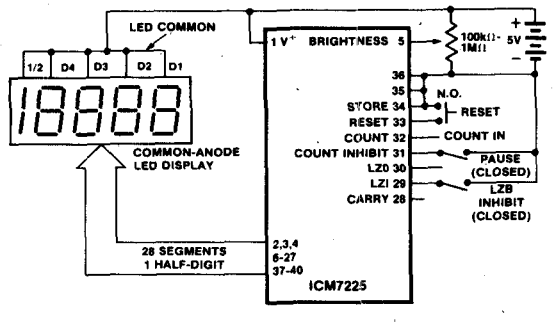
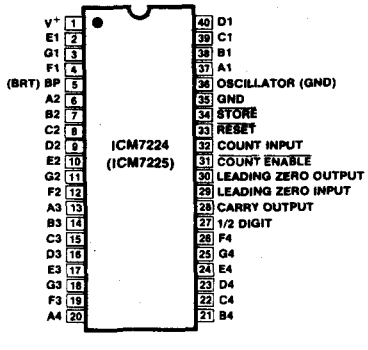
TYPICAL APPLICATION (UNIT COUNTER)



PIN CONFIGURATION

(OUTLINE DRAWING PL)



ORDERING INFORMATION

	ORDER PART NUMBER	COUNT OPTION
LCD DISPLAY	ICM7224 IPL	19999
	ICM7224A IPL	15959
LED DISPLAY	ICM7225 IPL	19999
	ICM7225A IPL	15959

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 70°C
Supply Voltage (V^+) 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, −0.3V
Operating Temperature Range ..... −20°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

OPERATING CHARACTERISTICS TABLE 2

(All Parameters measured with $V^+ = 5V$ unless otherwise indicated)

ICM7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	Test circuit, Display blank		10	50	μA
Operating supply voltage range	V^+		3	5	6	V
Oscillator input current	I_{OSCI}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		
Oscillator frequency	f_{osc}	Pin 36 Floating		16		KHz
Backplane frequency	f_{bp}	Pin 36 Floating		125		Hz

ICM7225 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (Brightness) at GROUND Pins 29, 31-34 at V^+		10	50	μA
Operating supply voltage range	V^+		4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment on current	I_{SEG}	Segment On, Vout = + 3V	5	8		mA
Half digit on current	I_H	Half digit on, Vout = + 3V	10	16		

FAMILY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Currents	I_P	Pins 29, 31, 33, 34 Vout = V^+ - 3V		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			1	
Count Input Threshold	V_{CT}			2		
Count Input Hysteresis	V_{CH}			0.5		
Output High Current	I_{OH}	Carry Pin 28 Leading Zero Out Pin 30 Vout = V^+ −3V	350	500		μA
Output Low Current	I_{OL}	Carry Pin 28 Leading Zero Out Pin 30 Vout = +3V	350	500		
Count Frequency	f_{count}	4.5V < V^+ < 6V	0	DC-25	15	MHz
$\overline{\text{Store}}$, $\overline{\text{Reset}}$ Minimum Pulse Width	t_S,t_R		3			μs

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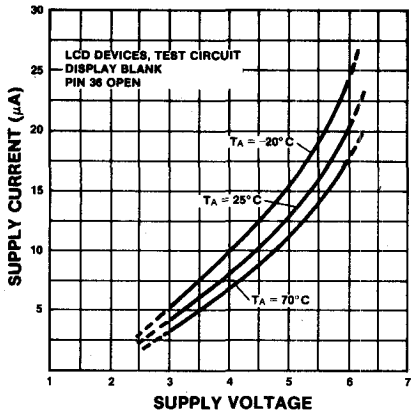
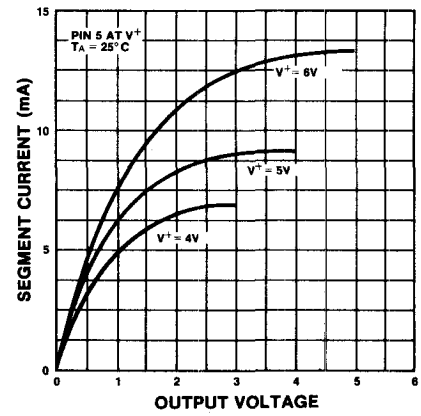
TYPICAL CHARACTERISTICS

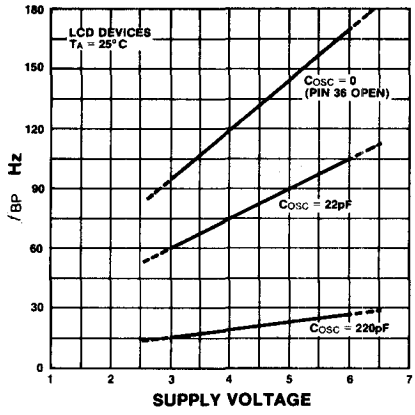
7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



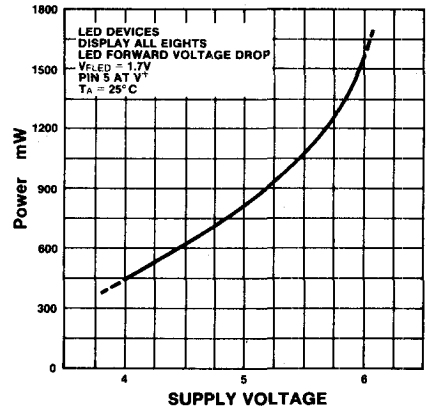
7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



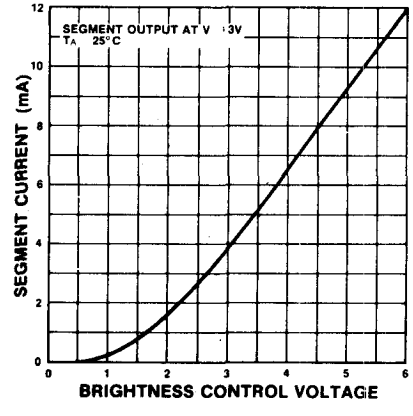
7224 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



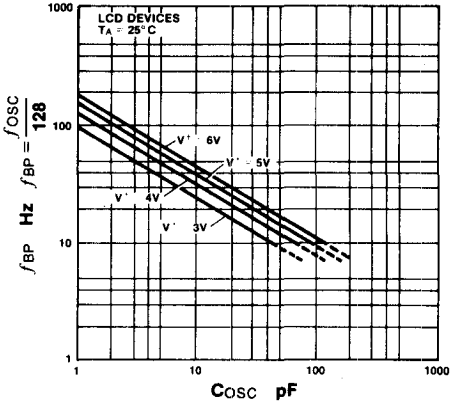
7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



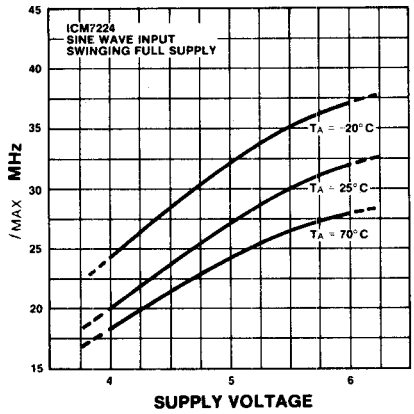
7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



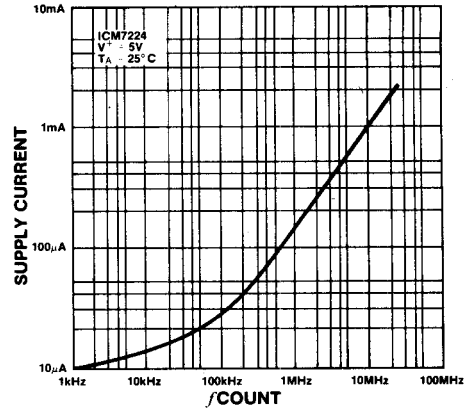
BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR COSC



MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE

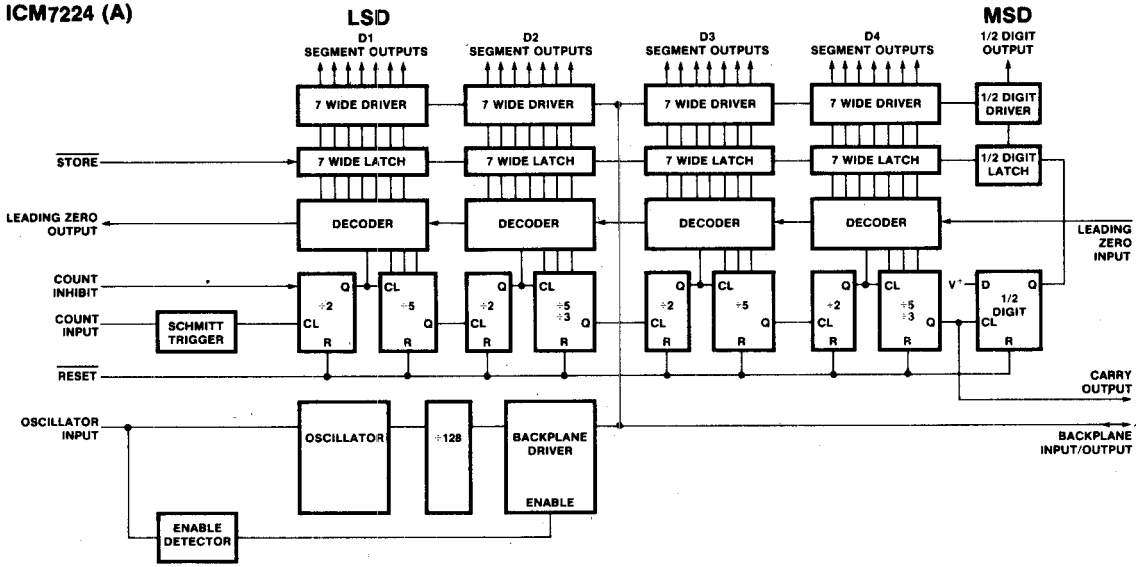


SUPPLY CURRENT AS A FUNCTION OF COUNT FREQUENCY

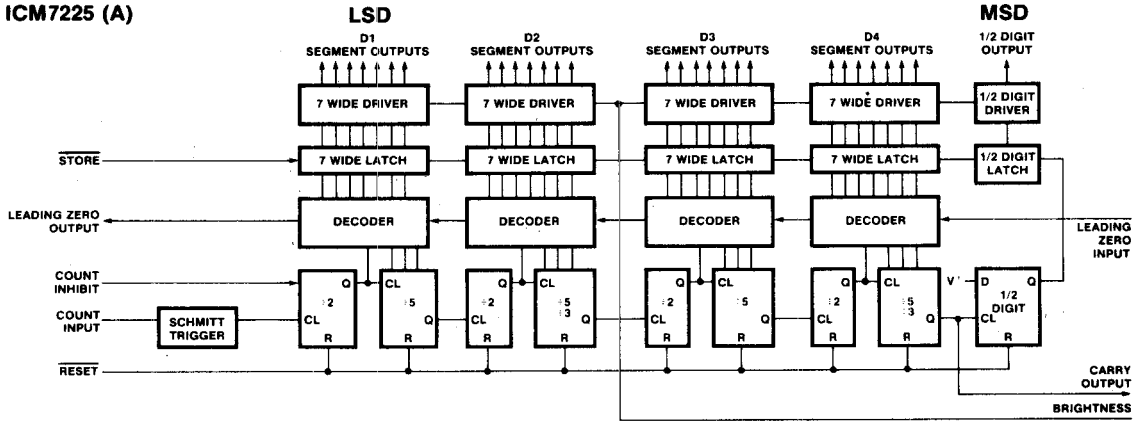


BLOCK DIAGRAMS

ICM7224 (A)



ICM7225 (A)



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CONTROL INPUT DEFINITIONS

In this table, V and GROUND are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	VOLTAGE	FUNCTION
LEADING ZERO INPUT	29	V^+ or Floating GROUND	Leading Zero Blanking Enabled Leading Zeroes Displayed
Count Inhibit	31	V^+ or Floating GROUND	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V^+ or Floating GROUND	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V^+ or Floating GROUND	Output Latches not Updated Output Latches Updated

DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional 4-1/2 digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

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The backplane output devices can be disabled by connecting the OSCILLATOR input (pin 36) to GROUND. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the OSCILLATOR terminal (pin 36); see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving 4-1/2 digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100kΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when at V^+, the display is fully on, and at GROUND, fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for GROUND; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED}) \times (I_{SEG}) \times (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

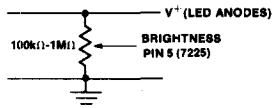


Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four digit ripple carry resetable counter, including a Schmitt trigger on the COUNT INPUT and a CARRY OUTPUT. Also included is an extra D-type flip-flop, clocked by the CARRY signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the COUNT INPUT, while the CARRY OUTPUT provides a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half digit is set, and subsequent CARRY outputs will not be affected.

A negative level at the $\overline{\text{COUNT ENABLE}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the count input, which prevents false counts that can result from using a normal logic gate to prevent counting.

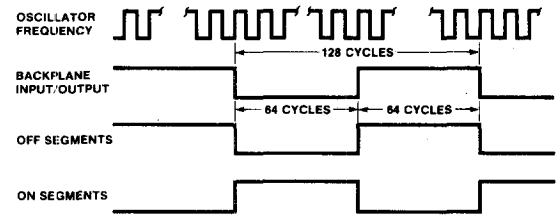
Each decade of counter drives directly into a four-to-seven decoder which develops the seven segment output code. The output data is latched at the driver; when the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the LEADING ZERO INPUT is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes; when low, or the half digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The LEADING ZERO OUTPUT is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the LEADING ZERO INPUT is at a positive level and the half digit is not set.

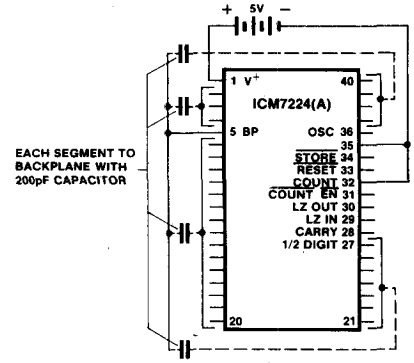
For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the LEADING ZERO OUTPUT of the high order digit device would be connected to the LEADING ZERO INPUT of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT ENABLE}}$, and LEADING ZERO INPUTS are provided with pullup devices, so that they may be left open when a positive level is desired. The CARRY and LEADING ZERO OUTPUTS are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 or ICM7225 devices in four digit blocks.

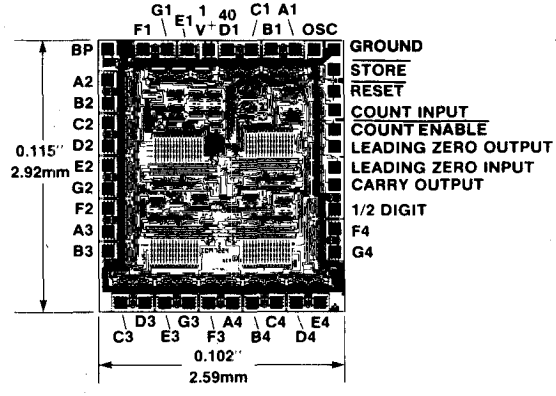
DISPLAY WAVEFORMS



TEST CIRCUIT

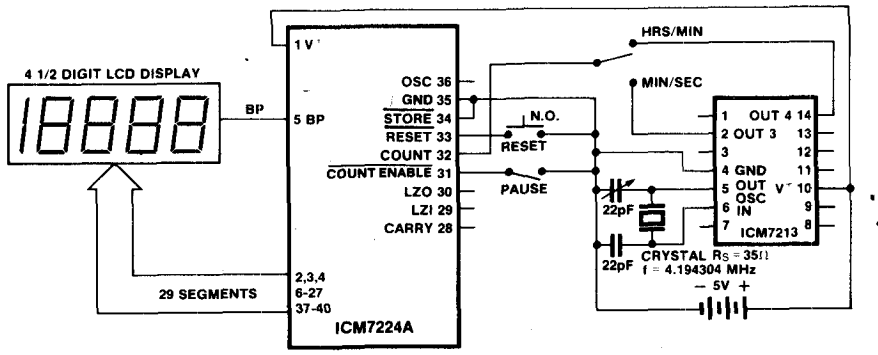


CHIP TOPOGRAPHY



APPLICATIONS

1. Two-Hour Precision Timer



2. Eight-Digit Precision Frequency Counter