

**1.5A LOW QUIESCENT CURRENT, FAST TRANSIENT
ULTRA-LOW DROPOUT LINEAR REGULATOR**
Description

The AP7363 is a 1.5A adjustable output voltage linear regulator with ultra-low dropout. The device includes pass element, error amplifier, band-gap, current limit and thermal shutdown circuitry.

The characteristics of low dropout voltage and fast transient response to step changes in load make it suitable for low voltage microprocessor applications. The typical quiescent current is approximately 0.5mA and changes little with load current. The built-in current-limit and thermal-shutdown functions prevent IC from damage in fault conditions.

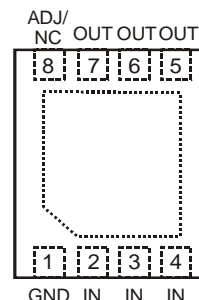
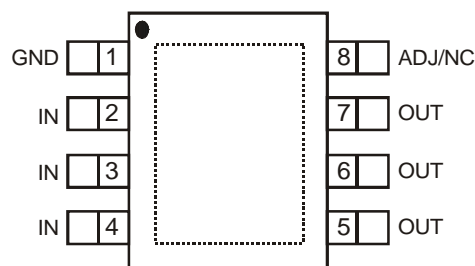
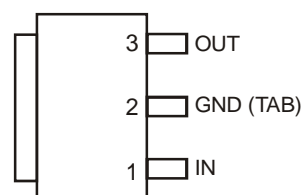
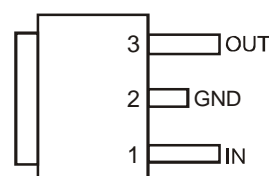
This device is available in U-DFN2030-8, SO-8EP, SOT223 and TO252 packages.

Features

- 1.5A ultra-low dropout linear regulator
- Ultra-low dropout: 190mV at 1.5A
- Stable with 10 μ F input/output capacitor, any types
- Wide input voltage range: 2.2V to 5.5V
- Adjustable output voltage: 0.6V to 5.0V
- Fixed output options: 1V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V
- Low ground pin current
- 25nA quiescent current in shutdown mode
- V_{ADJ} accuracy of $\pm 1.5\%$ @ +25°C
- V_{ADJ} accuracy of $\pm 3\%$ over line, load and temperature
- Excellent Load/Line Transient Response
- Current limit and thermal shutdown protection
- Ambient temperature range: -40°C to +85°C
- U-DFN2030-8, SO-8EP, SOT223 and TO252: Available in "Green" Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

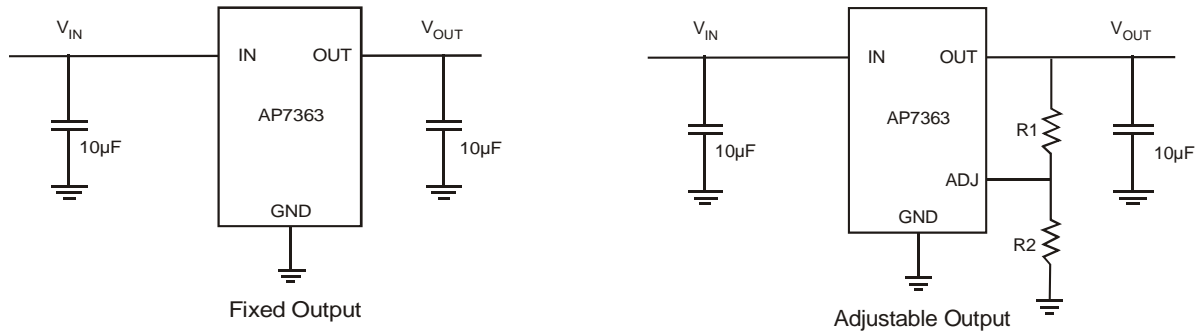
Applications

- ASIC power supplies in printers, graphics cards, DVD players, STBs, routers, etc
- FPGA and DSP core or I/O power supplies
- SMPS regulator
- Conversion from 3.3V or 5V rail

Pin Assignments
(Top View)

U-DFN2030-8
(Top View)

SO-8EP
(Top View)

**SOT223
(Fixed Output)**
(Top View)

TO252

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

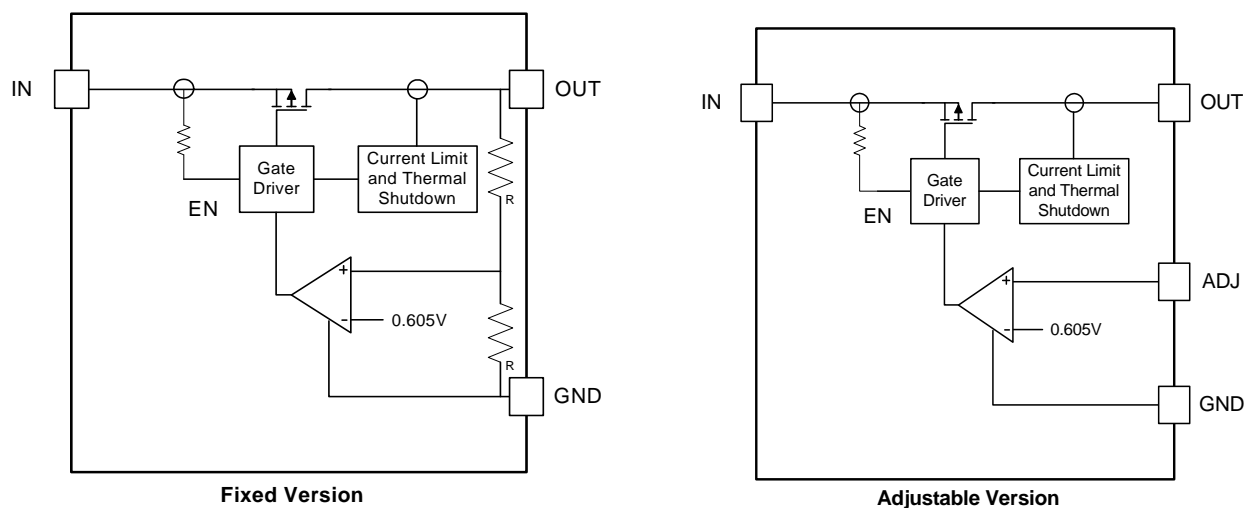


$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right) \text{ where } R_2 \leq 10k\Omega$$

Pin Descriptions

Pin Name	Pin Number		Function
	SOT223 TO252	U-DFN2030-8 SO-8EP	
GND	2	1	Ground.
IN	1	2, 3, 4	Voltage input pin.
OUT	3	5, 6, 7	Voltage output pin.
ADJ	NA	8	Output feedback pin for adjustable version only – a resistor divider from this pin to the OUT pin and ground sets the output voltage.
NC	NA	8	No connection for fixed output version.
EP/TAB	—	—	The exposed pad (EP) is used to remove heat from the package and it is recommended that it is connected to a copper area. The die is electrically connected to the exposed pad. It is recommended to connect it externally to GND, but should not be the only ground connection.

Functional Block Diagram



Absolute Maximum Ratings (cont.) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	2000	V
ESD MM	Machine Model ESD Protection	200	V
V _{IN}	Input Voltage	-0.3 to +6.0	V
V _{OUT}	OUT Voltage	-0.3 to V _{IN} +0.3	V
I _{OUT}	Continuous Load Current	Internal Limited	
T _{ST}	Storage Temperature Range	-65 to +150	°C
T _J	Maximum Junction Temperature	150	°C

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V _{IN}	Input voltage	2.2	5.5	V
I _{OUT}	Output Current	0	1.5	A
T _A	Operating Ambient Temperature	-40	+85	°C
T _J	Operating Junction Temperature (Note 5)	-40	+125	°C

- Notes:
- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated are not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
 - Operating junction temperature must be evaluated and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature (T_{J-MAX}), and package thermal resistance (θ_{JA}).

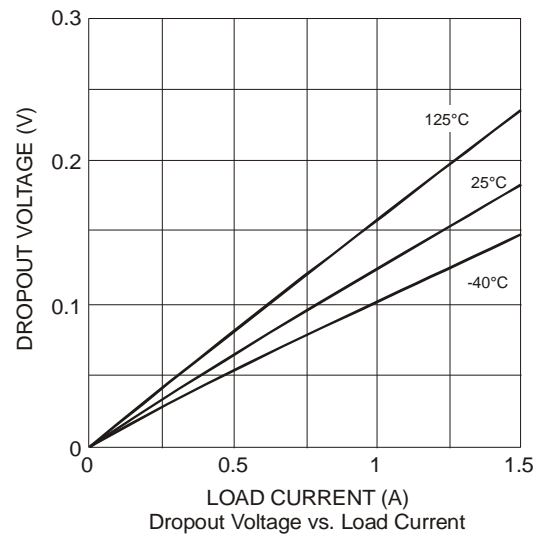
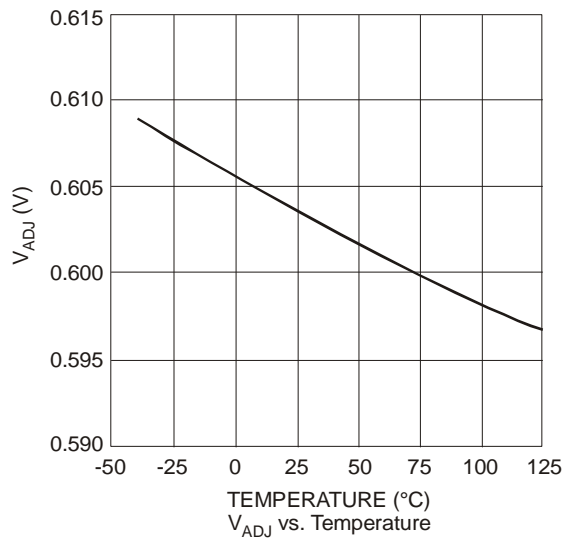
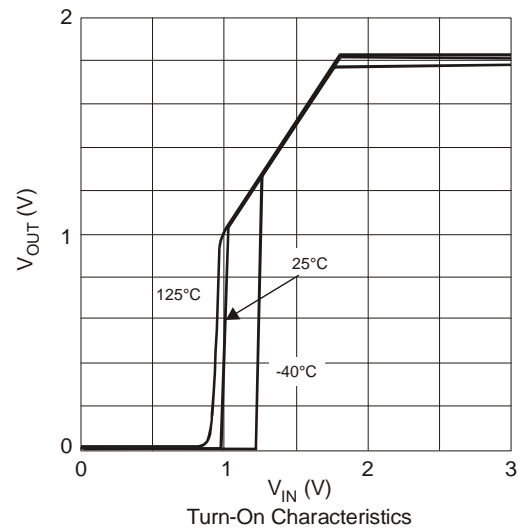
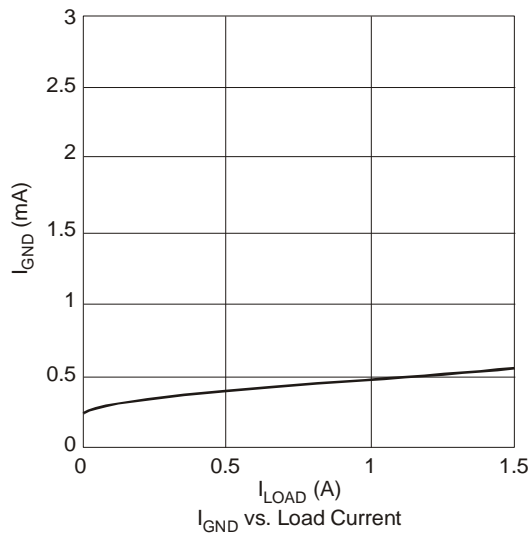
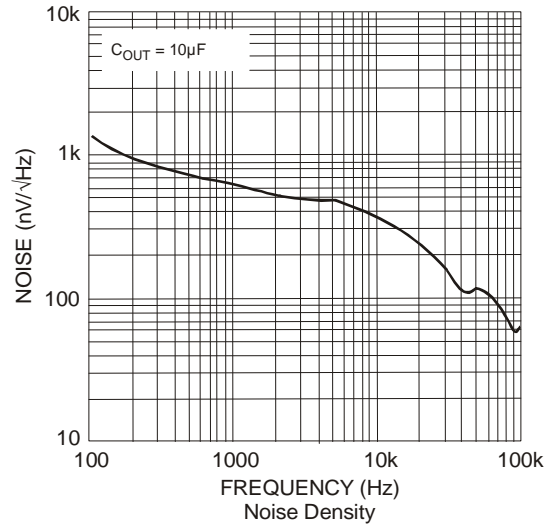
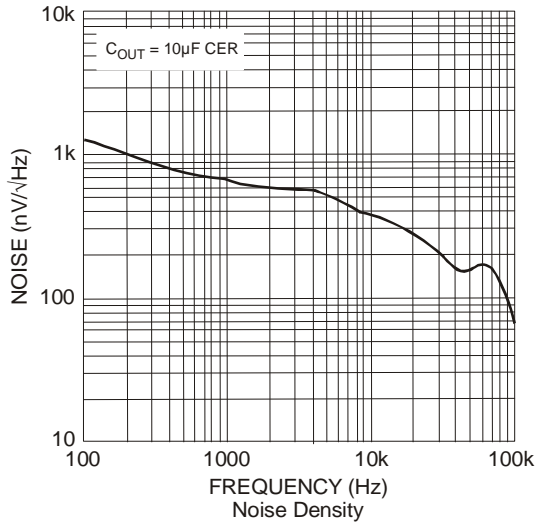
Electrical Characteristics (@T_A = +25°C, V_{IN} = 3.3V, I_{OUT} = 10mA, C_{IN} = 10μF, C_{OUT} = 10μF, unless otherwise specified.)

Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = +25°C, and are provided for reference purposes only.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V _{ADJ}	ADJ Pin Voltage	V _{IN} = V _{IN-MIN} to V _{IN-MAX} , I _{OUT} = 10mA to 1.5A	T _A = +25°C Over temp	0.584 0.575	0.605	0.626 0.635	V
I _{ADJ}	ADJ Pin Bias Current	V _{IN} = V _{IN-MIN} to V _{IN-MAX}	T _A = +25°C Over temp		50	750	nA
V _{DROPOUT}	Dropout Voltage (Note 6)	I _{OUT} = 1.5A, V _{OUT} = 2.5V	T _A = +25°C Over temp		190	240 280	mV
ΔV _{OUT} /ΔV _{IN}	Line Regulation (Note 7)	V _{IN} = V _{IN-MIN} to V _{IN-MAX}	T _A = +25°C Over temp	—	0.04 0.05	—	%/V
ΔV _{OUT} /ΔI _{OUT}	Load Regulation (Note 7)	I _{OUT} = 10mA to 1.5A	T _A = +25°C Over temp	—	0.18 0.33	—	%/A
I _{GND}	Ground Pin Current in Normal Operation Mode	I _{OUT} = 10mA to 1.5A	T _A = +25°C Over temp		1.0	1.2 1.3	mA
I _{OUT-PK}	Peak Output Current	V _{OUT} ≥ V _{OUT} - NOM -5%			3.6		A
I _{SC}	Short Circuit Current	OUT grounded	T _A = +25°C Over temp		3.7 2		A
t _{d(off)}	Turn-Off Delay	From V _{EN} < V _{IL} to V _{OUT} = OFF, I _{OUT} = 1.5A			25		μs
t _{d(on)}	Turn-On Delay	From V _{EN} > V _{IH} to V _{OUT} = ON, I _{OUT} = 1.5A			25		μs
PSRR	Ripple Rejection	V _{IN} = 3.0V, I _{OUT} = 1.5A, f = 120Hz V _{IN} = 3.0V, I _{OUT} = 1.5A, f = 1kHz			65 61		dB
ρ _{n(lf)}	Output Noise Density	F = 120Hz, C _{OUT} = 10μF ceramic			1.0		μV/√Hz
e _n	Output Noise Voltage	BW = 100Hz – 100kHz, C _{OUT} = 10μF ceramic			100		μV(rms)
T _{SHDN}	Thermal Shutdown Threshold	T _J rising			170		°C
T _{HYS}	Thermal Shutdown Hysteresis	T _J falling from T _{SHDN}			10		
θ _{JA}	Thermal Resistance Junction-to-Ambient	U-DFN2030-8 (Note 8)			174.0		°C/W
		SO-8EP (Note 8)			52.8		
		SOT223 (Note 8)			105.7		
		TO252 (Note 8)			87.8		
θ _{JC}	Thermal Resistance Junction-to-Case	U-DFN2030-8 (Note 8)			28.2		°C/W
		SO-8EP (Note 8)			10.0		
		SOT223 (Note 8)			18.5		
		TO252 (Note8)			17.3		

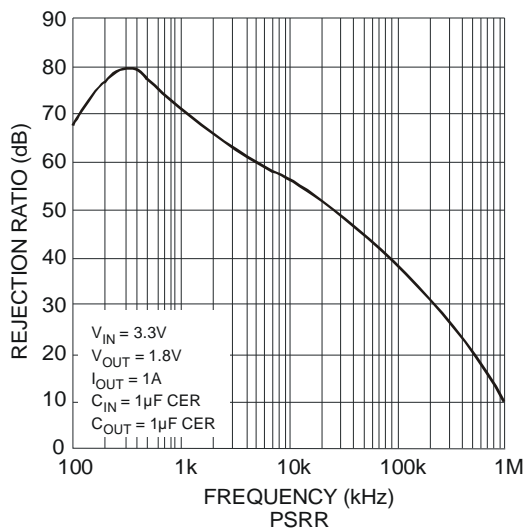
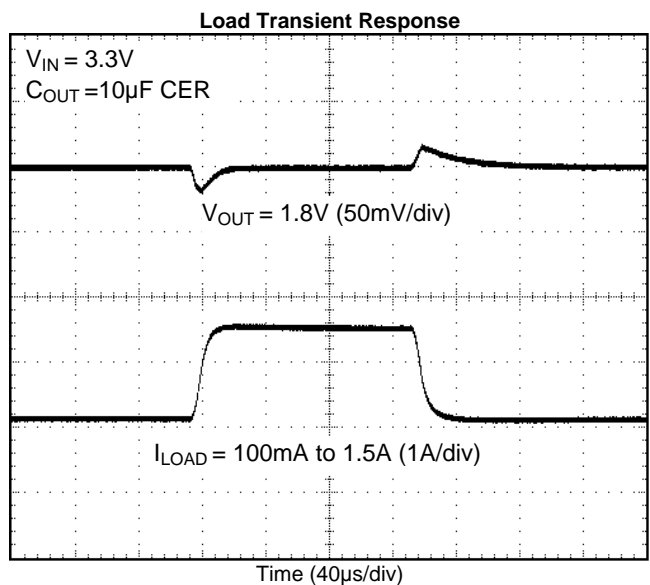
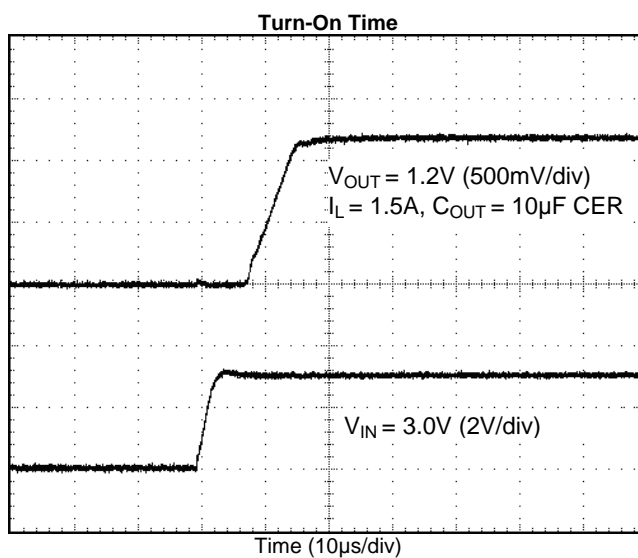
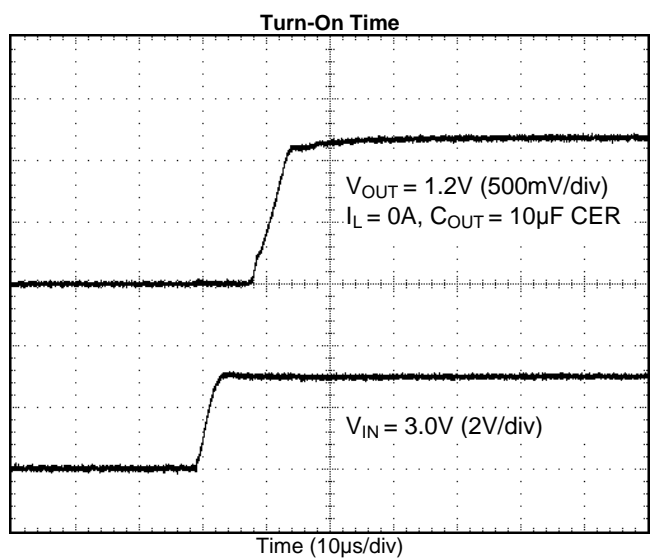
- Notes:
- Dropout voltage is the minimum voltage difference between the input and the output at which the output voltage drops 2% below its nominal value. For any output voltage less than 2.5V, the minimum V_{IN} operating voltage is the limiting factor.
 - The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the adjust voltage tolerance specification.
 - Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper with minimum recommended pad layout.

Typical Performance Characteristics (@ $T_J = +25^\circ\text{C}$, $V_{IN} = 2.7\text{V}$, $C_{IN} = 10\mu\text{F}$, $C_{OUT} = 10\mu\text{F}$, $I_{OUT} = 10\text{mA}$, $V_{OUT} = 1.8\text{V}$.)



Typical Performance Characteristics (cont.)

(@T_J = +25°C, V_{IN} = 2.7V, C_{IN} = 10μF, C_{OUT} = 10μF, I_{OUT} = 10mA, V_{OUT} = 1.8V.)



Application Note

Input Capacitor

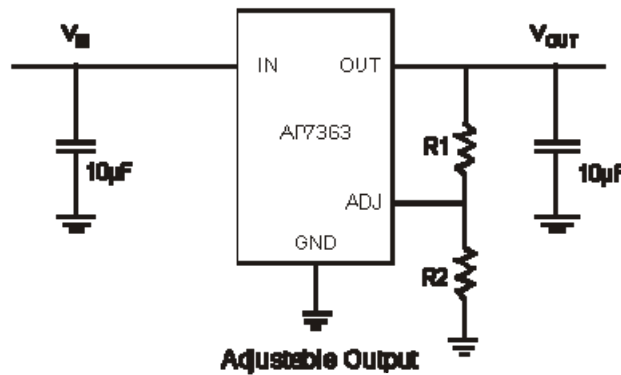
A minimum 2.2μF ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. Larger input capacitor like 10μF will provide better load transient response. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

Output Capacitor

The output capacitor is required to stabilize and help the transient response of the LDO. The AP7363 is stable with any type of capacitor, with no limitations on minimum or maximum ESR. The device is designed to have excellent transient response for most applications with a small amount of output capacitance. The device is also stable with multiple capacitors in parallel, which can be of any type of value. Additional capacitance helps to reduce undershoot and overshoot during transient loads. This capacitor should be placed as close as possible to OUT and GND pins for optimum performance.

Adjustable Operation

The AP7363 provides output voltage from 0.6V to 5.0V through external resistor divider as shown below.



The output voltage is calculated by:

$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right)$$

Where $V_{REF} = 0.6V$ (the internal reference voltage)

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

To maintain the stability of the internal reference voltage, R_2 need to be kept smaller than 10kΩ.

No Load Stability

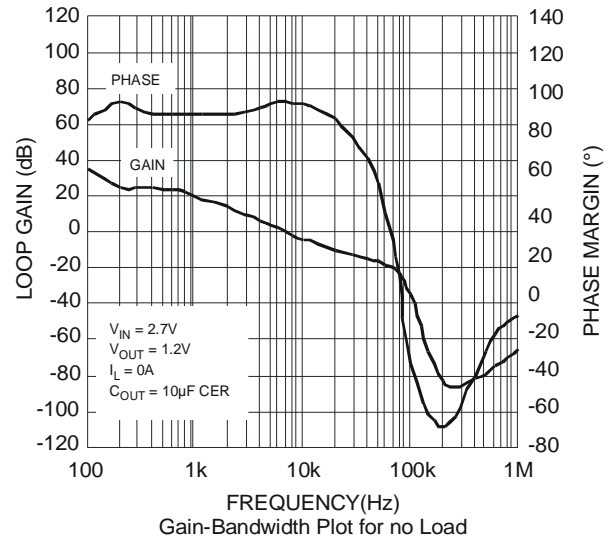
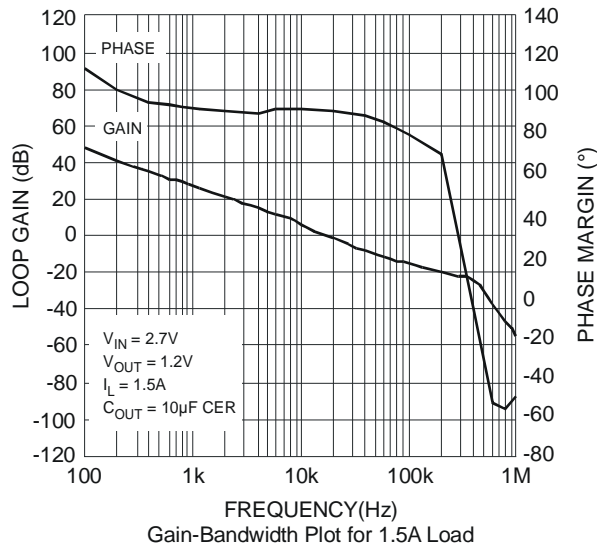
Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

Application Note (cont.)

Stability and Phase Margin

Any regulator which operates using a feedback loop must be compensated in such a way as to ensure adequate phase margin, which is defined as the difference between the phase shift and -180 degrees at the frequency where the loop gain crosses unity (0 dB). For most LDO regulators, the ESR of the output capacitor is required to create a zero to add enough phase lead to ensure stable operation. The AP7363 has an internal compensation circuit which maintains phase margin regardless of the ESR of the output capacitor, any type of capacitor can be used.

The two charts on the next page show the gain/phase plot of the AP7363 with an output of 1.2V, 10 μ F ceramic output capacitor, delivering 1.5A load current and no load. It can be seen the phase margin is about 90° (which is very stable).



Short Circuit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool down. When the junction temperature reduces to approximately +160°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Low Quiescent Current

The AP7363, consuming only around 0.5mA for all input range, provides great power saving in portable and low power applications.

Output Noise

This is the integrated value of the output noise over a specified frequency range. Input voltage and output load current are kept constant during the measurement. Results are expressed in μV_{rms} or $\mu V/\sqrt{Hz}$.

The AP7363 is a low noise regulator and needs no external noise reduction capacitor. Output voltage noise is typically 100 μV_{rms} overall noise level between 100 Hz and 100 kHz.

Noise is specified in two ways:

Output noise density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Output noise voltage is the RMS sum of spot noise over a specified bandwidth. Spot noise is measured in units $\mu V/\sqrt{Hz}$ or nV/\sqrt{Hz} and total output noise is measured in $\mu V_{(rms)}$. The primary source of noise in low-dropout regulators is the internal reference.

Application Note (cont.)

Power Dissipation

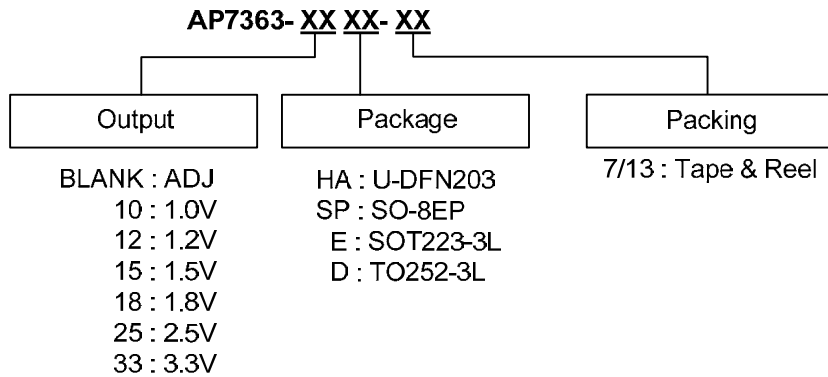
The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the junction to ambient thermal resistance, and maximum ambient temperature, which can be calculated by the equation in the following:

$$P_{D_max} = \frac{(+150^{\circ}\text{C} - T_A)}{R_{\theta JA}}$$

Ordering Information



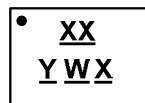
Part Number	Package Code	Packaging (Note 9)	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP7363-XXHA-7	HA	U-DFN2030-8	3000/Tape & Reel	-7
AP7363-XXSP-13	SP	SO-8EP	2500/Tape & Reel	-13
AP7363-XXE-13	E	SOT223-3L	2500/Tape & Reel	-13
AP7363-XXD-13	D	TO252-3L	2500/Tape & Reel	-13

Note: 9. TO252 and SOT223 are only available with fixed output version.

Marking Information

(1) U-DFN2030-8

(Top View)

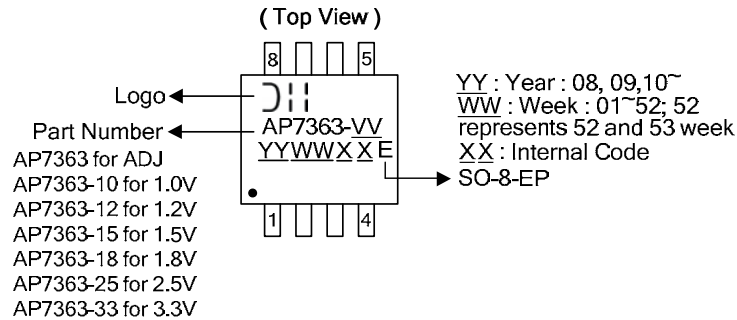


XX : Identification Code
 Y : Year : 0~9
 W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
 X : Internal Code

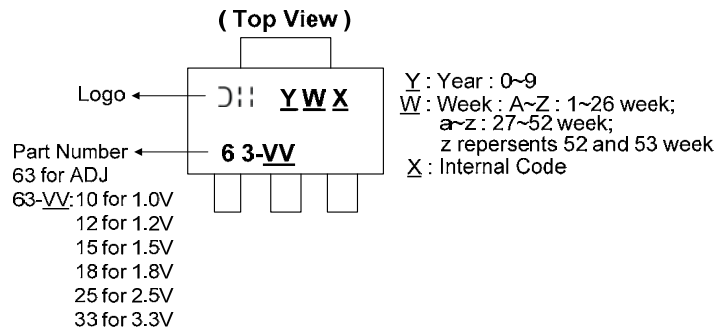
Device	Package	Identification Code
AP7363ADJ	U-DFN2030-8	SA
AP7363-10	U-DFN2030-8	SB
AP7363-12	U-DFN2030-8	SC
AP7363-15	U-DFN2030-8	SD
AP7363-18	U-DFN2030-8	SE
AP7363-25	U-DFN2030-8	SF
AP7363-33	U-DFN2030-8	SG

Marking Information (cont.)

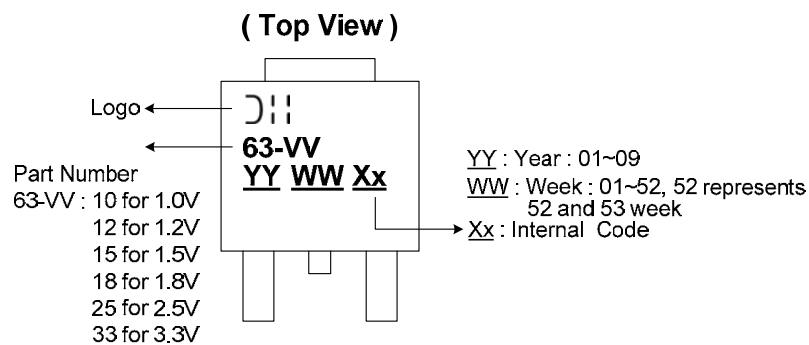
(2) SO-8EP



(3) SOT223



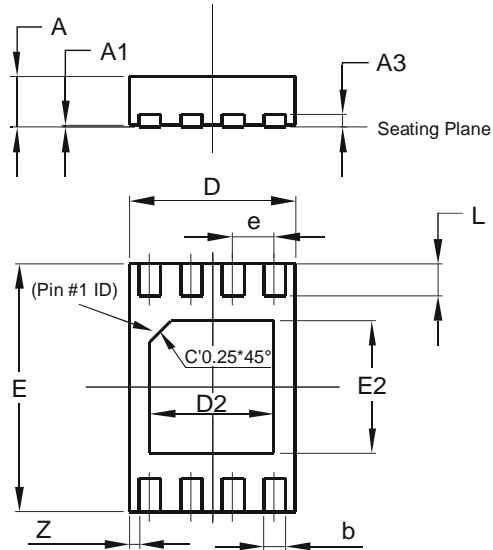
(4) TO252



Package Outline Dimensions (All dimensions in mm.)

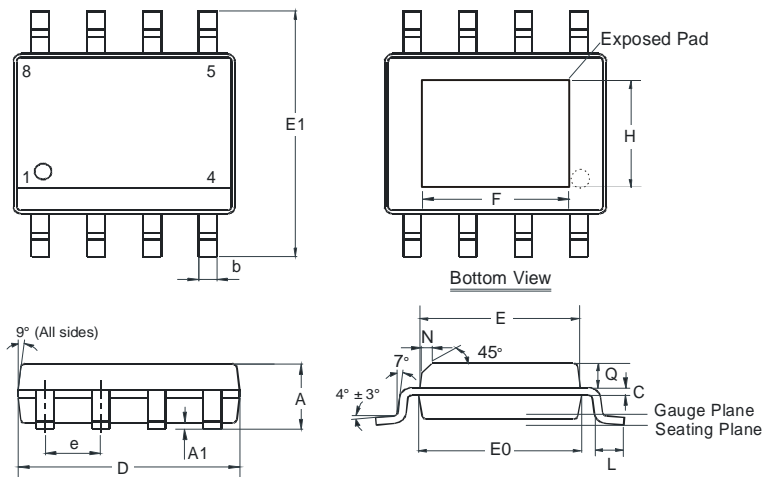
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

(1) U-DFN2030-8



U-DFN2030-8			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	1.95	2.05	2.00
D2	1.40	1.60	1.50
e	-	-	0.50
E	2.95	3.05	3.00
E2	1.50	1.70	1.60
L	0.35	0.45	0.40
Z	-	-	0.125
All Dimensions in mm			

(2) SO-8EP

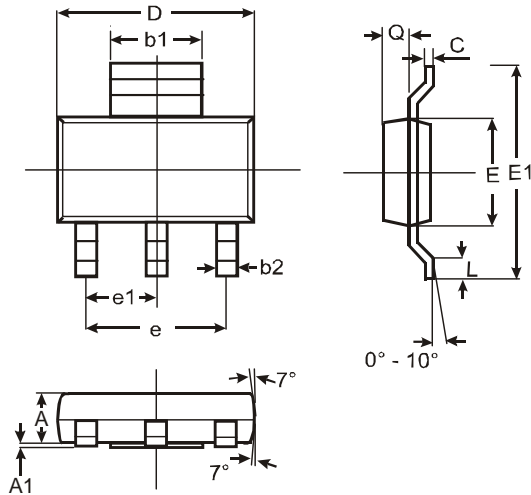


SO-8EP (SOP-8L-EP)			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Package Outline Dimensions (cont.) (All dimensions in mm.)

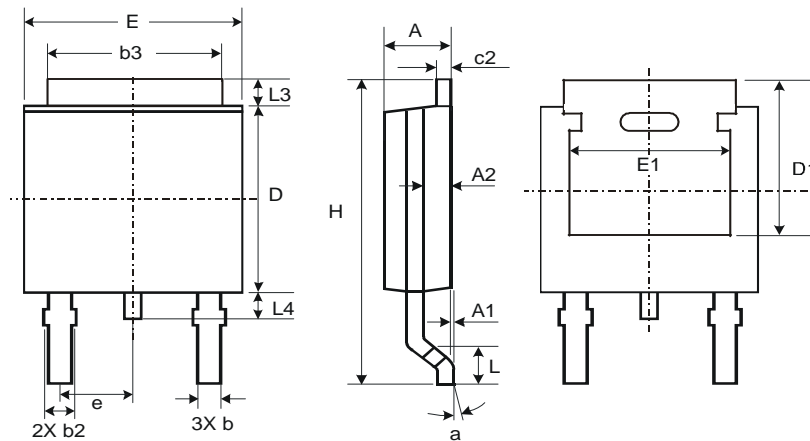
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

(3) SOT223



SOT223			
Dim	Min	Max	Typ
A	1.55	1.65	1.60
A1	0.010	0.15	0.05
b1	2.90	3.10	3.00
b2	0.60	0.80	0.70
C	0.20	0.30	0.25
D	6.45	6.55	6.50
E	3.45	3.55	3.50
E1	6.90	7.10	7.00
e	—	—	4.60
e1	—	—	2.30
L	0.85	1.05	0.95
Q	0.84	0.94	0.89
All Dimensions in mm			

(4) TO252

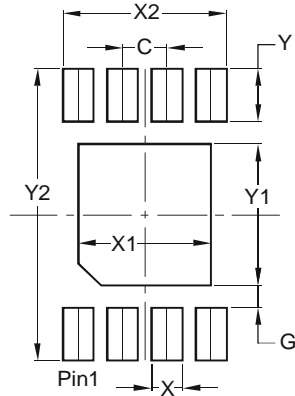


TO252			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	—	—
e	—	—	2.286
E	6.45	6.70	6.58
E1	4.32	—	—
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	—
All Dimensions in mm			

Suggested Pad Layout

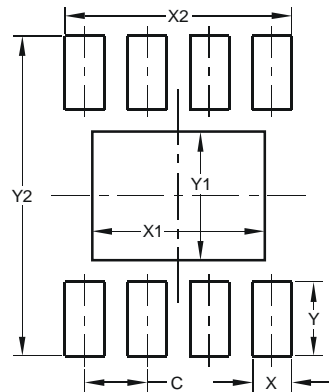
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(1) U-DFN2030-8



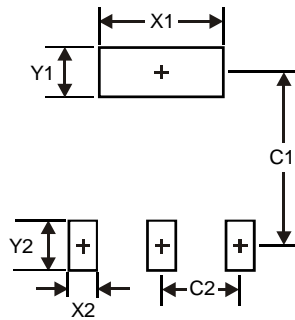
Dimensions	Value (in mm)
C	0.500
G	0.250
X	0.350
X1	1.500
X2	1.850
Y	0.600
Y1	1.600
Y2	3.300

(2) SO-8EP



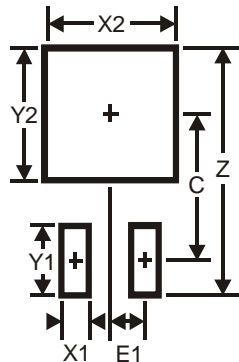
Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

(3) SOT223



Dimensions	Value (in mm)
X1	3.3
X2	1.2
Y1	1.6
Y2	1.6
C1	6.4
C2	2.3

(4) TO252



Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
C	6.9
E1	2.3

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