



STB7NB40

N-CHANNEL 400V - 0.75 Ω - 7.0A D²PAK

PowerMESH™ MOSFET

PRELIMINARY DATA

Table 1. General Features

Type	V _{DSS}	R _{DS(on)}	I _D
STB7NB40	400 V	< 0.9 Ω	7.0 A

FEATURES SUMMARY

- TYPICAL R_{DS(on)} = 0.75 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

DESCRIPTION

Using the latest high voltage technology, STMicroelectronics has designed an advanced family of power Mosfets with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

Figure 1. Package

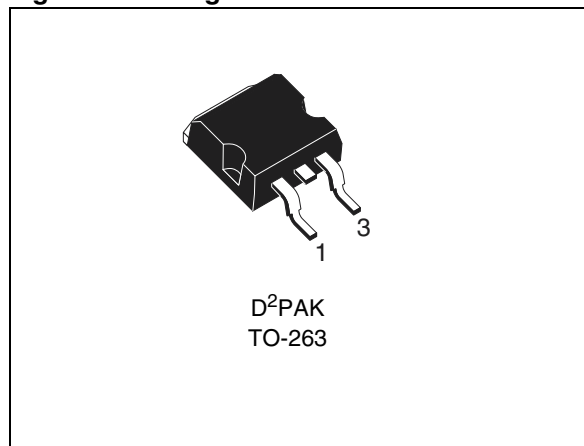


Figure 2. Internal Schematic Diagram

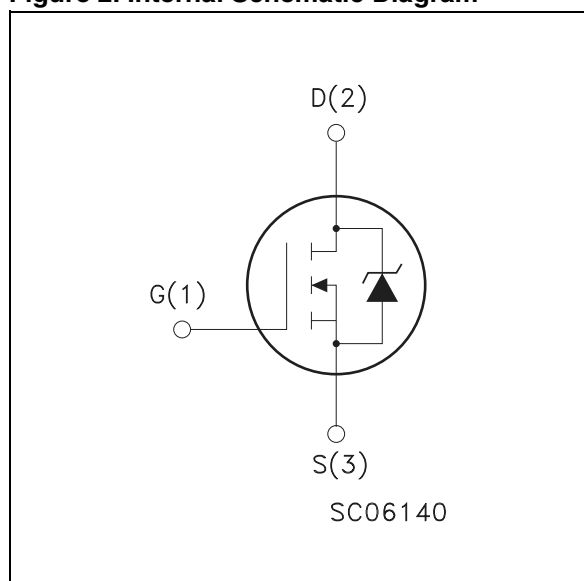


Table 2. Order Codes

Part Number	Marking	Package	Packaging
STB7NB40T4	B7NB40	D ² PAK	TAPE & REEL

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	400	V
V_{DGR}	Drain- gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	400	V
V_{GS}	Gate-source Voltage	± 30	V
I_D	Drain Current (cont.) at $T_C = 25\text{ }^\circ\text{C}$	7	A
I_D	Drain Current (cont.) at $T_C = 100\text{ }^\circ\text{C}$	4.4	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	28	A
P_{tot}	Total Dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
	Derating Factor	0.8	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak Diode Recovery voltage slope	4.5	V/ns
T_{stg}	Storage Temperature	-65 to 150	$^\circ\text{C}$
T_j	Max. Operating Junction Temperature	150	$^\circ\text{C}$

Note: 1. Pulse width limited by safe operating area

2. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$ **Table 4. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	1.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

Table 5. Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	7	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\text{ }^\circ\text{C}$; $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	300	mJ

ELECTRICAL CHARACTERISTICS ($T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified)**Table 6. Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$; $V_{\text{GS}} = 0$	400			V
I_{DSS}	Zero Gate Voltage	$V_{\text{DS}} = \text{Max Rating}$			1	μA
	Drain Current ($V_{\text{GS}} = 0$)	$V_{\text{DS}} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			50	μA
I_{GSS}	Gate-body Leakage Current ($V_{\text{DS}} = 0$)	$V_{\text{GS}} = \pm 30\ \text{V}$			± 100	nA

Table 7. On ⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$; $I_D = 250\ \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static Drain-source On Resistance	$V_{\text{GS}} = 10\text{V}$; $I_D = 3.5\ \text{A}$		0.75	0.9	Ω

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %**Table 8. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{\text{fs}}^{(1)}$	Forward Transconductance	$V_{\text{DS}} > I_{\text{D(on)}} \times R_{\text{DS(on)max}}$; $I_D = 3.5\ \text{A}$	2.5	4.2		S
C_{iSS}	Input Capacitance	$V_{\text{DS}} = 25\ \text{V}$; $f = 1\ \text{MHz}$; $V_{\text{GS}} = 0$		705	720	pF
C_{oSS}	Output Capacitance			132	175	pF
C_{rSS}	Reverse Transfer Capacitance			17	25	pF

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %**Table 9. Switching On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on Time	$V_{\text{DD}} = 200\ \text{V}$; $I_D = 3.5\ \text{A}$; $R_G = 4.7\ \Omega$		11.5	16	ns
t_r	Rise Time	$V_{\text{GS}} = 10\ \text{V}$ (see test circuit, Figure 5)		7.5	11	ns
Q_g	Total Gate Charge	$V_{\text{DD}} = 320\ \text{V}$; $I_D = 7\ \text{A}$; $V_{\text{GS}} = 10\ \text{V}$		21	30	nC
Q_{gs}	Gate-Source Charge			7.3		nC
Q_{gd}	Gate-Drain Charge			8.5		nC

Table 10. Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{r(Voff)}}$	Off-voltage Rise Time	$V_{\text{DD}} = 320\ \text{V}$; $I_D = 7\ \text{A}$; $R_G = 4.7\ \Omega$		9.5	15	ns
t_f	Fall Time	$V_{\text{GS}} = 10\ \text{V}$ (see test circuit, Figure 7)		9	14	ns
t_c	Cross-over Time			16.5	25	ns

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				7	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				28	A
$V_{SD}^{(2)}$	Forward On Voltage	$I_{SD} = 7\text{ A}$; $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 7\text{ A}$; $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$; $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, Figure 7)		300		ns
Q_{rr}	Reverse RecoveryCharge			2		μC
I_{RRAM}	Reverse RecoveryCharge			13.7		A

Note: 1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Figure 3. Unclamped Inductive Load Test Circuit

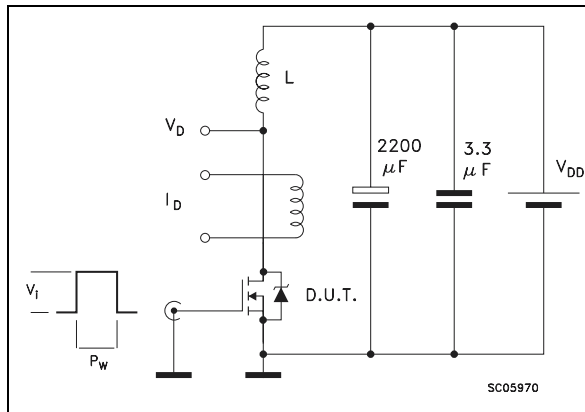


Figure 4. Unclamped Inductive Waveforms

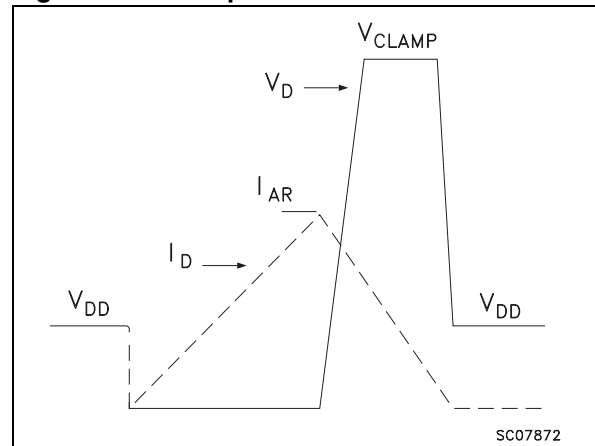


Figure 5. Switching Times Test Circuits For Resistive Load

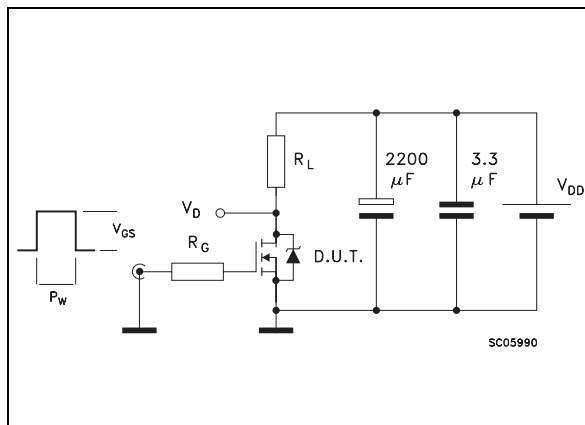


Figure 6. Gate Charge Test Circuit

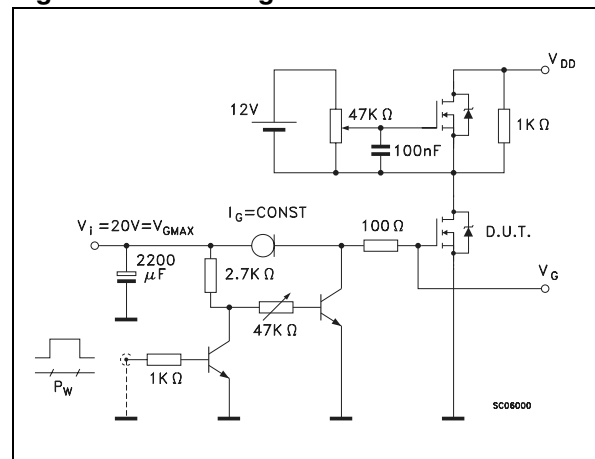
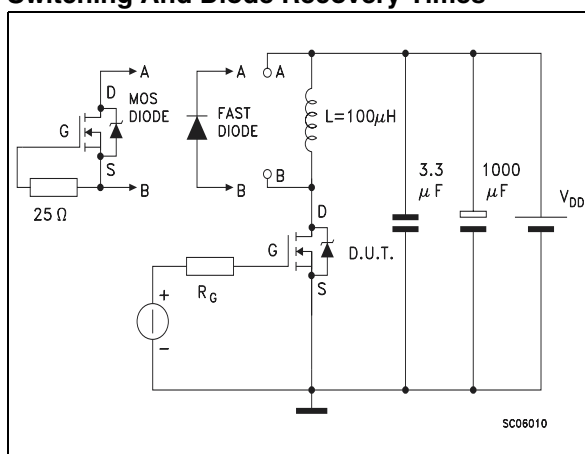


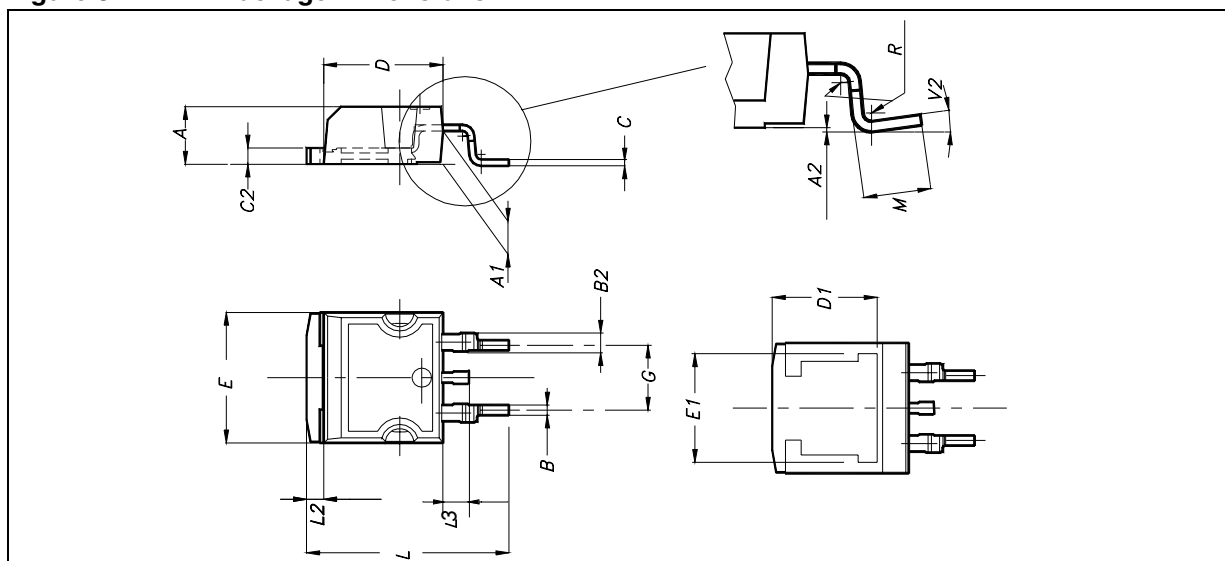
Figure 7. Test Circuit For Inductive Load Switching And Diode Recovery Times



PACKAGE MECHANICAL

Table 12. D²PAK Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

Figure 8. D²PAK Package Dimensions

Note: Drawing is not to scale.

REVISION HISTORY**Table 13. Revision History**

Date	Revision	Description of Changes
October-1997	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.

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