



Low-Voltage Single SPDT MICRO FOOT™ Analog Switch

FEATURES

- MICRO FOOT Chip Scale Package (1.07 x 1.57 mm)
- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 1.4 Ω
- Fast Switching - t_{ON} : 24 ns, t_{OFF} : 9 ns
- Low Power Consumption
- TTL/CMOS Compatible

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- PCM Cards
- PDA

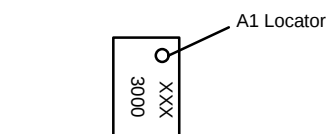
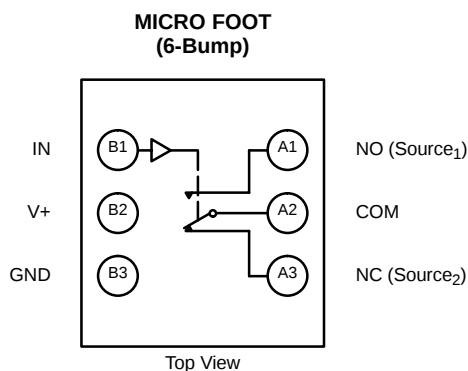
DESCRIPTION

The DG3000 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 24 ns, t_{OFF} : 9 ns), low on-resistance ($r_{DS(on)}$: 1.4 Ω) and small physical size (MICRO FOOT, 6-bump), the DG3000 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG3000 is built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG3000.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: 3000
xxx = Date/Lot Traceability Code

TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	MICRO FOOT: 6-Bump (2 x 3, 0.5-mm Pitch)	DG3000DB



ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +6 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	± 50 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	± 200 mA
Storage Temperature (D Suffix)	-65 to 150°C
Package Reflow Conditions ^b	
VPR	215°C
IR/Convection	220°C

Power Dissipation (Packages)^c6-Bump, 2 x 3 MICRO FOOT^d 250 mW

Notes:

- a Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b Refer to IPC/JEDEC (J-STD-020A). No hand/manual solder rework recommended
c All bumps soldered to PC Board.
d Derate 6.5 mW/°C above 25°C

SPECIFICATIONS (V+ = 2.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, ±10%, VIN = 0.4 or 1.6 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance	rON	V+ = 1.8 V, VCOM = 1.0 V, INO, INC = 10 mA	Room Full ^d		17	20 22.5	Ω
rON Flatness ^d	rON Flatness	V+ = 1.8 V, VCOM = 0 to V+, INO, INC = 10 mA	Room		14		
Switch Off Leakage Current ^f	INO(off), INC(off)	V+ = 2.2 V VNO, VNC = 0.5 V/1.5 V, VCOM = 1.5 V/0.5 V	Room Full ^d	-700 -11		700 11	pA nA
	ICOM(off)		Room Full ^d	-700 -11		700 11	pA nA
Channel-On Leakage Current ^f	ICOM(on)	V+ = 2.2 V, VNO, VNC = VCOM = 0.5 V/1.5 V	Room Full ^d	-700 -11		700 11	pA nA
Digital Control							
Input High Voltage	VINH		Full	1.6			V
Input Low Voltage	VINL		Full			0.4	
Input Capacitance ^d	Cin		Full		5		pF
Input Current ^d	IINL or IINH	VIN = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time	tON	VNO or VNC = 1.5 V, RL = 300 Ω, CL = 35 pF Figures 1 and 2	Room Full ^d		61	76 79	ns
Turn-Off Time	tOFF		Room Full ^d		17	33 36	
Break-Before-Make Time	t _d		Room	1	45		
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω, Figure 3	Room		2		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		-61		dB
Crosstalk ^d	XTALK		Room		-67		
NO, NC Off Capacitance ^d	CNO(off), CNC(off)	VIN = 0 or V+, f = 1 MHz	Room		31		pF
Channel-On Capacitance ^d	CON		Room		98		
Power Supply							
Power Supply Range	V+			1.8		2.2	V
Power Supply Current ^d	I+	VIN = 0 or V+			0.1	1.0	μA
Power Consumption	PC					2.2	μW



SPECIFICATIONS (V+ = 3.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance ^d	rON	V+ = 2.7 V, VCOM = 1.5 V, INO, INC = 10 mA	Room Full		3.3 3.4	4.1 4.2	Ω
rON Flatness ^d	rON Flatness	V+ = 2.7 V, VCOM = 0 to V+, INO, INC = 10 mA	Room		1.3		
Switch Off Leakage Current ^f	INO(off), INC(off)	V+ = 3.3 V VNO, VNC = 1 V/3 V, VCOM = 3 V/1 V	Room Full	-800 -13		800 13	pA nA
	ICOM(off)		Room Full	-800 -13		800 13	pA nA
Channel-On Leakage Current ^f	ICOM(on)	V+ = 3.3 V, VNO, VNC = VCOM = 1 V/3 V	Room Full	-800 -13		800 13	pA nA
Digital Control							
Input High Voltage	VINH		Full	2			V
Input Low Voltage	VINL		Full			0.4	
Input Capacitance ^d	Cin		Full		5		pF
Input Current ^d	INIL or IINH	VIN = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	tON	VNO or VNC = 2.0 V, RL = 300 Ω, CL = 35 pF Figure 1 and 2	Room Full		34	49 52	ns
Turn-Off Time ^d	tOFF		Room Full		12	30 33	
Break-Before-Make Time ^d	td		Room	1	23		
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω, Figure 3	Room		4		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		-61		dB
Crosstalk ^d	XTALK		Room		-67		
NO, NC Off Capacitance ^d	CNO(off), CNC(off)	VIN = 0 or V+, f = 1 MHz	Room		31		pF
Channel-On Capacitance ^d	CON		Room		47		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current ^d	I+	VIN = 0 or V+			0.1	1.0	μA
Power Consumption	PC					3.3	μW

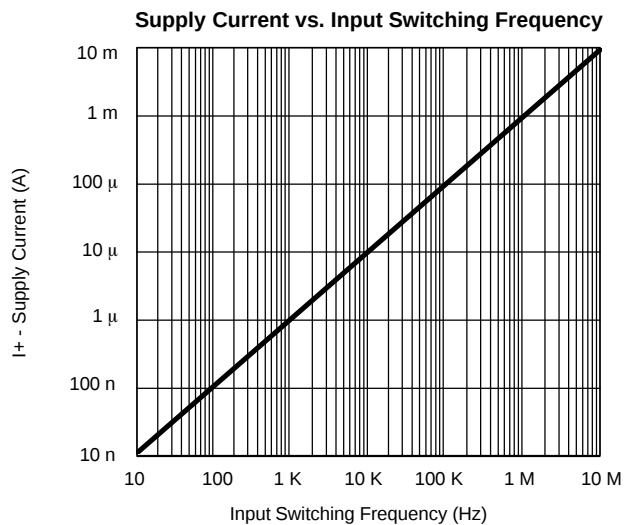
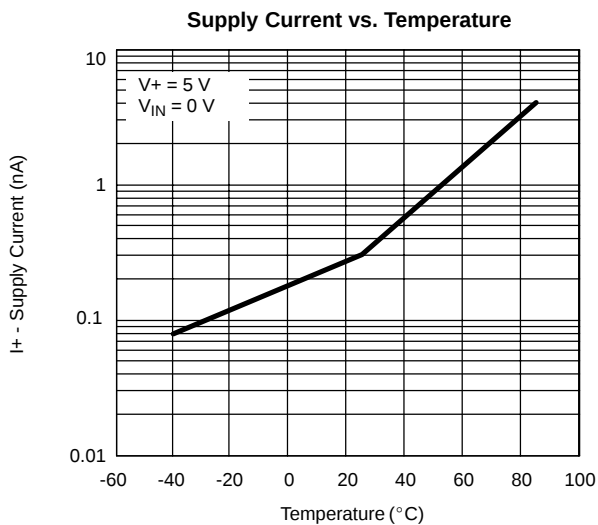
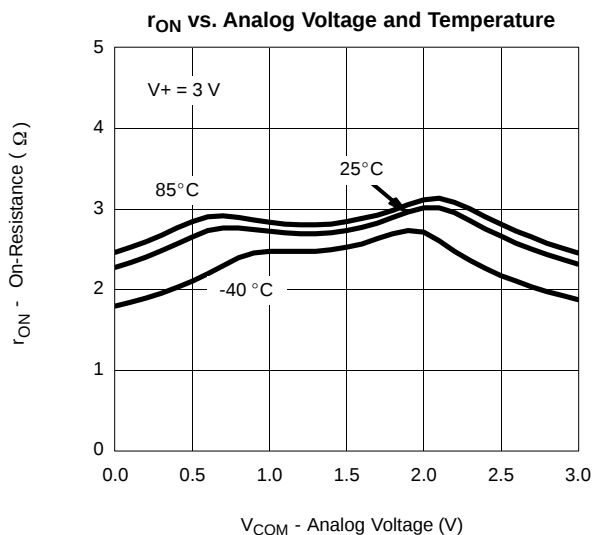
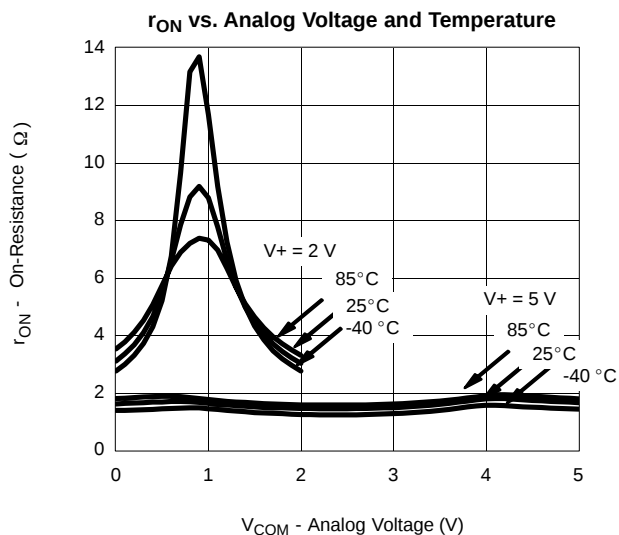
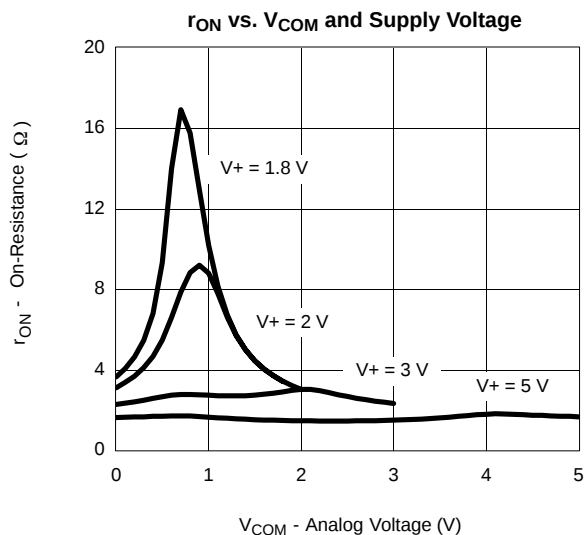


SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.4 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance	rON	V+ = 4.5 V, VCOM = 3 V, INO, INC = 10 mA	Room Full		1.4 1.6	2.3 2.8	Ω
rON Flatness ^d	rON Flatness	V+ = 4.5 V, VCOM = 0 to V+, INO, INC = 10 mA	Room		0.5		
Switch Off Leakage Current	INO(off), INC(off)	V+ = 5.5 V VNO, VNC = 1 V/4.5 V, VCOM = 4.5 V/1 V	Room Full	-1.2 -21		1.2 21	nA
	ICOM(off)		Room Full	-1.2 -21		1.2 21	
Channel-On Leakage Current	ICOM(on)	V+ = 5.5 V, V+ = 5.5 V VNO, VNC = VCOM = 1 V/4.5 V	Room Full	-1.2 -21		1.2 21	
Digital Control							
Input High Voltage	VINH		Full	2.4			V
Input Low Voltage	VINL		Full			0.8	
Input Capacitance	Cin		Full		5		pF
Input Current	IINL or IINH	VIN = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	tON	VNO or VNC = 3 V, RL = 300 Ω, CL = 35 pF Figure 1 and 2	Room Full		24	36 39	ns
Turn-Off Time ^d	tOFF		Room Full		9	22 25	
Break-Before-Make Time ^d	td		Room	1	15		
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω, Figure 3	Room		38		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		-61		dB
Crosstalk ^d	XTALK		Room		-67		
Source-Off Capacitance ^d	CNO(off), CNC(off)	VIN = 0 or V+, f = 1 MHz	Room		30		pF
Channel-On Capacitance ^d	CON		Room		96		
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	VIN = 0 or V+			0.1	1.0	μA
Power Consumption	PC					5.5	μW

Notes:

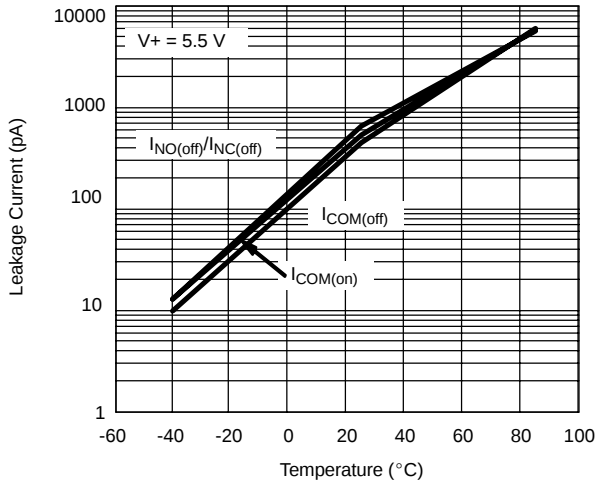
- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

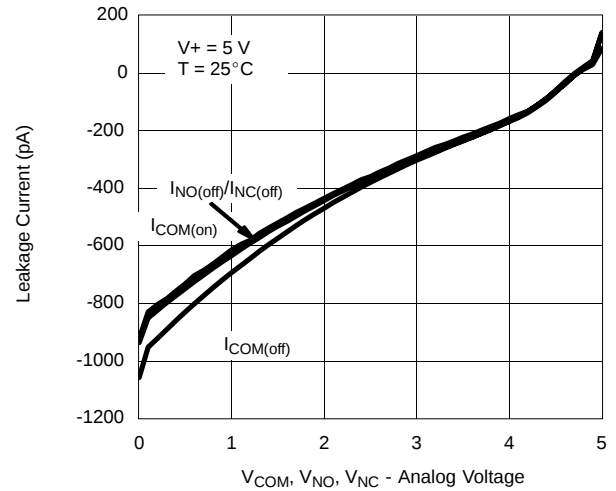


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

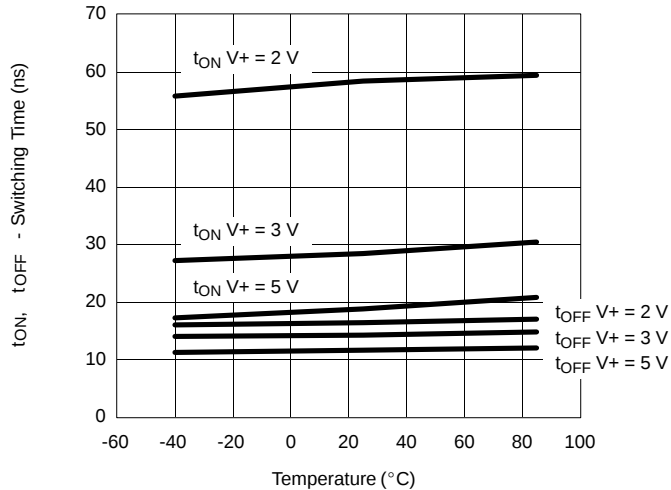
Leakage Current vs. Temperature



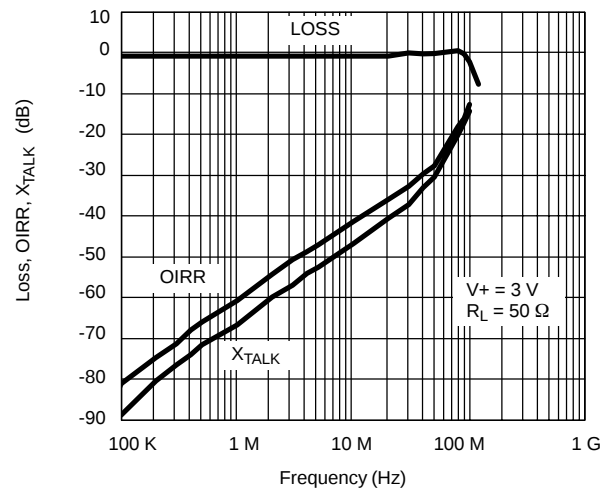
Leakage vs. Analog Voltage



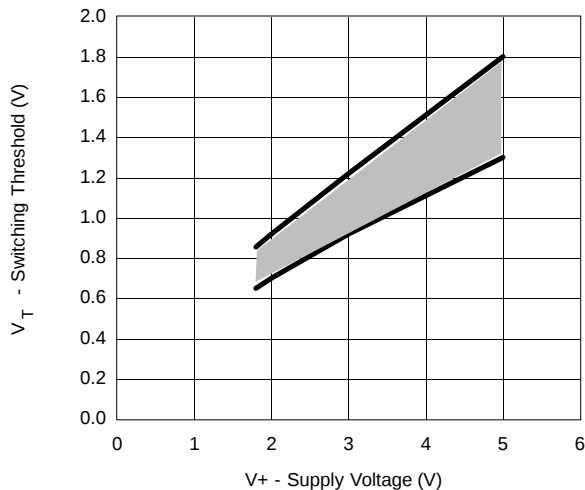
Switching Time vs. Temperature and Supply Voltage



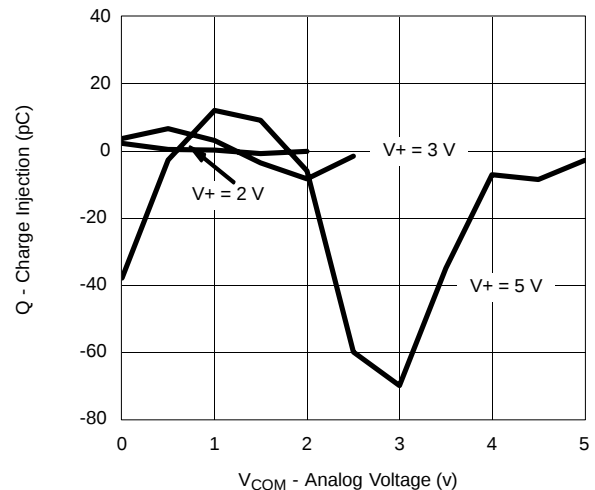
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



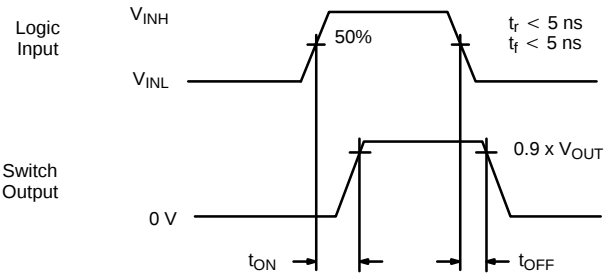
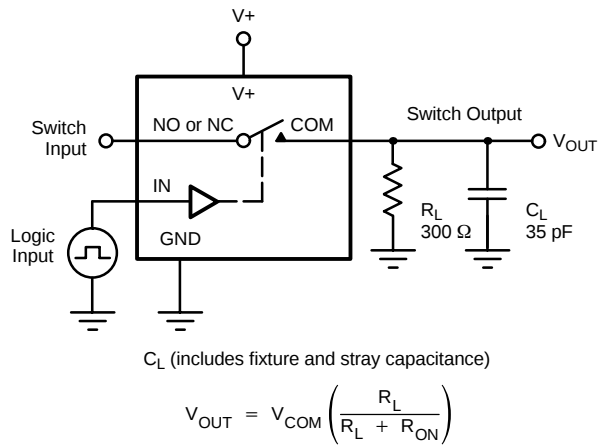
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage



TEST CIRCUITS



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

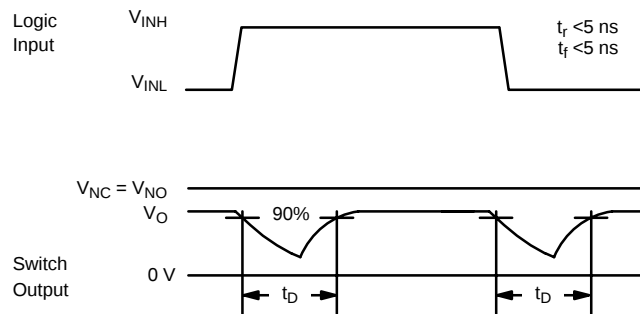
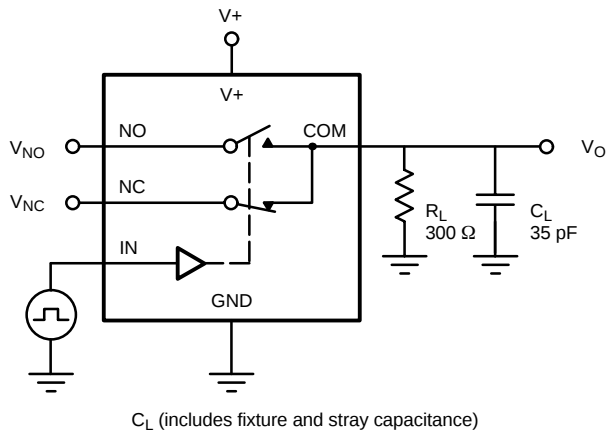
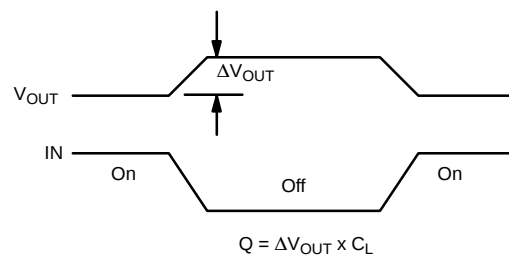
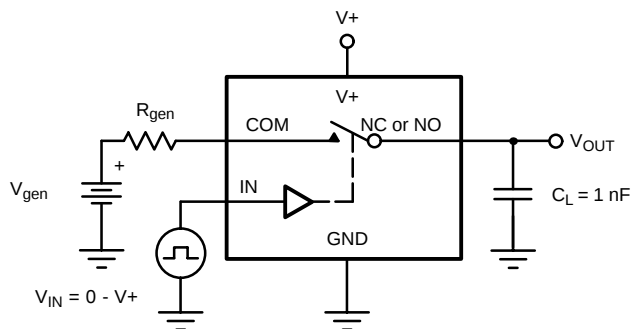


FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection



TEST CIRCUITS

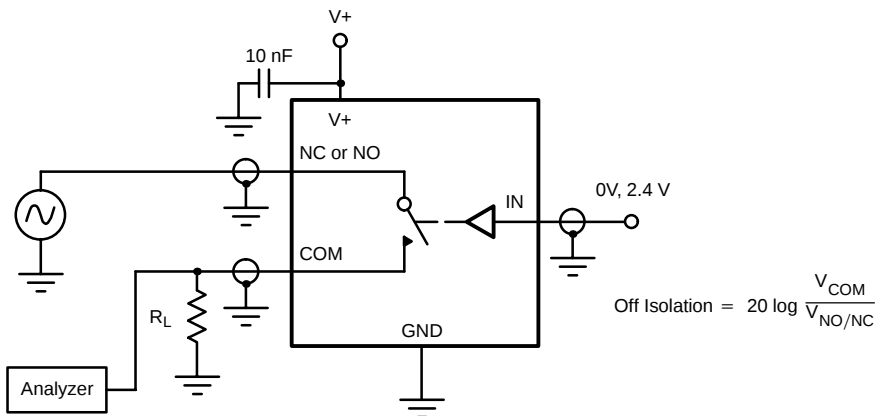


FIGURE 4. Off-Isolation

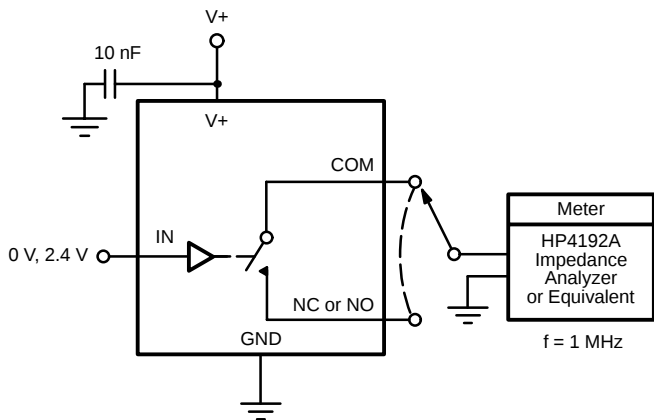
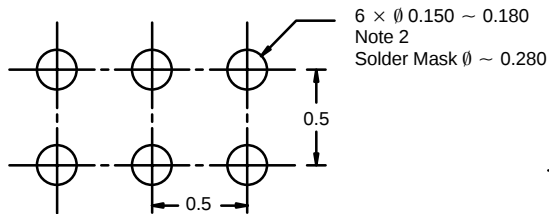


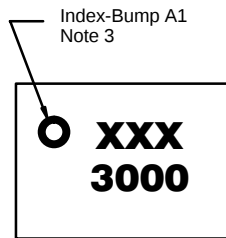
FIGURE 5. Channel Off/On Capacitance

PACKAGE OUTLINE

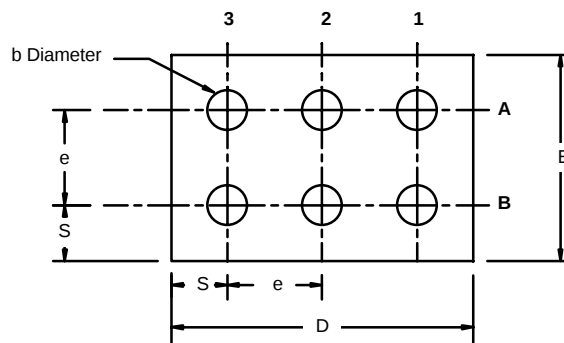
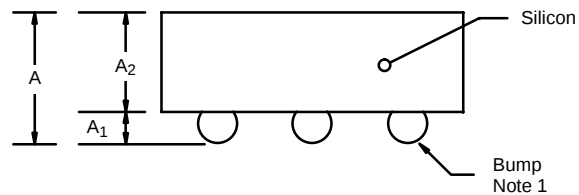
MICRO FOOT: 6-BUMP (2 X 3, 0.5-mm PITCH)



Recommended Land Pattern



Top Side (Die Back)



NOTES (Unless Otherwise Specified):

1. Bump is Eutectic 63/57 Sn/Pb.
2. Non-solder mask defined copper landing pad.
3. Laser Mark on silicon die back; no coating. Shown is not actual marking; sample only.

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.615	0.715	0.0242	0.0281
A ₁	0.140	0.190	0.0055	0.0075
A ₂	0.475	0.525	0.0187	0.0207
b	0.180	0.250	0.0071	0.0098
D	1.555	1.585	0.0612	0.0624
E	1.055	1.085	0.0415	0.0427
e	0.5 BASIC		0.0197 BASIC	
S	0.278	0.293	0.0109	0.0115

* Use millimeters as the primary measurement.