RoHS

Analog Dual Axis Micromachined Accelerometer

The MMA62XXAKEG series of dual axis (X and Y) silicon capacitive, micromachined accelerometers features a full digital signal processing for filtering, trim and data formatting. It has been optimized for analog output and offers an over-damped transducer.

Features

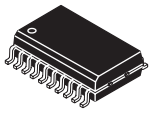
- Available in ±20/20g, ±50/50g, or ±100/100g versions. Additional g-ranges between 20 and 100g may be available upon request
- Full-scale range is independently specified for each axis
- 400 Hz, 4 Pole, 16 µs sample time, additional filter options are available
- Ratiometric analog voltage output
- Capture/hold input for system-wide synchronization support
- 3.3 or 5 V single supply operation
- On-chip temperature sensor and voltage regulator
- Internal self-test
- Minimal external component requirements
- Pb-free 20-pin SOIC package
- Qualified AEC-Q100, Rev. F Grade 2 (-40°C/ +105°C)

Typical Applications

- Crash Detection (Airbag)
- Impact and vibration monitoring
- Shock detection

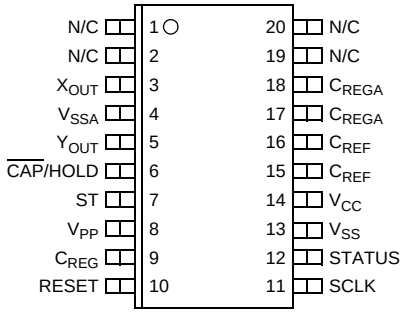
MMA6222AKEG
MMA6255AKEG
MMA621010AKEG

2-AXIS ACCELEROMETER



KEG SUFFIX (Pb-free)
20-LEAD SOIC
CASE 475A-02

PIN CONNECTIONS



20-PIN SOIC PACKAGE

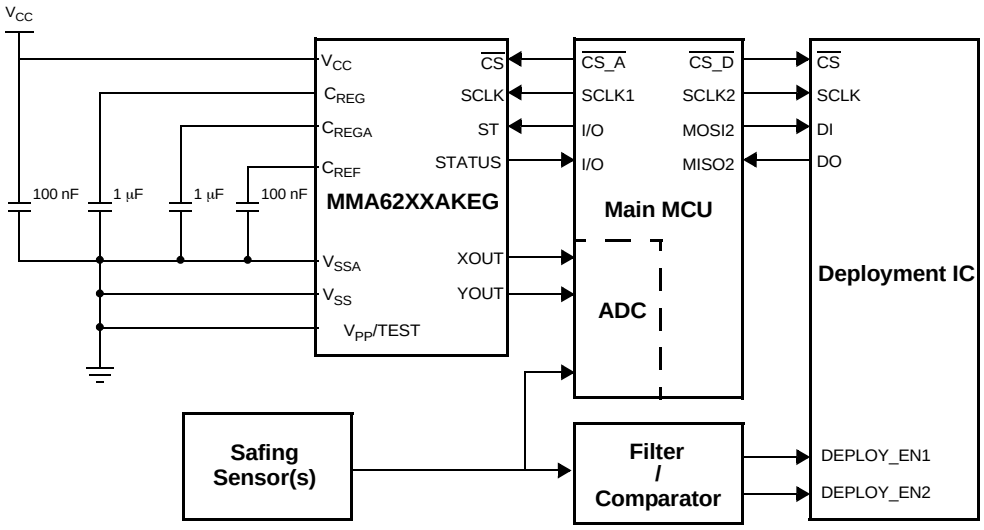
N/C: NO INTERNAL CONNECTION

ORDERING INFORMATION

Device Name	X-Axis g-Level	Y-Axis g-Level	Temperature Range	Package	Packaging
MMA6222AEG	20	20	-40 to +105°C	475A-02	Tubes
MMA6222AEGR2	20	20	-40 to +105°C	475A-02	Tape & Reel
MMA6222AKEG*	20	20	-40 to +105°C	475A-02	Tubes
MMA6222AKEGR2*	20	20	-40 to +105°C	475A-02	Tape & Reel
MMA6255AEG	50	50	-40 to +105°C	475A-02	Tubes
MMA6255AEGR2	50	50	-40 to +105°C	475A-02	Tape & Reel
MMA6255AKEG*	50	50	-40 to +105°C	475A-02	Tubes
MMA6255AKEGR2*	50	50	-40 to +105°C	475A-02	Tape & Reel
MMA621010AEG	100	100	-40 to +105°C	475A-02	Tubes
MMA621010AEGR2	100	100	-40 to +105°C	475A-02	Tape & Reel
MMA621010AKEG*	100	100	-40 to +105°C	475A-02	Tubes
MMA621010AKEGR2*	100	100	-40 to +105°C	475A-02	Tape & Reel

*Part number sourced from a different facility.

freescale semiconductor



Note: If one axis of the MMA62XXAKEG sensor is expected to be used as a confirmation of the other axis, Freescale recommends that MMA62XXAKEG used in conjunction with an additional sensing/safing device for each axis.

Figure 1-1 Simplified Airbag Application Diagram

1.1 INTRODUCTION

The MMA62XXKEG is trimmed to provide the most accurate voltage representation of acceleration at X_{OUT} and Y_{OUT}. This is done by adjusting the signal within the DSP to compensate for errors within the digital-to-analog converters. The SPI is disabled when the device is in normal operating mode, and dedicated ST (self-test activation) and STATUS pin functions are assigned.

1.2 BLOCK DIAGRAM

A block diagram illustrating the major components of the design is shown in Figure 1-2.

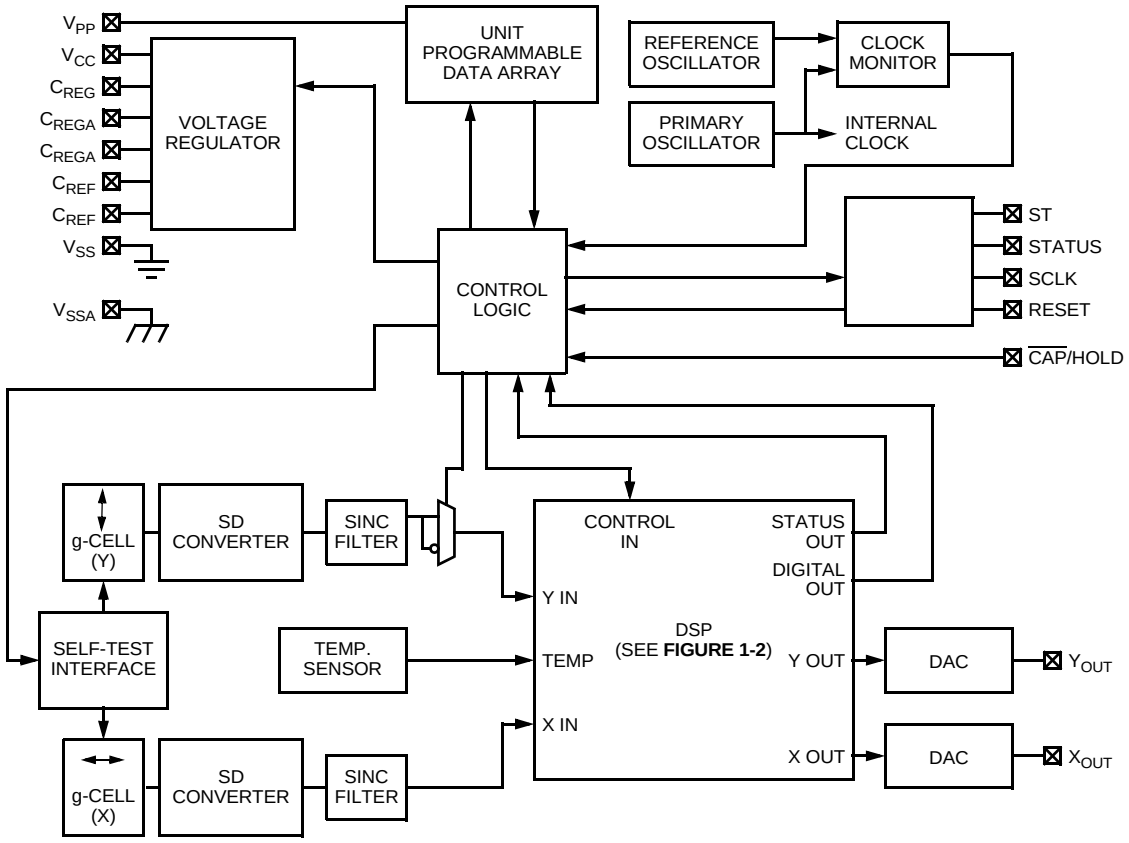


Figure 1-2 MMA62XXAKEG Block Diagram

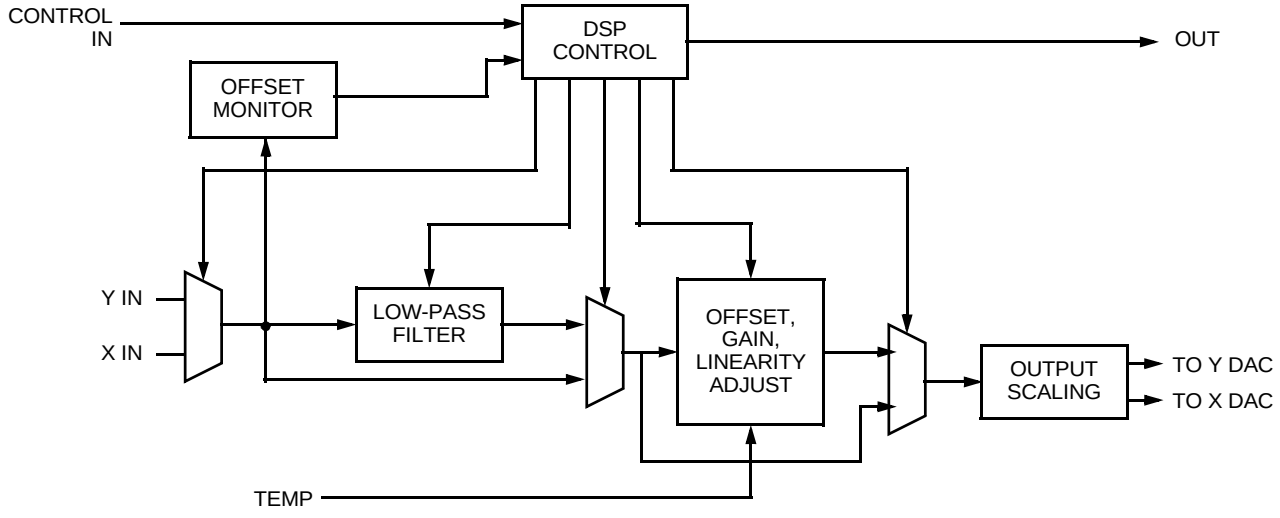
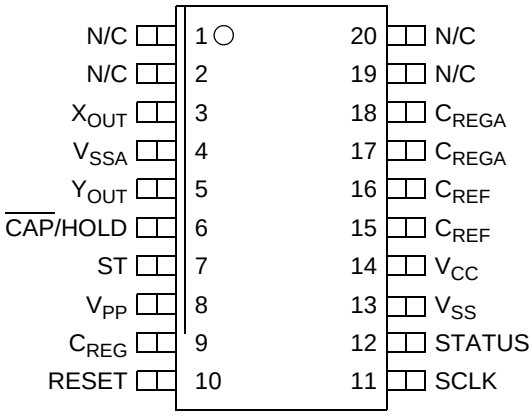


Figure 1-3 MMA62XXAKEG DSP Block Diagram
NOTE: Models of signal chain are available upon request

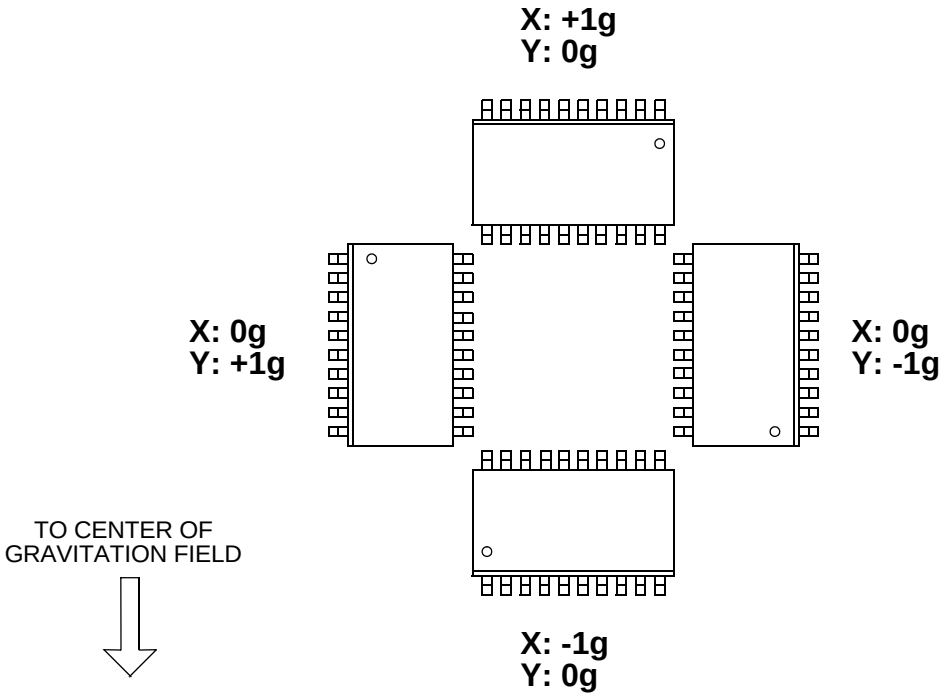
1.3 PIN FUNCTIONS

The pinout for the MMA62XXAKEG device is illustrated in Figure 1-4. Pin functions are described below. When self-test is active, the output becomes more positive in both axes if ST1 is cleared, or more negative in both axes if ST1 is set.



20-PIN SOIC PACKAGE

N/C: NO INTERNAL CONNECTION



Response to static orientation within 1g field.

Figure 1-4 MMA62XXAKEG Pinout

1.4 PIN FUNCTION DESCRIPTIONS

1.4.1 V_{CC}

This pin supplies power to the device. Careful printed wiring board layout and capacitor placement is critical to ensure best performance. An external bypass capacitor between this pin and V_{SS} is required, as described in Section 1.5.

1.4.2 V_{SS}

This pin is the power supply return node for the digital circuitry on the MMA62XXKEG device.

1.4.3 V_{SSA}

This pin is the power supply return node for analog circuitry on the MMA62XXAKEG device. An external bypass capacitor between this pin and V_{CC} is required, as described in Section 1.5.

1.4.4 C_{REG}

This pin is connected to the internal digital circuitry power supply rail. An external filter capacitor must be connected between this pin and V_{SS}, as described in Section 1.5.

1.4.5 C_{REGA}

These pins are connected in parallel to the internal analog circuitry power supply rail. One or two external filter capacitors must be connected between these pins and V_{SSA}, as described in Section 1.5. Two pins are provided to support redundant connection to the printed wiring board assembly. Redundant external capacitors may be connected to these pins for maximum reliability, as described in Section 1.5.

1.4.6 C_{REF}

These pins are connected in parallel to an internal reference voltage node utilized by the analog circuitry. One or two external filter capacitors must be connected between these pins and V_{SSA}, as described shown in Section 1.5. Two pins are provided to support redundant connection to the printed wiring board assembly. Redundant external capacitors may be connected to these pins for maximum reliability, as described in Section 1.5.

1.4.7 VPP

This pin should be tied directly to V_{SS}.

1.4.8 SCLK

This input may be left unconnected unless it is desired to initiate device reset as described in Section 1.4.9.

1.4.9 RESET

This pin may be used to initiate a hardware reset. If RESET is held low and SCLK is held high for 512 μs, the internal reset signal is asserted.

An internal pull-up device is connected to this pin.

1.4.10 STATUS

This pin provides an indicator of internal status. The STATUS output will be driven to a logic high level should any of the following fault conditions be detected:

- Internal parity fault
- Over-temperature condition
- Internal clock frequency fault
- Device reset
- Device initialization

Immediately following device reset, STATUS is placed in a high impedance state for approximately 800 μs. At the end of this time, STATUS is driven high and a 3ms stabilization delay required by the internal circuitry begins. The STATUS condition may not be cleared during the stabilization delay. Reset is reported by the device so the system can be aware of potential difficulties if unexpected resets occur.

Once asserted, the STATUS output will remain high until the ST pin is driven from a logic low to a logic high state. If a fault condition persists, the STATUS output will be driven high again as soon as it is cleared.

1.4.11 ST

This pin performs a dual function. When driven to a logic high level, the internal self-test voltage generator is activated. A low-to-high transition on this pin will clear the internal STATUS latch. Note that under certain fault conditions, the STATUS latch will be immediately reset, indicating a terminal fault condition.

A diagram illustrating operation of the STATUS latch following device initialization is illustrated in Figure 1-5.

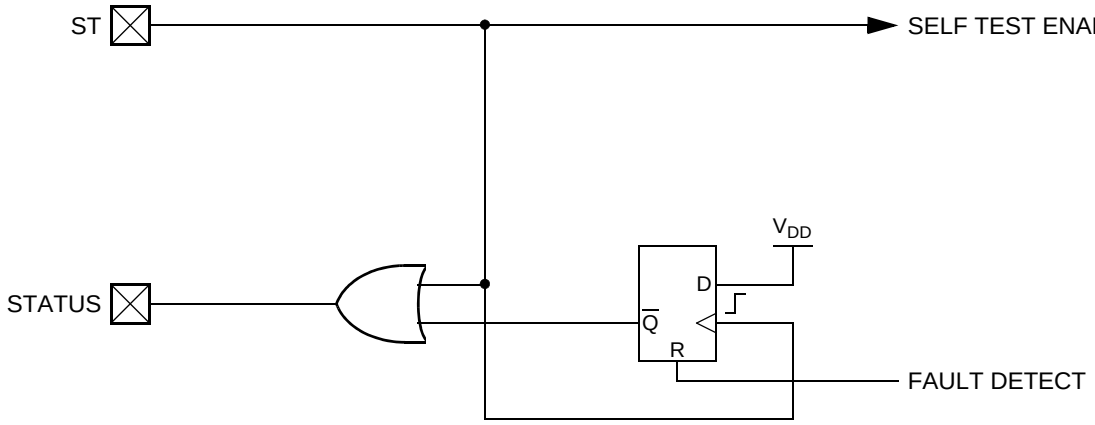


Figure 1-5 ST and STATUS Interaction

1.4.12 $\overline{\text{CAP}}$/HOLD

When this input pin is low, acceleration data is updated by the DSP whenever a data sample becomes available. Upon a low-to-high transition of $\overline{\text{CAP}}$/HOLD acceleration data is frozen. Acceleration data is not updated as long as the pin remains at a logic '1' level. This pin may be tied directly to V_{SS} if the hold function is not desired.

1.4.13 X_{OUT}, Y_{OUT}

Two digital-to-analog converters (DACs) are provided. These converters translate output of the DSP block into voltage levels proportional to the magnitude of the numerical result and ratiometric to V_{CC}.

1.5 EXTERNAL COMPONENTS

The connections illustrated in Figure 1-1 are recommended. Careful printed wiring board layout and component placement is essential for best performance. Low ESR capacitors must be connected to C_{REG} and C_{REGA} pins for the best performance. A grounded land area with solder mask should be placed under the package for improved shielding of the device from external effects. If a land area is not provided, no signals should be routed beneath the package. See Figure 1-1.

SECTION 2 PERFORMANCE SPECIFICATION

2.1 MAXIMUM RATINGS

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it. The device contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep input and output voltages within the range $V_{SS} \le V \le V_{CC}$.

Ref	Rating	Symbol	Value	Unit	
1	Supply Voltage	V_{CC}	-0.3 to +7	V	(1)
2	C_{REG}, C_{REGA}, C_{REF}	V_{REG}	-0.3 to +3	V	(1)
3	V_{PP}	V_{REG}	-0.3 to +11	V	(1)
4	SCLK, ST, $\overline{CAP}$/HOLD	V_{IN}	-0.3 to V_{CC} + 0.3	V	(1)
5	STATUS (high impedance state)	V_{IN}	-0.3 to V_{CC} + 0.3	V	(1)
6	X_{OUT}, Y_{OUT} (DACEN = 0)	V_{DAC}	-0.3 to V_{CC} + 0.3	V	(1)
7	Current Drain per Pin Excluding V_{CC} and V_{SS}	I	10	mA	(1)
8	Acceleration (without hitting internal g-cell stops)	g_{max}	±800	g	(1)
9	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±1500	g	(1)
10	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±2000	g	(1)
11	Drop Shock (to concrete surface)	h_{DROP}	1.2	m	(1)
	Electrostatic Discharge				
12	Human Body Model (HBM)	V_{ESD}	±2000	V	(1)
13	Charge Device Model (CDM)	V_{ESD}	±500	V	(1)
14	Machine Model (MM)	V_{ESD}	±200	V	(1)
15	Storage Temperature Range	T_{stg}	-40 to +125	°C	(1)

Notes:
1. Verified by characterization, not tested in production.

2.2 OPERATING RANGE

The operating ratings are the limits normally expected in the application and define the range of operation.

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
	Supply Voltage		V_L		V_H		
16	Standard Operating Voltage, 3.3V operating range	V_{CC}	+3.15	+3.3	+3.45	V	(1)
17	Standard Operating Voltage, 5V operating range	V_{CC}	+4.75	+5.0	+5.25	V	(1)
	Operating Temperature Range		T_L		T_H		
18		T_A	-40	—	+105	C	(2)

Notes:
1. Characterized at all values of V_L and V_H. Production test is conducted at typical voltage unless otherwise noted.
2. Parameters tested 100% at final test.

2.3 ELECTRICAL CHARACTERISTICS

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

Ref	Characteristic		Symbol	Min	Typ	Max	Units	
	Supply Current Drain							
19	Analog-only output configuration		I_{DD}		—	9.0	mA	(1)
	Power-On Recovery Threshold (See Figure 2-1)							
20	V_{CC}		V_{POR_N}	2.77	—	3.15	V	(2)
21	C_{REG}		V_{POR_N}	1.80	—	2.32	V	(2)
22	C_{REGA}		V_{POR_N}	2.18	—	2.50	V	(2)
23	C_{REF}		V_{POR_N}	1.11	—	1.29	V	(2)
	Power-On Reset Threshold (See Figure 2-1)							
24	V_{CC}		V_{POR_A}	2.77	—	2.95	V	(2)
25	C_{REG}		V_{POR_A}	1.80	—	2.10	V	(2)
26	C_{REGA}		V_{POR_A}	2.18	—	2.31	V	(2)
27	C_{REF}		V_{POR_A}	1.11		1.19	V	(2)
	Hysteresis (VPOR_N - VPOR_A, See Figure 2-1)				—			
28	V_{CC}		V_{HYST}	0	—	388	mV	
29	C_{REG}		V_{HYST}	0	—	300	mV	
30	C_{REGA}		V_{HYST}	0	—	261	mV	
31	C_{REF}		V_{HYST}	0		150	mV	
32	Minimum Functional Voltage (See Figure 2-1)		V_{DACU}	—	—	2.0	V	(2)
	Internally Regulated Voltages							
33	C_{REG}		V_{DD}	2.42	2.50	2.58	V	(1)
34	C_{REGA} (3)	*	$V_{2.5}$	2.42	2.50	2.58	V	(1)
35	C_{REF}	*	V_{REF}	1.20	1.25	1.29	V	(1)
	External Filter Capacitor (C_{REG}, C_{REGA})							
36	Value		C_{REG}	800	1000	—	nF	(2)
37	ESR (including interconnect resistance)		ESR	—	—	200	mΩ	(2)
	Power Supply Coupling (4)							
38	Analog output			See Figure 2-2				(2)
	Analog Sensitivity (X_{OUT}, Y_{OUT})							
39	20g Range	*	ASENS	—	23.40	—	mV/V/g	(1)(5)
40	35g Range	*	ASENS	—	13.40	—	mV/V/g	(1)(5)
41	50g Range	*	ASENS	—	9.37	—	mV/V/g	(1)(5)
42	100g Range	*	ASENS	—	4.68	—	mV/V/g	(1)(5)
	Sensitivity Error							
43	T_A = 25°C	*	ΔSENS	-8	—	+8	%	(1)(5)
44	40°C ≤ T_A ≤ 105°C	*	ΔSENS	-8	—	+8	%	(1)(5)
	Offset at 0g							
45	Analog output (X_{OUT}, Y_{OUT})	*	A_{OUT}	0.46 × V_{CC}	0.5 × V_{CC}	0.54 × V_{CC}	V	(1)(5)

Notes:

1. Parameters tested 100% at final test.
2. Verified by characterization, not tested in production.
3. Tested at $V_{CC} = V_L$ and $V_{CC} = V_H$.
4. Power supply ripple at frequencies greater than 900 kHz should be minimized to the greatest extent possible.
5. Devices are trimmed at 100 Hz with 1000 Hz low-pass filter option selected.

(#) Indicates a FSL significant parameter (CPK > 1.33).

(*) Indicates a FSL critical parameter (CPK > 1.67).

2.3 ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
	Output value on overrange						
46	20g Range	g_{OVER}	+20.0	+20.9	+22.1	g	(3)
47	35g Range	g_{OVER}	+35.0	+36.6	+38.7	g	(3)
48	50g Range	g_{OVER}	+50.0	+52.1	+55.3	g	(3)
49	100g Range	g_{OVER}	+100.1	+104.3	+110.5	g	(3)
	Output value on Underrange						
50	20g Range	g_{UNDER}	-20.1	-20.9	-22.2	g	(3)
51	35g Range	g_{UNDER}	-35.1	-36.6	-38.8	g	(3)
52	50g Range	g_{UNDER}	-50.1	-52.2	-55.4	g	(3)
53	100g Range	g_{UNDER}	-100.3	-104.5	-110.7	g	(3)
	Maximum acceleration without saturation of internal circuitry						
54	All ranges	g_{SAT}	-200	—	+200	g	(3)
55	Nonlinearity	NL_{OUT}	-1	—	1	% FSR	(3)
56	Noise (1Hz-1kHz)	n_{SD}	—	—	1.1	mg/$\sqrt{Hz}$	(3)
	Positive Self Test Output Change (X_{OUT}, Y_{OUT}, analog)						
57	T_A = 25°C	ΔST	10	—	18	% FS	(1)
58	-40°C ≤ T_A ≤ 105°C	ΔST	10	—	18	% FS	(1)
	Cross-Axis Sensitivity						
59	V_{ZX}	V_{ZX}	-4	—	+4	%	(3)
60	V_{YX}	V_{YX}	-4	—	+4	%	(3)
61	V_{ZY}	V_{ZY}	-4	—	+4	%	(3)
62	V_{XY}	V_{XY}	-4	—	+4	%	(3)
	DAC Characteristics (X_{OUT}, Y_{OUT})						
63	Minimum Output Level, I_{OUT} = -200 μA	AV_{LOW}	—	—	0.25	V	(2)
64	Maximum Output Level, I_{OUT} = 200 μA	AV_{HIGH}	V_{CC} - 0.25	—	—	V	(2)
65	Offset Error	OFST	-0.2	—	+0.2	%FSR	(2)
66	Gain Error	GERR	-0.3	—	+0.3	%FSR	(2)
67	Differential Nonlinearity	DNL	-2		+2	digit	(2)
	Integral Nonlinearity						
68	T_A = 25°C	INL	-3	—	+3	digit	(2)
69	-40°C ≤ T_A ≤ 105°C	INL	-3.5	—	+3.5	digit	(3)
	Output High Voltage STATUS (I_{Load} = -100 μA)						
70	3.15 V ≤ (V_{CC} - V_{SS}) ≤ 3.45 V	V_{OH}	3.25	—	—	V	(2)
71	4.75 V ≤ (V_{CC} - V_{SS}) ≤ 5.25 V	V_{OH}	3.75	—	—	V	(2)
	Output Low Voltage STATUS (I_{Load} = 100 μA)						
72	3.15 V ≤ (V_{CC} - V_{SS}) ≤ 3.45 V	V_{OL}	—	—	0.4	V	(2)
73	4.75 V ≤ (V_{CC} - V_{SS}) ≤ 5.25 V	V_{OL}	—	—	0.4	V	(2)
	Output Loading (STATUS)						
74	Load Resistance	Z_{OUT}	47	—	—	kΩ	(3)
75	Load Capacitance	C_{OUT}	—	—	35	pF	(3)

Notes:
1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.

2.3 ELECTRICAL CHARACTERISTICS (CONTINUED)

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
	Output Loading (X_{OUT}, Y_{OUT})						
76	Load Resistance	Z_{OUT}	25	—	—	kΩ	(3)
77	Load Capacitance	C_{OUT}	—	—	60	pF	(3)
	Input High Voltage						
	RESET, SCLK, ST, $\overline{CAP}$/HOLD						
78	3.15 V ≤ (V_{CC} - V_{SS}) ≤ 3.45 V	V_{IH}	1.5	—	—	V	(2)
79	4.75 V ≤ (V_{CC} - V_{SS}) ≤ 5.25 V	V_{IH}	2.5	—	—	V	(2)
	Input Low Voltage						
	RESET, SCLK, ST, $\overline{CAP}$/HOLD						
80	3.15 V ≤ (V_{CC} - V_{SS}) ≤ 3.45 V	V_{IL}	—	—	0.85	V	(2)
81	4.75 V ≤ (V_{CC} - V_{SS}) ≤ 5.25 V	V_{IL}	—	—	1.0	V	(2)
	Input Current						
	High (at V_{IH})						
82	SCLK, ST, $\overline{CAP}$/HOLD	I_{IH}	-30	-50	-260	μA	(2)
83	V_{PP}/TEST (internal pulldown resistor)	R_{IN}	190	270	350	kΩ	(2)
84	Low (at V_{IL})						
85	RESET	I_{IL}	30	50	260	μA	(2)

Notes:
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.

2.4 CONTROL TIMING

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
	DSP Low-Pass Filter (Note 9) Cutoff frequency (Note 10)						
86	Filter Option $0C, $1F	$f_{C(LPF)}$	380	400	420	Hz	(7)
87	DSP Low-Pass Filter Cutoff frequency (-3dB, referenced to 0 Hz) Filter $0C, $1F	$f_{C(LPF)}$	335	353	371	Hz	(7)
88	Filter Order Filter $00 - $12	O_{LPF}	—	4	—	1	(7)
89	Power-On Recovery Time Power applied to X_{OUT}, Y_{OUT} valid	t_{XY}	——	—	10	ms	(1)
90	Internal Oscillator Frequency	f_{OSC}	3.8	4.0	4.2	MHz	(1)
91	Clock Monitor Threshold	f_{MON}	3.6	—	4.4	MHz	(7)
92	Chip Select to Internal Reset (See Figure 2-3)	t_{CSRES}	486	512	538	µs	(7)
	DAC Low-Pass Filter						
93	Number of Poles	nPOLES	—	1	—	unit	(1)
94	Cutoff Frequency	f_C	5	10	20	kHz	(7)
95	Sensing Element Rolloff Frequency (-3 dB)	BW_{GCELL}	—	3	—	kHz	(1)

Notes:

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a FSL critical parameter (CPK > 1.67). (#) Indicates a FSL significant parameter (CPK > 1.33).
7. Functionality verified 100% via scan. Timing characteristic is directly determined by internal oscillator frequency.
9. Devices are trimmed at 100 Hz with 1000 Hz low-pass filter option selected.
10. Low-pass filter characteristics match those of other Freescale accelerometer devices. Cutoff frequencies shown are -4dB referenced to 0 Hz response, to correspond with previous specifications.

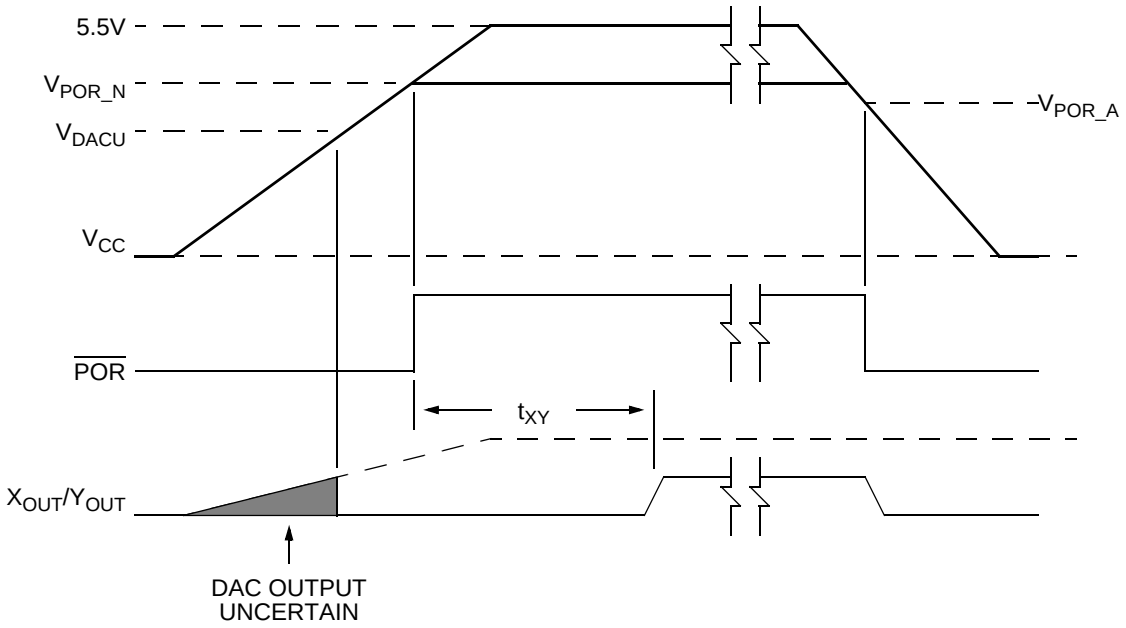


Figure 2-1 Power-Up Timing

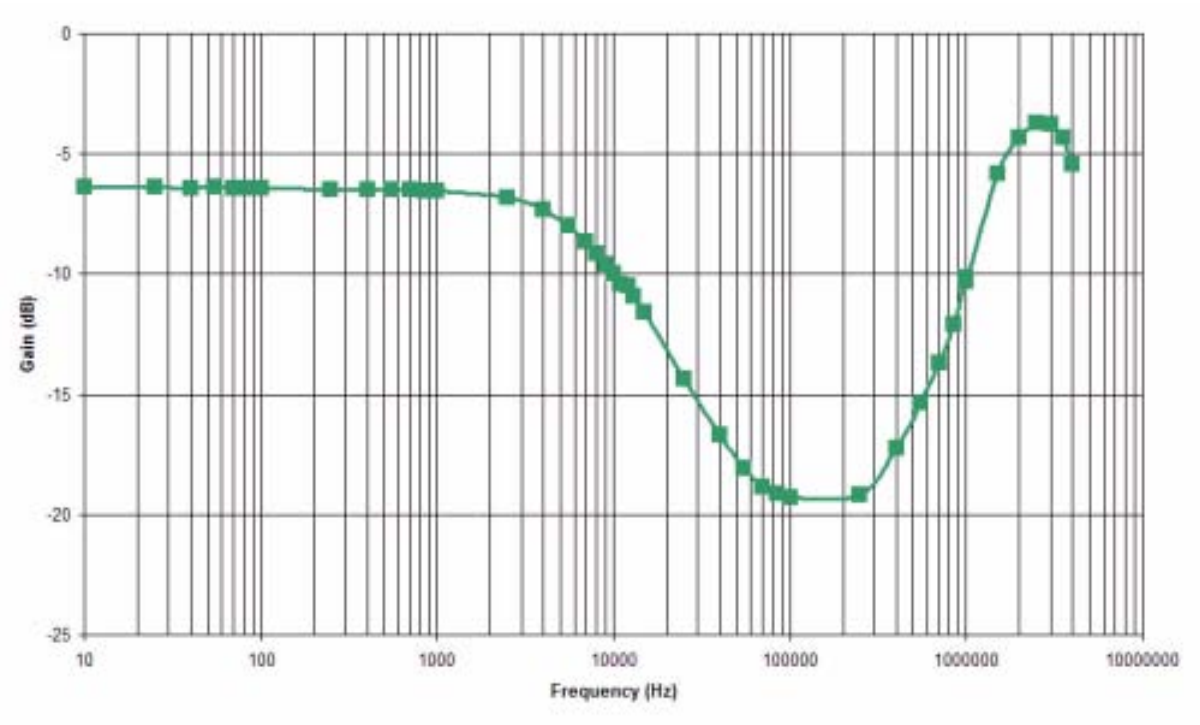


Figure 2-2 Power Supply Coupling - DAC Outputs

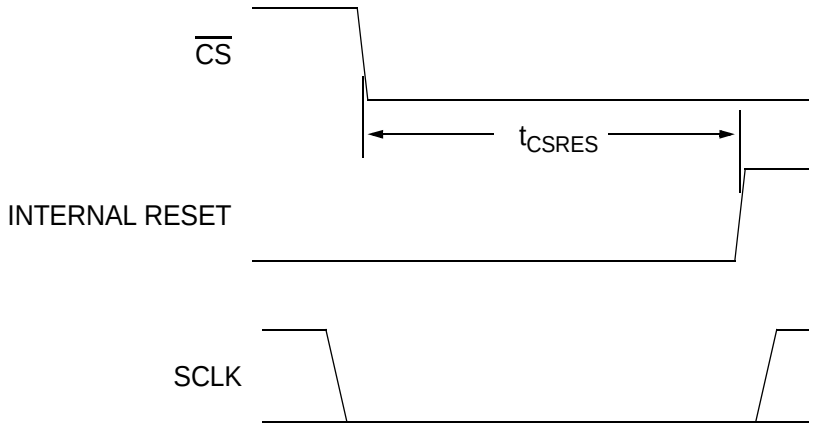
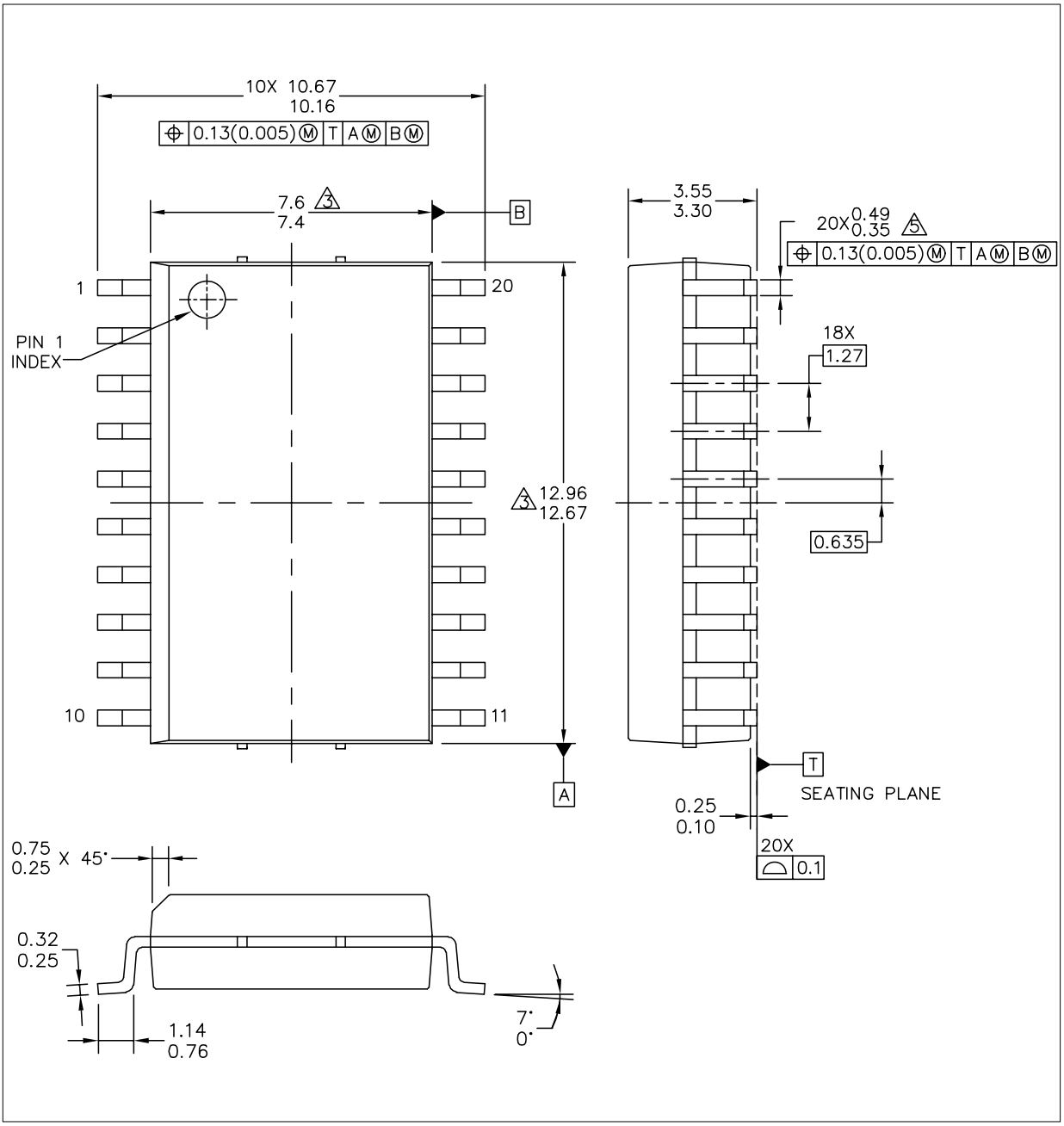


Figure 2-3 $\overline{CS}$ Reset Timing

PACKAGE DIMENSIONS



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	CASE NUMBER: 475A–02	06 JUL 2006
	STANDARD: NON–JEDEC	

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. THIS DIMENSION DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15(0.006) PER SIDE.
5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13(0.005) TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
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MMA6222AKEG
Rev. 0
12/2009