CY7C09099V

3.3 V, 128K × 8 Synchronous Dual-Port Static RAM

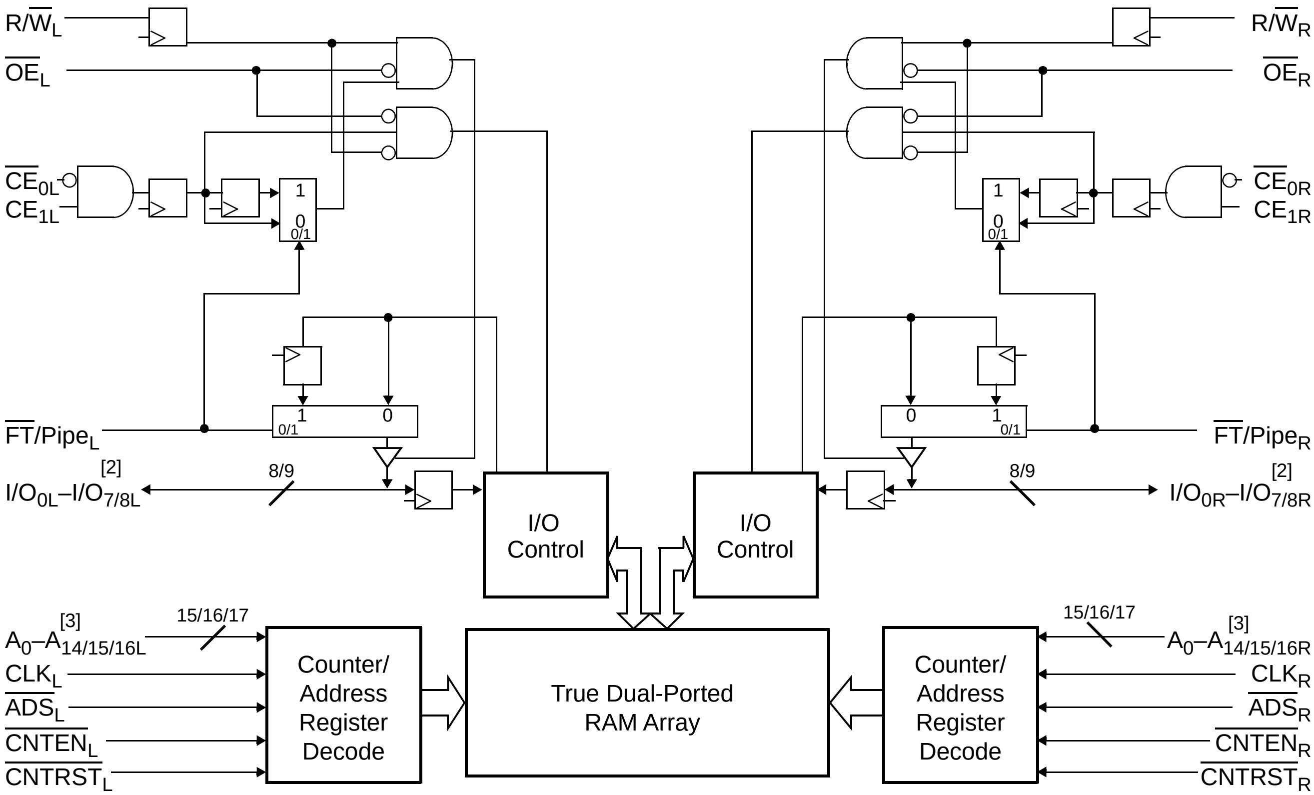
Features

- True Dual-Ported memory cells which enable simultaneous access of the same memory location
- Flow-through and Pipelined devices
- 128K × 8 organizations (CY7C09099V)
- Three Modes
  - Flow-through
  - Pipelined
  - Burst
- Pipelined output mode on both ports enables fast 100-MHz operation
- 0.35-micron CMOS for optimum speed and power
- High-speed clock to data access 7.5[1]/12 ns (max.)
- 3.3-V low operating power
  - Active = 115 mA (typical)
  - Standby = 10 µA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
- Shorten cycle times
- Minimize bus noise
- Supported in Flow-through and Pipelined modes
- Dual Chip Enables for easy depth expansion
- Automatic power down
- Commercial and Industrial temperature ranges
- Available in 100-pin TQFP
- Pb-free packages available

For a complete list of related documentation, click here.

Note
1. See page 8 and page 9 for Load Conditions.

Logic Block Diagram



Notes
2. I/O_0–I/O_7 for ×8 devices, I/O_0–I/O_8 for ×9 devices.
3. A_0–A_{14} for 32K and A_0–A_{16} for 128K devices.

Functional Description

The CY7C09099V is high speed synchronous CMOS 128K × 8 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.[4] Registers on control, address, and data lines enable minimal setup and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid t_{CD2} = 7.5 ns[5] (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode, data is available t_{CD1} = 22 ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the $\overline{FT}$/Pipe pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW-to-HIGH transition of the clock signal. The internal write pulse is self-timed to enable the shortest possible cycle times.

A HIGH on $\overline{CE}_0$ or LOW on CE_1 for one clock cycle powers down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables enables easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with $\overline{CE}_0$ LOW and CE_1 HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and use the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe ($\overline{ADS}$). When the port's Count Enable ($\overline{CNTEN}$) is asserted, the address counter increments on each LOW-to-HIGH transition of that port's clock signal. This reads/writes one word from/into each successive address location until $\overline{CNTEN}$ is deasserted. The counter can address the entire memory array and loops back to the start. Counter Reset ($\overline{CNTRST}$) is used to reset the burst counter.

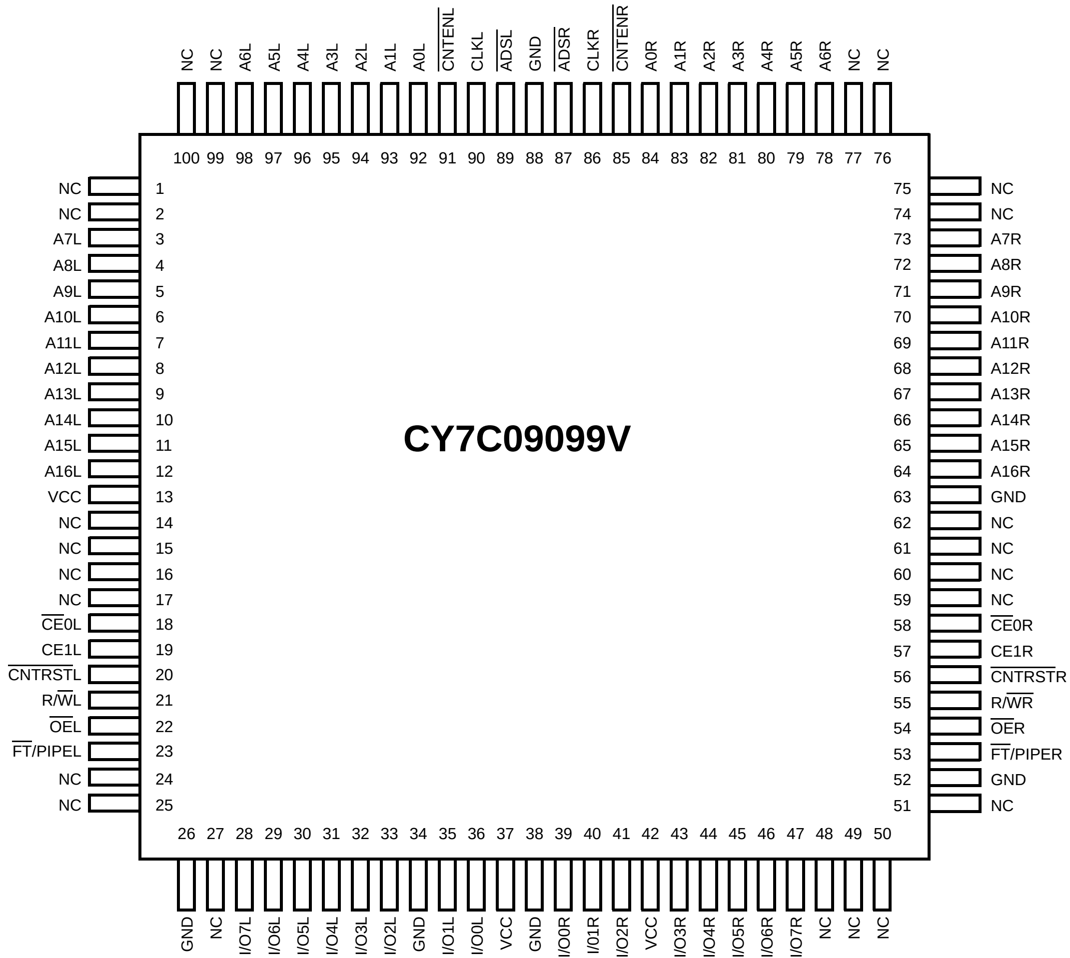
All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages.

Notes
4. When writing simultaneously to the same location, the final value cannot be guaranteed.
5. See page 8 and page 9 for Load Conditions.

Contents

Pin Configuration

Figure 1. 100-pin TQFP (Top View) - CY7C09099V (128K × 8)



Selection Guide

Description	CY7C09099V-7[6]	CY7C09099V-12
f_{MAX2} (MHz) (Pipelined)	83	50
Max. Access Time (ns) (Clock to Data, Pipelined)	7.5	12
Typical Operating Current I_{CC} (mA)	155	115
Typical Standby Current for I_{SB1} (mA) (Both Ports TTL Level)	25	20
Typical Standby Current for I_{SB3} (μA) (Both Ports CMOS Level)	10	10

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{16L}	A_{0R}–A_{16R}	Address Inputs (A_0–A_{14} for 32K and A_0–A_{16} for 128K devices).
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW to access the part using an externally supplied address. Asserting this signal LOW also loads the burst counter with the address present on the address pins.
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enable Input. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$).
CLK_L	CLK_R	Clock Signal. This input can be free running or strobed. Maximum clock input rate is f_{MAX}.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. $\overline{CNTEN}$ is disabled if $\overline{ADS}$ or $\overline{CNTRST}$ are asserted LOW.
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset Input. Asserting this signal LOW resets the burst address counter of its respective port to zero. $\overline{CNTRST}$ is not disabled by asserting $\overline{ADS}$ or $\overline{CNTEN}$.
I/O_{0L}–I/O_{8L}	I/O_{0R}–I/O_{8R}	Data Bus Input/Output (I/O_0–I/O_7 for ×8 devices; I/O_0–I/O_8 for ×9 devices).
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable Input. This signal must be asserted LOW to enable the I/O data pins during read operations.
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipelined Select Input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH.
GND		Ground Input.
NC		No Connect.
V_{CC}		Power Input.

Note

6. See page 8 and page 9 for Load Conditions.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.[7]

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage to Ground Potential ....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State ....–0.5 V to V_{CC} + 0.5 V

DC Input Voltage ....–0.5 V to V_{CC} + 0.5 V

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... > 2001 V

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 300 mV
Industrial[8]	–40 °C to +85 °C	3.3 V ± 300 mV

Electrical Characteristics

Over the Operating Range

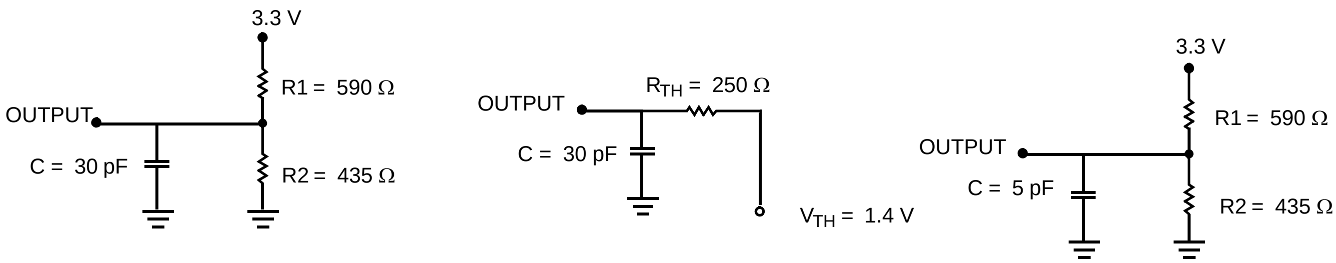
Parameter	Description		CY7C09099V -7[9] Min	-7[9] Typ	-7[9] Max	-12 Min	-12 Typ	-12 Max	Unit
V_{OH}	Output HIGH Voltage (V_{CC} = Min., I_{OH} = –4.0 mA)		2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW Voltage (V_{CC} = Min., I_{OH} = +4.0 mA)		–		0.4	–		0.4	V
V_{IH}	Input HIGH Voltage		2.0		–	2.0		–	V
V_{IL}	Input LOW Voltage		–		0.8	–		0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA) Outputs Disabled	Commercial	–	155	275	–	115	205	mA
		Industrial[8]		275	390		–	–	mA
I_{SB1}	Standby Current (Both Ports TTL Level)[10] $\overline{CE}_L$ & $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}	Commercial		25	85		20	50	mA
		Industrial[8]		85	120		–	–	mA
I_{SB2}	Standby Current (One Port TTL Level)[10] $\overline{CE}_L$ | $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}	Commercial		105	165		85	140	mA
		Industrial[8]		165	210		–	–	mA
I_{SB3}	Standby Current (Both Ports CMOS Level)[10] $\overline{CE}_L$ & $\overline{CE}_R$ ≥ V_{CC} – 0.2 V, f = 0	Commercial		10	250		10	250	µA
		Industrial[8]		10	250		–	–	µA
I_{SB4}	Standby Current (One Port CMOS Level)[10] $\overline{CE}_L$ | $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}	Commercial		95	125		75	100	mA
		Industrial[8]		125	170		–	–	mA

Notes
7. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
8. Industrial parts are available in CY7C09099V.
9. See page 8 and page 9 for Load Conditions.
10. $\overline{CE}_L$ and $\overline{CE}_R$ are internal signals. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).

Capacitance

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25\ °C$, f = 1 MHz, $V_{CC} = 3.3\ V$	10	pF
C_{OUT}	Output Capacitance		10	pF

Figure 2. AC Test Loads



(a) Normal Load (Load 1)

(b) Thévenin Equivalent (Load 1)

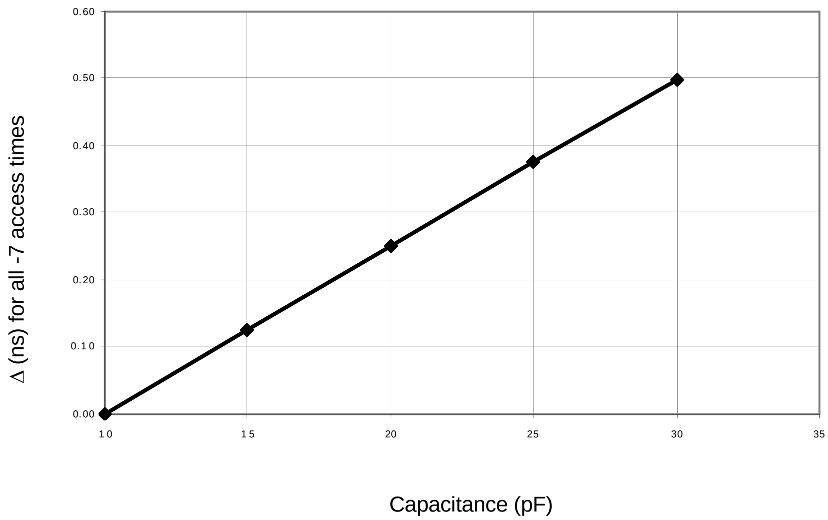
(c) Three-State Delay (Load 2)
(Used for t_{CKLZ}, t_{OLZ}, & t_{OHZ} including scope and jig)

Figure 3. AC Test Loads (Applicable to -6 and -7 only)[11]

(a) Load 1 (-6 and -7 only)

Note
11. Test Conditions: C = 10 pF.

Figure 4. Load Derating Curve



Switching Characteristics

Over the Operating Range

Parameter	Description	CY7C09099V -7[12] Min	CY7C09099V -7[12] Max	CY7C09099V -12 Min	CY7C09099V -12 Max	Unit
f_{MAX1}	f_{Max} Flow-through	–	45	–	33	MHz
f_{MAX2}	f_{Max} Pipelined	–	83	–	50	MHz
t_{CYC1}	Clock Cycle Time - Flow-through	22	–	30	–	ns
t_{CYC2}	Clock Cycle Time - Pipelined	12	–	20	–	ns
t_{CH1}	Clock HIGH Time - Flow-through	7.5	–	12	–	ns
t_{CL1}	Clock LOW Time - Flow-through	7.5	–	12	–	ns
t_{CH2}	Clock HIGH Time - Pipelined	5	–	8	–	ns
t_{CL2}	Clock LOW Time - Pipelined	5	–	8	–	ns
t_R	Clock Rise Time	–	3	–	3	ns
t_F	Clock Fall Time	–	3	–	3	ns
t_{SA}	Address Set-Up Time	4	–	4	–	ns
t_{HA}	Address Hold Time	0	–	1	–	ns
t_{SC}	Chip Enable Set-Up Time	4	–	4	–	ns
t_{HC}	Chip Enable Hold Time	0	–	1	–	ns
t_{SW}	R/$\overline{W}$ Set-Up Time	4	–	4	–	ns
t_{HW}	R/$\overline{W}$ Hold Time	0	–	1	–	ns
t_{SD}	Input Data Set-Up Time	4	–	4	–	ns
t_{HD}	Input Data Hold Time	0	–	1	–	ns
t_{SAD}	$\overline{ADS}$ Set-Up Time	4	–	4	–	ns
t_{HAD}	$\overline{ADS}$ Hold Time	0	–	1	–	ns
t_{SCN}	$\overline{CNTEN}$ Set-Up Time	4.5	–	5	–	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0	–	1	–	ns
t_{SRST}	$\overline{CNTRST}$ Set-Up Time	4	–	4	–	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0	–	1	–	ns
t_{OE}	Output Enable to Data Valid	–	9	–	12	ns
t_{OLZ}[13, 14]	$\overline{OE}$ to Low Z	2	–	2	–	ns
t_{OHZ}[13, 14]	$\overline{OE}$ to High Z	1	7	1	7	ns
t_{CD1}	Clock to Data Valid - Flow-through	–	18	–	25	ns
t_{CD2}	Clock to Data Valid - Pipelined	–	7.5	–	12	ns
t_{DC}	Data Output Hold After Clock HIGH	2	–	2	–	ns
t_{CKHZ}[13, 14]	Clock HIGH to Output High Z	2	9	2	9	ns
t_{CKLZ}[13, 14]	Clock HIGH to Output Low Z	2	–	2	–	ns

Notes
12. See page 8 and page 9 for Load Conditions.
13. Test conditions used are Load 2.
14. This parameter is guaranteed by design, but it is not production tested.

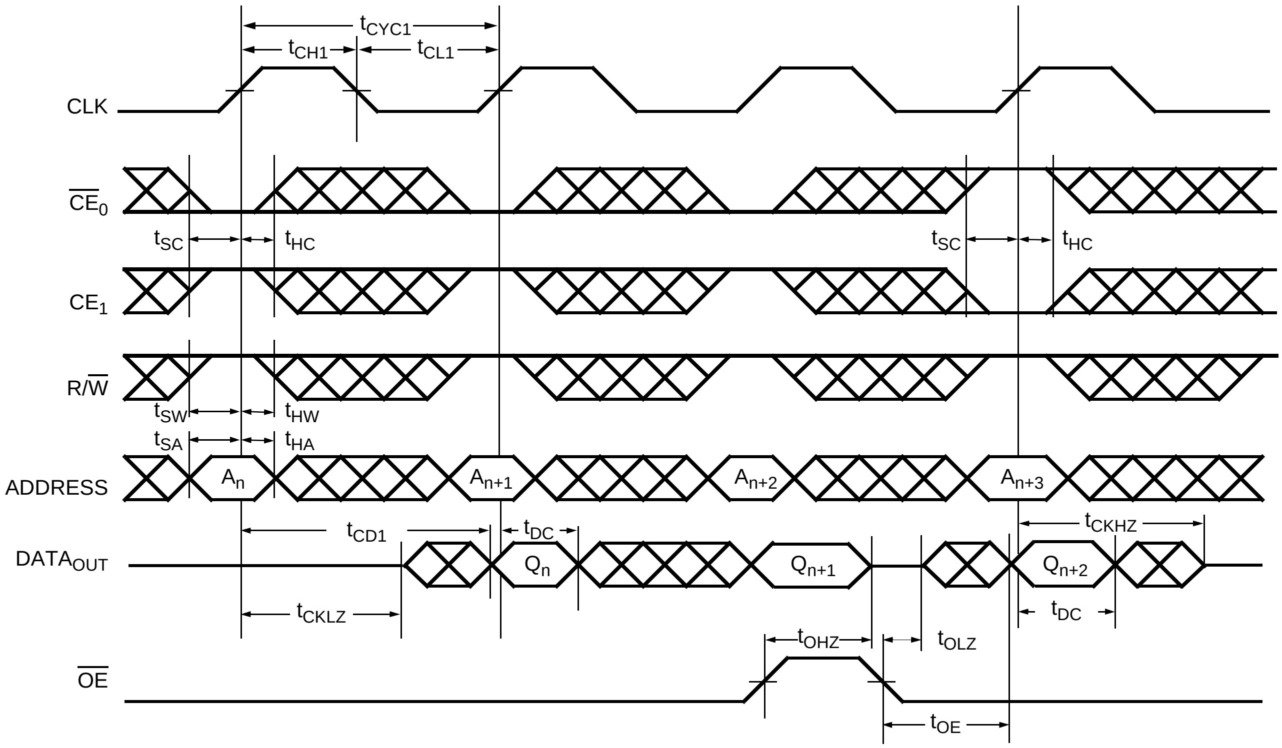
Switching Characteristics (continued)

Over the Operating Range

Parameter	Description	CY7C09099V -7[12] Min	CY7C09099V -7[12] Max	CY7C09099V -12 Min	CY7C09099V -12 Max	Unit
Port to Port Delays						
t_{CWDD}	Write Port Clock HIGH to Read Data Delay	–	35	–	40	ns
t_{CCS}	Clock to Clock Set-Up Time	–	10	–	15	ns

Switching Waveforms

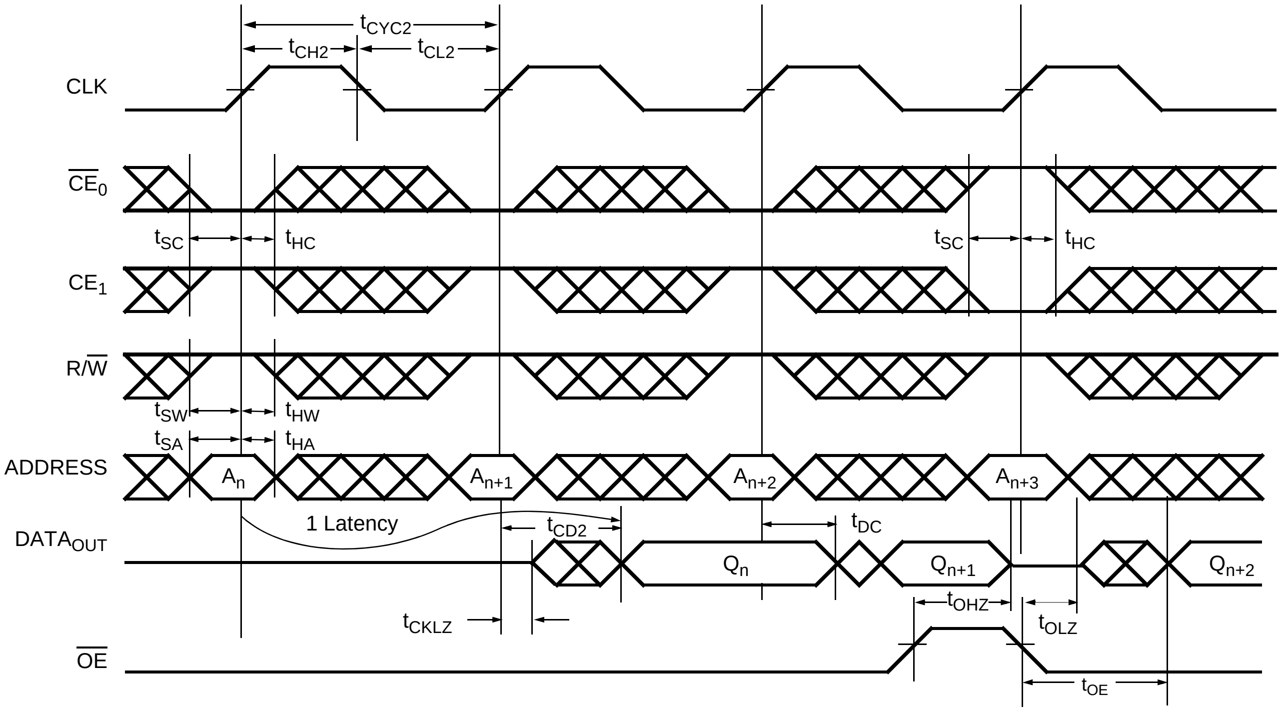
Figure 5. Read Cycle for Flow-through Output ($\overline{FT}$/PIPE = V_{IL})[15, 16, 17, 18]



Notes
15. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
16. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
17. The output is disabled (high-impedance state) by $\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL} following the next rising edge of the clock.
18. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

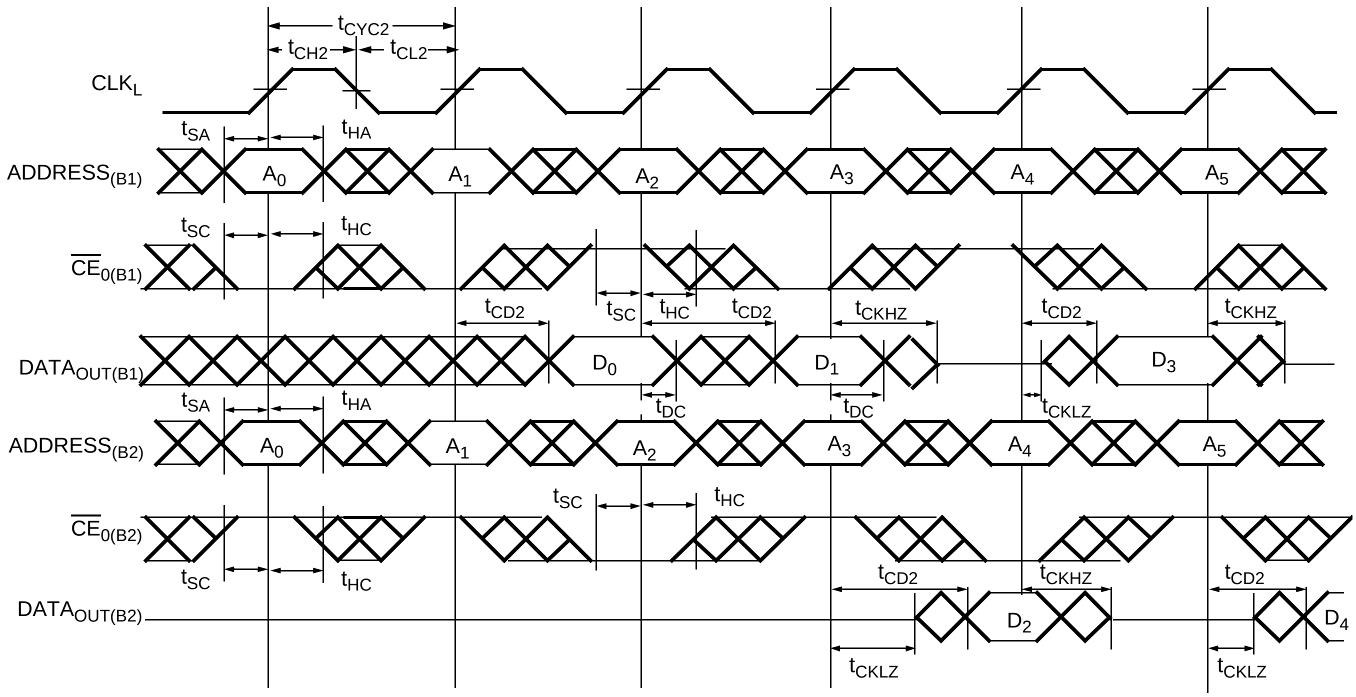
Figure 6. Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE = V_{IH})[19, 20, 21, 22]



Notes
19. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
20. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
21. The output is disabled (high-impedance state) by $\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL} following the next rising edge of the clock.
22. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Figure 7. Bank Select Pipelined Read[23, 24]

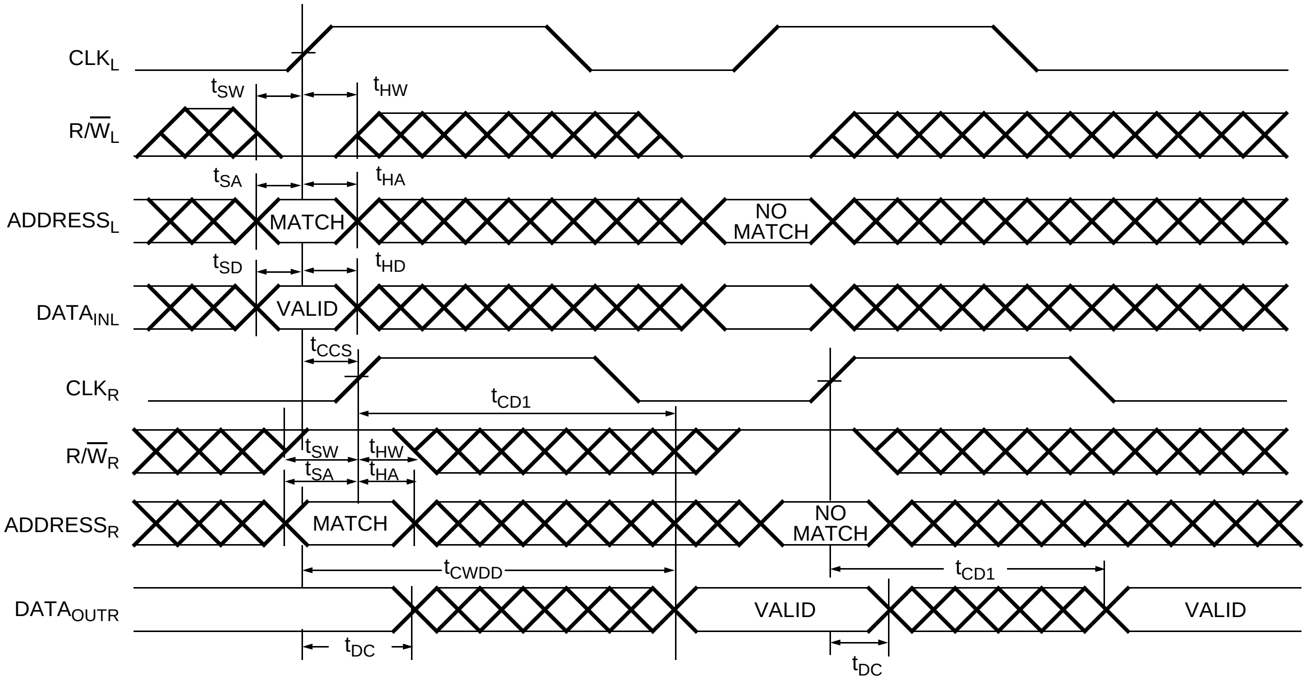


Notes

23. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this datasheet. $\text{ADDRESS}_{(B1)} = \text{ADDRESS}_{(B2)}$.
24. $\overline{\text{OE}}$ and $\overline{\text{ADS}} = V_{IL}$; $CE_{1(B1)}$, $\overline{CE}_{1(B2)}$, R/$\overline{\text{W}}$, $\overline{\text{CNTEN}}$, and $\overline{\text{CNTRST}} = V_{IH}$.

Switching Waveforms (continued)

Figure 8. Left Port Write to Flow-through Right Port Read[25, 26, 27, 28]

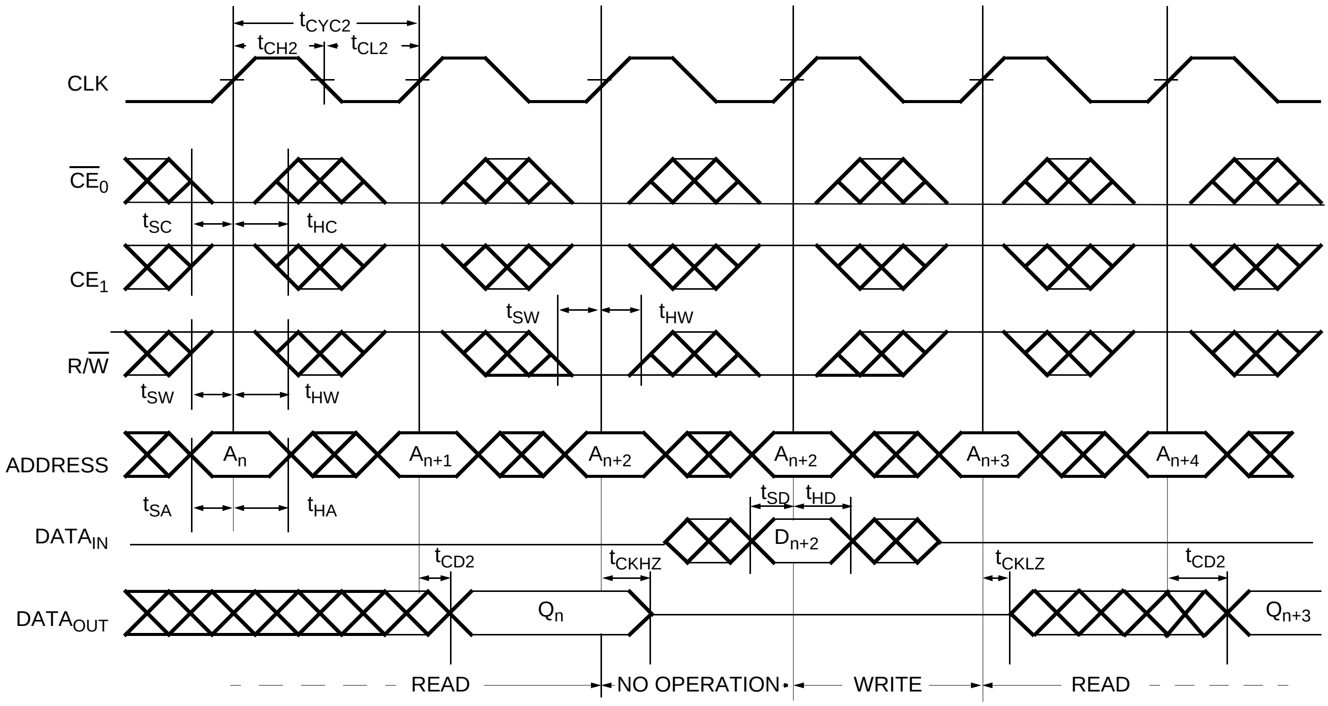


Notes

25. The same waveforms apply for a right port write to flow-through left port read.
26. $\overline{CE}_0$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
27. $\overline{OE}$ = V_{IL} for the right port, which is being read from. $\overline{OE}$ = V_{IH} for the left port, which is being written to.
28. It $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS} > maximum specified, then data is not valid until t_{CCS} + t_{CD1}. t_{CWDD} does not apply in this case.

Switching Waveforms (continued)

Figure 9. Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)[29, 30, 31, 32]



Notes

29. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
30. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
31. $\overline{CE}_0$ and $\overline{ADS} = V_{IL}$; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
32. During “No Operation”, data in memory at the selected address may be corrupted and should be re-written to ensure data integrity.

Switching Waveforms (continued)

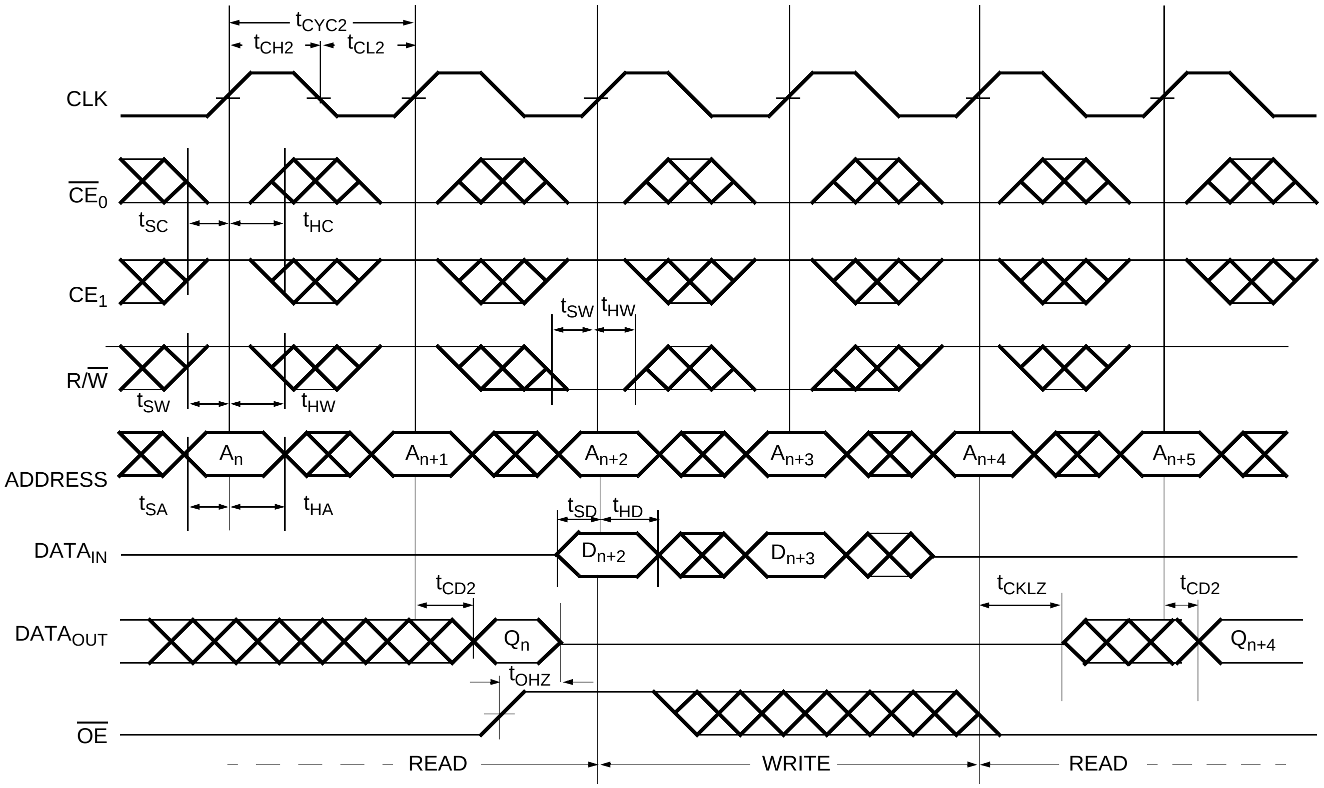


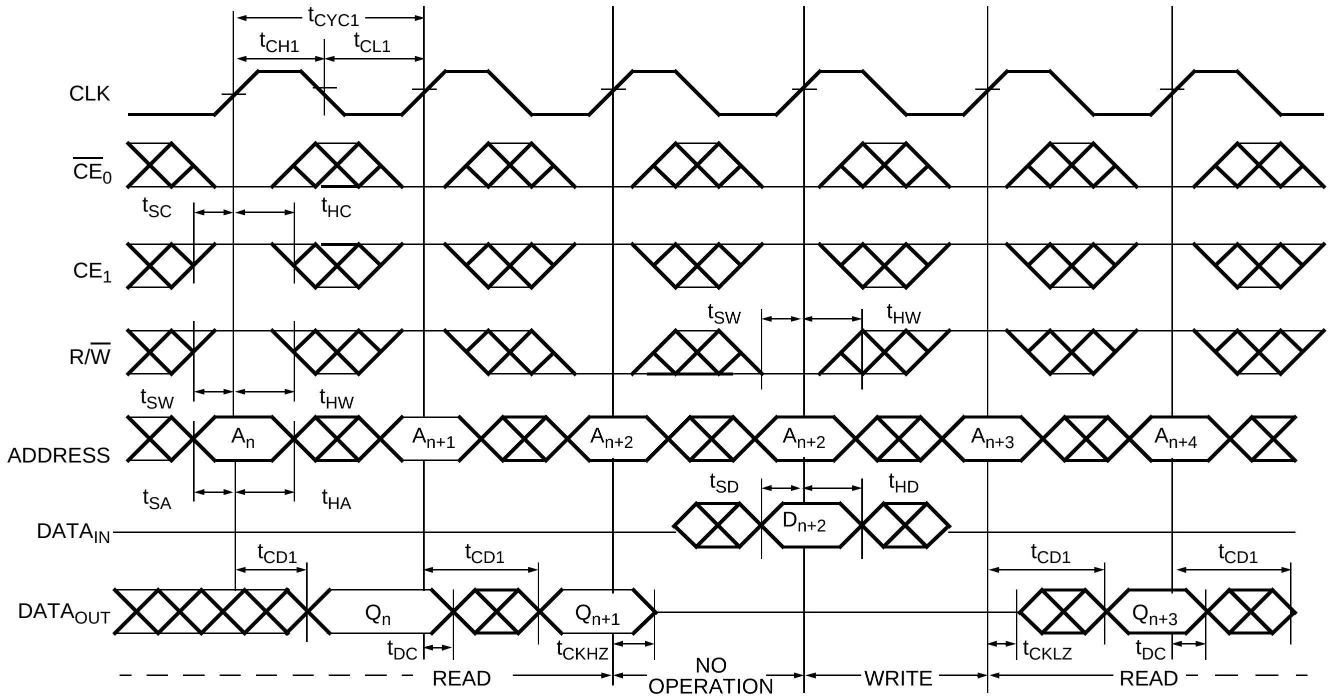
Figure 10. Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)[33, 34, 35, 36]

Notes

33. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
34. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
35. $\overline{CE_0}$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
36. During "No Operation", data in memory at the selected address may be corrupted and should be re-written to ensure data integrity.

Switching Waveforms (continued)

Figure 11. Flow-through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)[37, 38, 39, 40, 41]

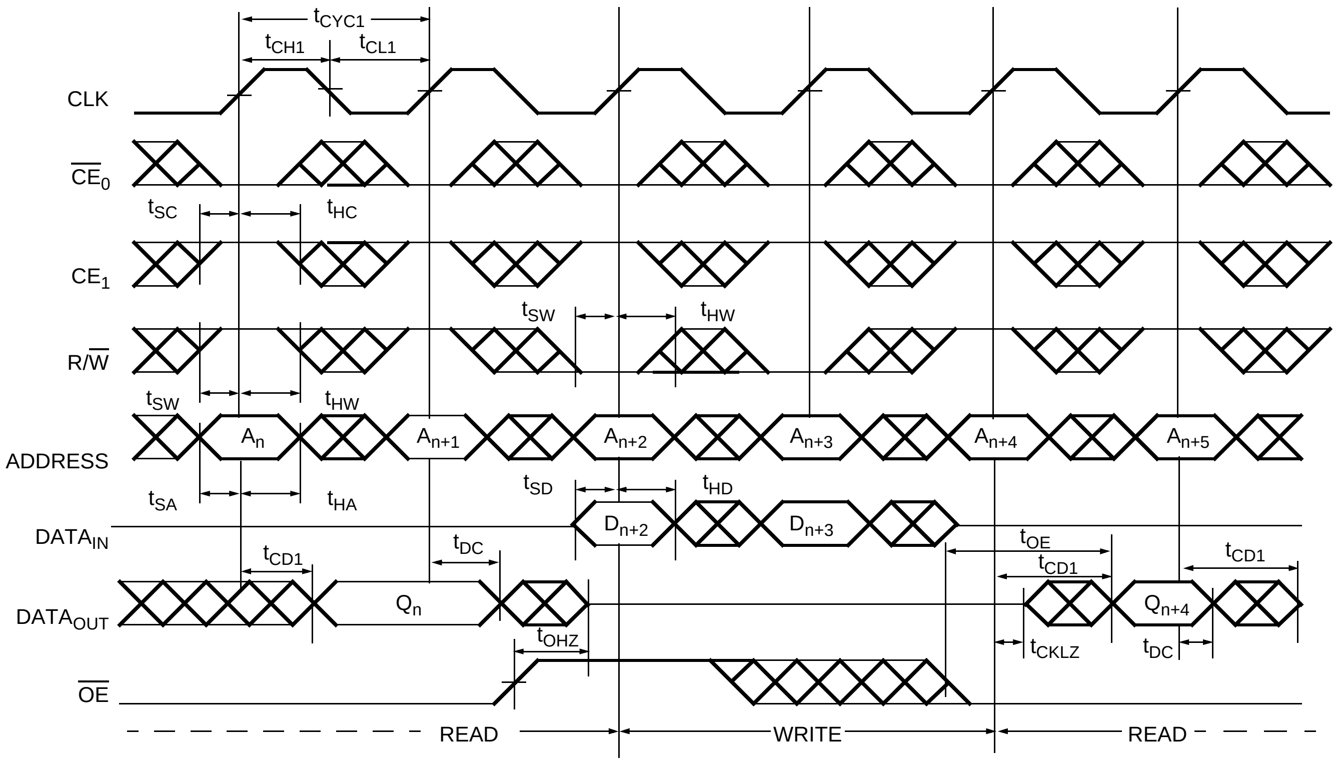


Notes

37. $\overline{ADS} = V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST} = V_{IH}$.
38. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
39. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
40. $\overline{CE_0}$ and $\overline{ADS} = V_{IL}$; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
41. During "No Operation", data in memory at the selected address may be corrupted and should be re-written to ensure data integrity.

Switching Waveforms (continued)

Figure 12. Flow-through Read-to-Write-to-Read ($\overline{OE}$ Controlled)[42, 43, 44, 45, 46]



Notes
42. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
43. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this datasheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
44. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
45. $\overline{CE_0}$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
46. During “No Operation”, data in memory at the selected address may be corrupted and should be re-written to ensure data integrity.

Switching Waveforms (continued)

Figure 13. Pipelined Read with Address Counter Advance[47]

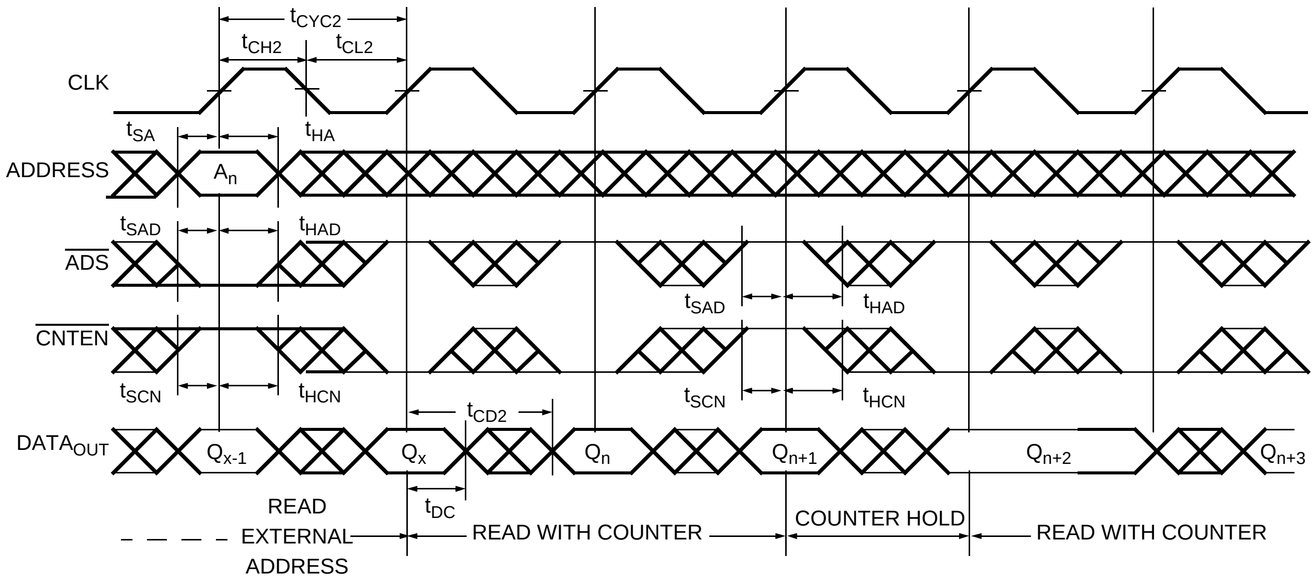
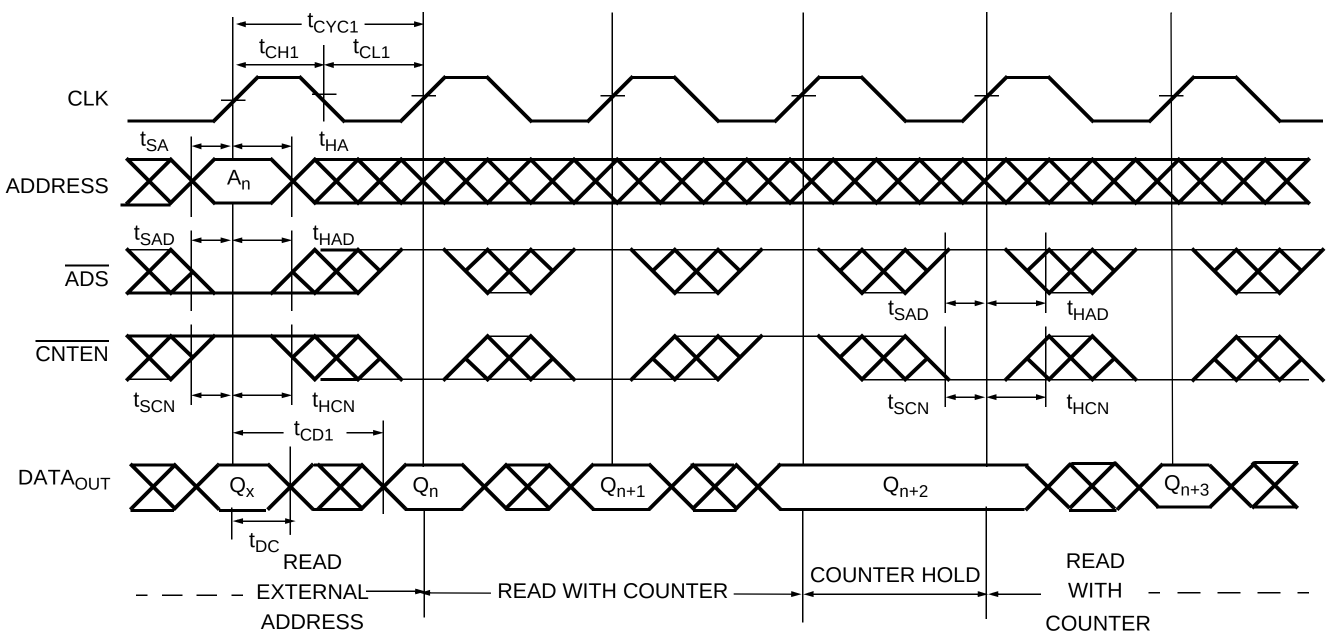


Figure 14. Flow-through Read with Address Counter Advance[47]

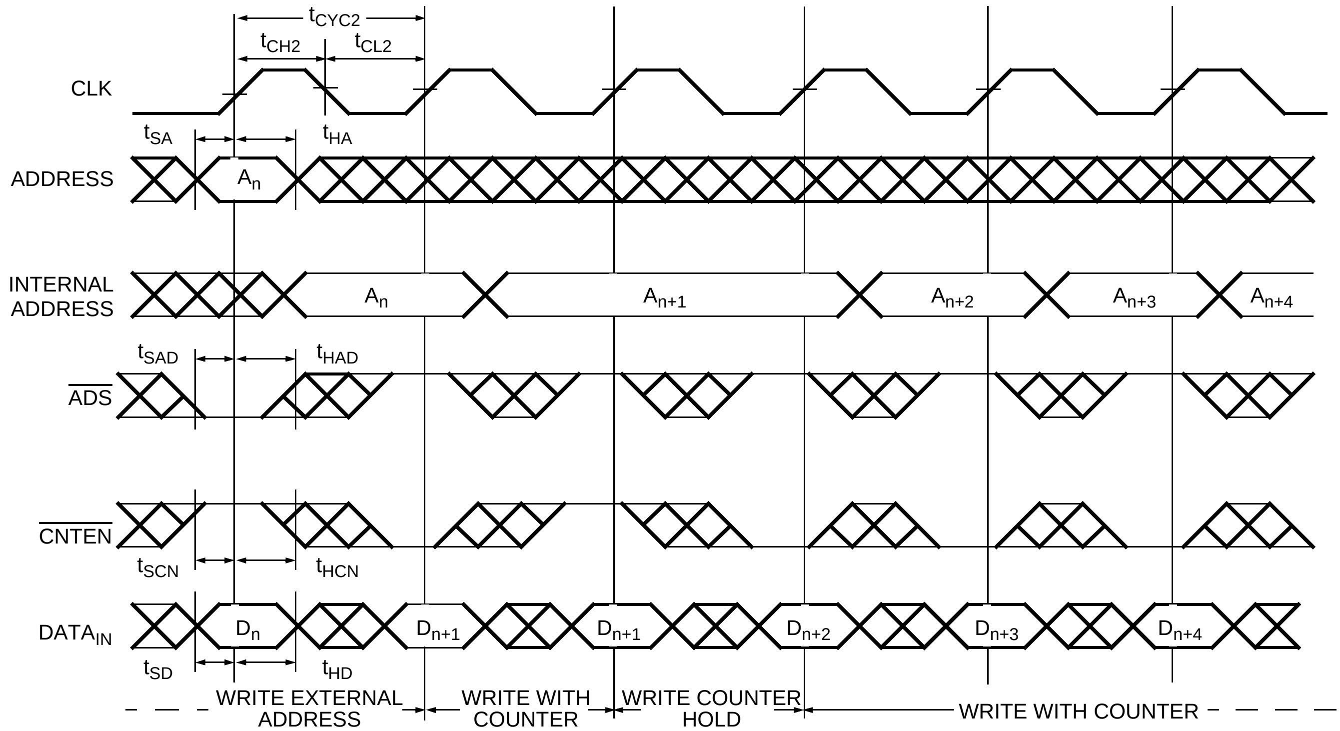


Note

47. $\overline{CE}_0$ and $\overline{OE} = V_{IL}$; CE_1, $R/\overline{W}$ and $\overline{CNTRST} = V_{IH}$.

Switching Waveforms (continued)

Figure 15. Write with Address Counter Advance (Flow-through or Pipelined Outputs)[48, 49]



Notes

48. $\overline{CE_0}$ and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
49. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.

Switching Waveforms (continued)

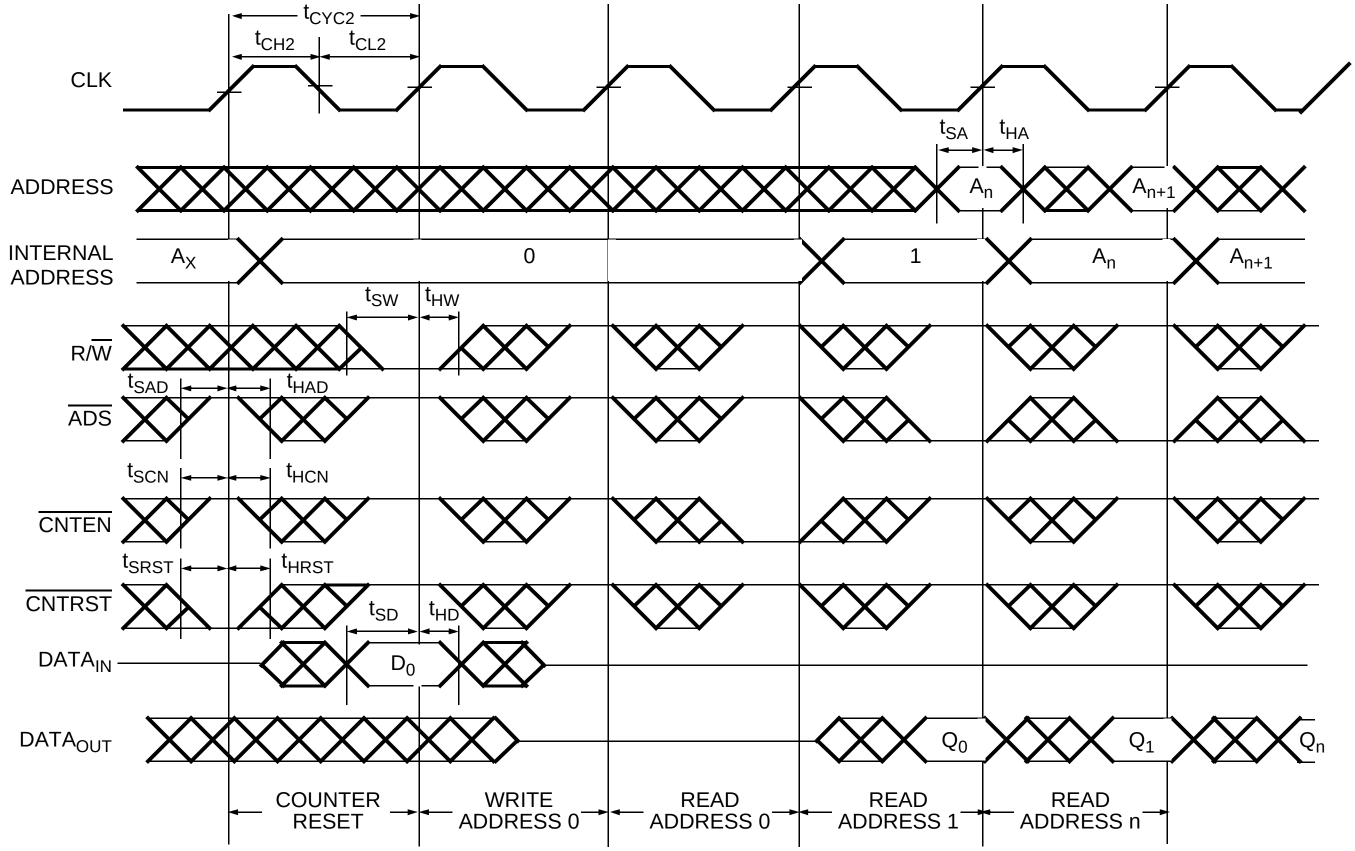


Figure 16. Counter Reset (Pipelined Outputs)[50, 51, 52, 53]

Notes

50. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
51. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
52. $\overline{CE_0} = V_{IL}$; $CE_1 = V_{IH}$.
53. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

Read/Write and Enable Operation[54, 55, 56]

Inputs					Outputs	Operation
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	$R/\overline{W}$	I/O_0–I/O_9	
X	↑	H	X	X	High Z	Deselected[57]
X	↑	X	L	X	High Z	Deselected[57]
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read[57]
H	X	L	H	X	High Z	Outputs Disabled

Address Counter Control Operation[54, 58, 59, 60]

Address	Previous Address	CLK	$\overline{ADS}$	$\overline{CNTEN}$	CNTRST	I/O	Mode	Operation
X	X	↑	X	X	L	$D_{out(0)}$	Reset	Counter Reset to Address 0
A_n	X	↑	L	X	H	$D_{out(n)}$	Load	Address Load into Counter
X	A_n	↑	H	H	H	$D_{out(n)}$	Hold	External Address Blocked—Counter Disabled
X	A_n	↑	H	L	H	$D_{out(n+1)}$	Increment	Counter Enabled—Internal Address Generation

Notes

54. "X" = "Don't Care", "H" = V_{IH}, "L" = V_{IL}.
55. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = "Don't Care."
56. $\overline{OE}$ is an asynchronous input signal.
57. When $\overline{CE}$ changes state in the pipelined mode, deselection and read happen in the following clock cycle.
58. $\overline{CE_0}$ and $\overline{OE}$ = V_{IL}; CE_1 and $R/\overline{W}$ = V_{IH}.
59. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.
60. Counter operation is independent of $\overline{CE_0}$ and CE_1.

Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

128 K × 8 3.3 V Synchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C09099V-12AXC	A100	100-pin Thin Quad Flat Pack (Pb-free)	Commercial

Ordering Code Definitions

CY 7C 09 X X9 V - XX A X X

- Temperature Range: X = C or I
  C = Commercial; I = Industrial
- X = Pb-free (RoHS Compliant)
- Package Type:
  A = 100-pin TQFP
- Speed Grade: 12 ns
- V = 3.3 V
- X9 = Depth: X = 7 or 9;
  9 = 128K
- X = Width: X = 0 or 1
  0 = × 8; 1 = × 9
- 09 = Sync
- 7C = Dual Port SRAM
- Company ID: CY = Cypress Device

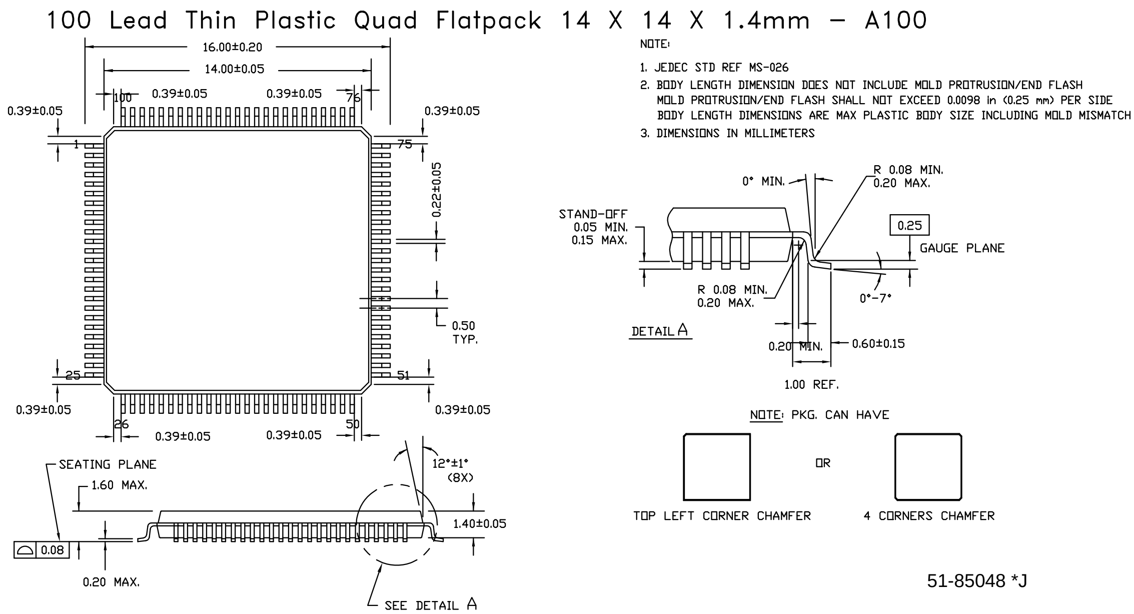
Note

61. See page 8 and page 9 for Load Conditions.

Package Diagram

Figure 17. 100-pin TQFP 14 × 14 × 1.4 mm A100SA, 51-85048

100 Lead Thin Plastic Quad Flatpack
14 X 14 X 1.4mm – A100



51-85048 *J

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microamperes
mA	milliamperes
mm	millimeter
ms	milliseconds
mV	millivolts
ns	nanoseconds
Ω	ohm
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY7C09099V, 3.3 V, 128K × 8 Synchronous Dual-Port Static RAM Document Number: 38-06043				
Rev.	**ECN No.**	**Orig. of Change**	**Orig. of Change**	**Description of Change**
**	110191	SZV	09/29/01	Change from Spec number: 38-00667 to 38-06043
*A	122293	RBI	12/27/02	Power up requirements added to Operating Conditions Information
*B	365034	PCN	See ECN	Added Pb-Free Logo Added Pb-Free Part Ordering Information: CY7C09089V-6AXC, CY7C09089V-12AXC, CY7C09099V-6AXC, CY7C09099V-7AI, CY7C09099V-7AXI, CY7C09099V-12AXC, CY7C09179V-6AXC, CY7C09179V-12AXC, CY7C09189V-6AXC, CY7C09189V-12AXC, CY7C09199V-6AXC, CY7C09199V-7AXC, CY7C09199V-9AXC, CY7C09199V-9AXI, CY7C09199V-12AXC
*C	2623658	VKN/PYRS	12/17/08	Added CY7C09089V-12AXI part in the Ordering information table
*D	2897159	RAME	03/22/10	Removed inactive parts from ordering information table. Updated package diagram. Added Note in ordering information section.
*E	3110406	ADMU	12/14/2010	Updated Ordering Information. Added Ordering Code Definitions.
*F	3264673	ADMU	05/24/2011	Updated Document Title to read “CY7C09099V, CY7C09179V, 3.3 V 32 K/64 K/128 K × 8/9 Synchronous Dual-Port Static RAM”. Updated Features. Updated Pin Configuration (Removed the Note “This pin is NC for CY7C09079V.” in page 5). Updated Selection Guide. Updated Package Diagram. Added Acronyms and Units of Measure. Updated in new template.
*G	3849285	ADMU	12/21/2012	Updated Ordering Information (Updated part numbers). Updated Package Diagram: spec 51-85048 – Changed revision from *E to *G.
*H	4411062	ADMU	06/17/2014	Information for MPNs CY7C09089V and CY7C09199V removed. Information for -6 and -9 speed bins also removed. Updated document title to “CY7C09099V, CY7C09179V, 3.3 V 32K/128K × 8/9 Synchronous Dual-Port Static RAM”
*I	4580622	ADMU	11/26/2014	Added related documentation hyperlink in page 1.
*J	5813056	VINI	07/12/2017	Updated template. Updated Document Title to “CY7C09099V, 3.3 V, 128 K × 8 Synchronous Dual-Port Static RAM”. Updated Features: Removed the reference to CY7C09179V. Updated Pin Configuration: Removed CY7C09179 pin configuration. Updated Ordering Code Definitions. Updated Figure 17 (spec 51-85048 *I to *J) in Package Diagram.

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