Am9582

Disk Data Separator (DDS)

DISTINCTIVE CHARACTERISTICS

- Complete Single-Chip Disk Data Separator for floppy disk and hard disk drives (minimal external components)
- Complete on-chip Phase-Locked-Loop (PLL), frequency may be dynamically changed
- Supports:
  - 1.25 to 5 Mbit/sec MFM data rate for hard disks and also the new high-density Floppy-disk drives
  - 125 to 500 kbit/sec FM data rate for single-density floppy disks
  - 250 to 1000 kbit/sec MFM data rate for double-density floppy disks
- On-chip Write Pre-Compensation Logic (frequency proportional)
- On-chip Address Mark Generator/Detector
- One Am9582 can support both floppy- and hard-disk drives. The on-chip analog section can be dynamically switched between the two modes . No external component needs to be switched.

GENERAL DESCRIPTION

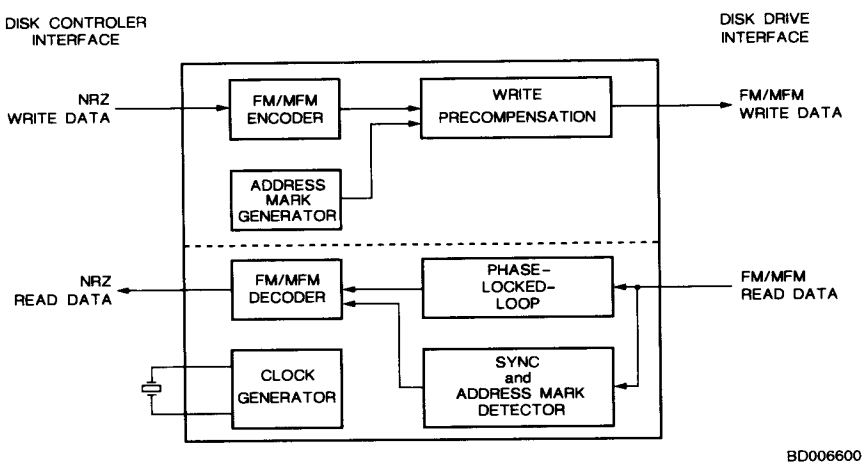
The Am9582 Disk Data Separator (DDS) is a single-chip solution to several functions associated with reading and writing data to systems having floppy- or hard-disk drives. The Am9582 is divided into two basic sections: the Read Section and the Write Section.

The Read Section contains an on-chip Phase-Locked-Loop (PLL) to provide a read clock signal that tracks the FM (Frequency Modulation) or MFM (Modified Frequency Modulation) serial data from the disk. The MFM or FM data is then fed into the MFM/FM decoder to be converted into NRZ (Non Return to Zero) data. A built-in Address Mark detector recognizes the standard address marks for both floppy and hard disks.

The Write Section contains an encoder which encodes the incoming NRZ data and the write (reference) clock into a single stream of either FM or MFM encoded data. The Write Section also contains an Address Mark generator and the Write Pre-Compensation Logic. This Address Mark generator can generate the standard Address Marks for both floppy- and hard-disk data formats. Write Pre-Compensation compensates bit-shifting caused by the characteristics (pulse superpositioning) of the magnetic media.

The Am9582 is the companion device for the Am9580A/90 Hard Disk Controller. This chip set provides a complete disk-controller solution to interface systems with ST506- or ST412-type hard-disk drives and floppy-disk drives. Also, the Am9582 can be integrated on disk drives offering a NRZ data interface (e.g., ESDI or SMD) to implement the on-drive data separator functions (MFM) or the PLL functions (RLL).

BLOCK DIAGRAM



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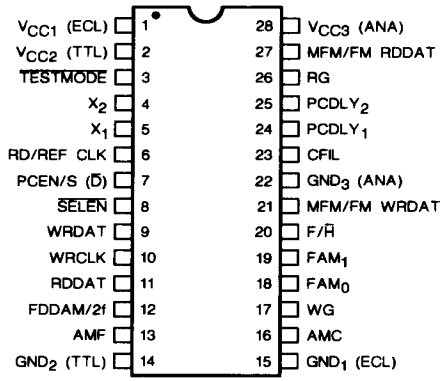
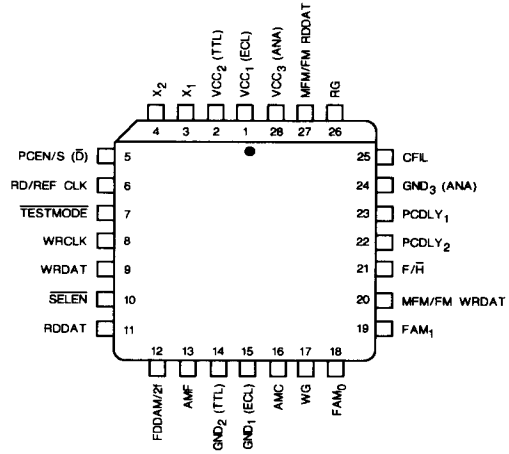
CONNECTION DIAGRAMS
Top View



CD010091



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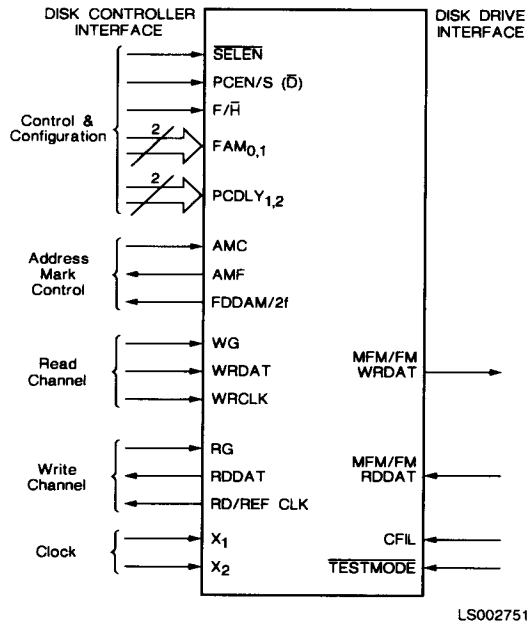
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



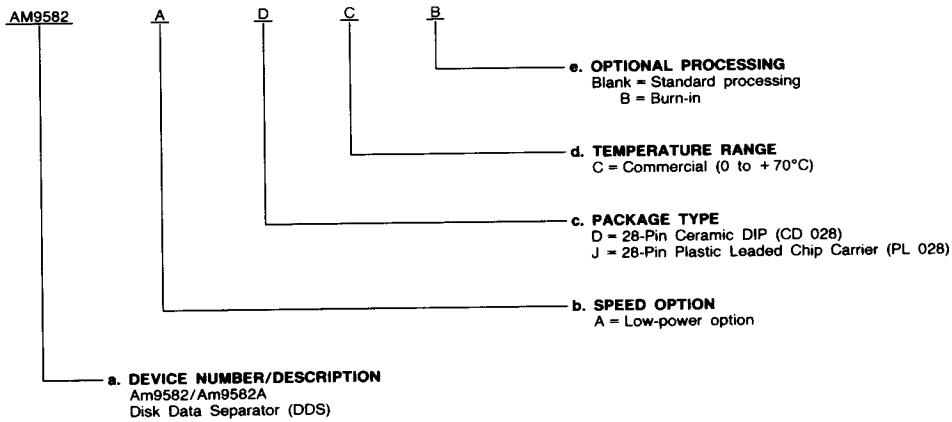
LS002751

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM9582	DC, DCB
AM9582A	DC, DCB, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

AMC Address Mark Control (Input)
This control input line is used to generate and write the Address Marks during a WRITE operation (with WG) and detect the Address Marks during a READ operation (with RG).

AMF Address Mark Found (Output, Three-state, Active HIGH)
During a write operation, AMF acknowledges that the Address Mark has been completely generated. With the first clock after AMF has been activated, the Am9582 latches the data bit following the Address Mark. During a read operation, AMF acknowledges that an address mark of the requested kind has been found. The Am9582 synchronously strobes out AMF and the first data bit following the Address Mark.

CFIL Filter Capacitor (Input; Analog)
A 33-nF filter capacitor (approx.) is connected between this pin and GND_3 (analog ground).

FAM_1, FAM_0 Floppy Address Mark Select (Inputs)
These two inputs select the Address Mark to be processed. These inputs are further qualified by F/$\overline{H}$ and PCEN/S($\overline{D}$). They also set up the Am9582 to support RLL code, clock dump, and data dump modes for MFM (see Table 1).

FDDAM/2f Floppy Deleted Data Address Mark/2f (Output; Three State)
In single-density floppy mode, this output indicates that the Am9582 has detected a Deleted Data Address Mark. During read operations, FDDAM is valid while AMF is asserted. In double-density or hard disk mode, or during write operation, FDDAM is LOW (Inactive). FDDAM2f is three-stated when $\overline{SELEN}$ is HIGH (Inactive). In RLL mode this output provides twice the read clock (2f clock) which is synchronous to RDDAT.

F/$\overline{H}$ Floppy/$\overline{Hard}$ Disk (Input)
When this input is HIGH, the Am9582 controls single- or double- density floppy-disk drives (selected by PCEN/S($\overline{D}$). When this input is LOW, the Am9582 controls hard disks. In combination with FAM_1 and FAM_0, this input also selects the type of Address Mark to be generated or detected. The selection criteria are listed in Table 1.

$PCDLY_1$, $PCDLY_2$ Pre-Compensation Delay (Inputs; Analog)
The ratio of the resistor connected between $PCDLY_1$ and V_{CC3} (R_1), and $PCDLY_2$ and V_{CC3} (R_2) sets the Pre-Compensation Delay as a fraction of the reference clock cycle time. The range of the Pre-Compensation Delay can be set from 1% to 20% of the bit cell time with an accuracy of ±5% of the chosen value. The minimum Pre-Compensation Delay can be set to 2 ns. Figure 6 gives the typical resistor values.

These inputs must not be left open. Open inputs disturb the operation of the on-chip PLL and thereby affect both the read and the write logic. If Pre-Compensation is not enabled, these inputs may be directly connected to V_{CC}.

PCEN/S($\overline{D}$) Pre-Compensation Enable/Single($\overline{Double}$) Density (Input)
This input implements two functions which are multiplexed. The Am9582 latches the level on this input with the falling edge of $\overline{SELEN}$. A HIGH selects single-density operation; a LOW selects double-density operation.

During a write operation, this input enables/disables the Write Pre-compensation Logic. If the input is LOW, the write data is not altered. If this input is HIGH, the Write Pre-Compensation Logic is activated. Pulses in the encoded data stream which are apart are moved even further apart. The degree of compensation is adjusted by the Pre-Compensation Delay inputs. For single-density operation, PCEN is ignored and the Write Pre-Compensation Logic is disabled.

RD/REF CLK Read/Reference Clock (Output; Three State)
During a read operation (RG Active), RD/REF CLK is the read clock derived from the encoded disk data signal on MFM/FM RDDAT. The disk controller should use this clock to sample the read data (RDDAT). When the system is not performing a read operation (RG Inactive), RD/REF CLK is the reference clock derived from the reference frequency supplied from X_1 and X_2. The switching from RDCLK to REF CLK is a glitch-free operation. This output is three-stated when $\overline{SELEN}$ is HIGH (inactive).

In RLL mode this output only provides the reference clock (not the read clock). For write operations this clock or the 2f clock can be used to clock the encoder. For read operations the decoder is clocked by the read clock (2f clock).

$\overline{SELEN}$ $\overline{Select\ Enable}$ (Input; Active LOW)
When $\overline{SELEN}$ is LOW (Active), all three-state outputs are enabled. The falling edge of $\overline{SELEN}$ latches the status of PCEN/S($\overline{D}$) to determine single- or double-density floppy operation. If the Am9582 only controls hard-disk drives (F/$\overline{H}$ tied LOW), $\overline{SELEN}$ may be tied LOW permanently.

$\overline{TESTMODE}$ Testmode (Input; Active LOW)
This input is used to test the Am9582 logic independent of the internal PLL. This input should be tied HIGH for normal operation. It is used for test purposes only.

X_1, X_2 Crystal Oscillator 1, 2 (Inputs)
An external crystal is connected to these two inputs (see Figure 7). Alternatively, a TTL-compatible clock may be connected to X_1 with X_2 tied to GND_3 (Analog GND). Table 1 specifies the crystal frequency for various operating modes. In floppy modes, the crystal frequency is divided down internally (by 16 or 32). This allows the crystal oscillator to operate between 4 and 16 MHz. This frequency interval covers applications ranging from 125 kbit/sec single-density floppy disks (4 MHz/32) up to 5 Mbit/sec hard disks (5 MHz/1).

Write Section

MFM/FM WRDAT MFM/FM Write Data (Output; Three State)
MFM/FM Write Data is encoded data output to the disk drive. The MFM format is used for single-density floppy disks. This output is three-stated when $\overline{SELEN}$ is HIGH (Inactive).

WG Write Gate (Input; Active HIGH)
When WG is HIGH the write logic is enabled. This input should be connected to the write gate output of the disk controller.

WRCLK Write Clock (Input)
This clock is typically connected to the RD/REF CLK output of the Am9582. WRDAT must satisfy the setup and hold time requirements with respect to WRCLK. In applications where the data separator and the disk controller are

physically separated (e.g., ESDI), this input should be connected to the write clock output of the disk controller (e.g., the Write Clock of the ESDI interface). This connection minimizes the skew between clock and data.

WRDAT Write Data (Input; Active HIGH)
This input receives the NRZ Write Data from the disk The controller. Am9582 samples this input with WRCLK (Write Clock).

Read Section

MFM/FM RDDAT MFM/FM Read Data (Input; Active HIGH)
This input provides the encoded data read from the disk. The Am9582 internally separates clock and data information of the encoded MFM/FM RDDAT and restores it to the original NRZ format (RDDAT) which is sent to the disk controller.

RDDAT Read Data (Output; Active HIGH)
This output provides the decoded NRZ data for the hard disk controller. In RLL mode the data is not decoded; the Am9582 directly passes the MFM/FM RDDAT to the RDDAT to the RDDAT output. No internal processing takes place.

RG Read Gate (Input; Active HIGH)
When RG is HIGH (Active) the read section of the Am9582 is enabled. The internal PLL (Phase-Locked-Loop) will lock up to the incoming encoded data stream. When AMC is activated the Am9582 is armed to search for Address Marks. After one Address Mark is found. RG must be pulsed LOW. This pulse resets the internal logic to prepare it for another synchronization and Address Mark search. A subsequent assertion of RG commands the internal PLL to again lock up to the data stream. RG and WG must not be active simultaneously.

GND_1 ECL Ground Potential (0 V)

GND_2 TTL Ground Potential (0 V)

GND_3 Analog Ground Potential (0 V)

V_{CC1} ECL Power Supply (+5 V)

V_{CC2} TTL Power Supply (+5 V)

V_{CC3} Analog Power Supply (+5 V)

FUNCTIONAL DESCRIPTION

The Am9582 is a highly integrated single-chip data separator for both floppy- and hard-disk drives which use FM or MFM codes. Data separation is the re-generation of a reference clock from an incoming bit steram (read data) and the use of that clock to separate out serial NRZ data. The coding rules for both FM and MFM defines a unit of time as a bit cell.

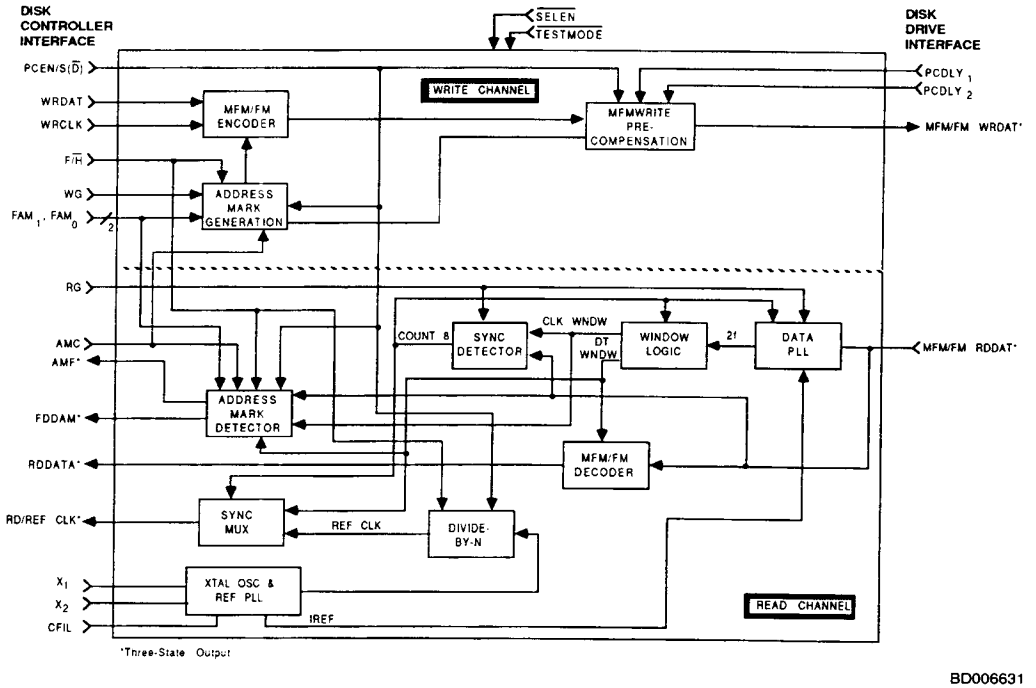


Figure 1. Detailed Block Diagram

FM Coding

The FM (or single-density) encoder generates one or two pulses per bit cell. The coding rules for FM are as follows:

- Each bit cell starts with a clock pulse.
- If a "1" (WRDAT HIGH) is to be strobed, a second pulse is generated in the middle of the bit cell. A "0" (WRDAT LOW) is represented if no pulse is in the middle of the bit cell.

Each pulse causes a flux transition on the magnetic storage media. The maximum flux transition density is media dependent.

This encoding scheme is called FM (Frequency Modulation) because the frequency of the encoded data signal is data dependent. The signal frequency of a sequence of "1"s is twice as high as the signal frequency of a sequence of "0"s.

MFM Coding

In the FM encoding scheme a bit cell accommodates up to two flux transitions — A first flux transition of the mandatory clock and an optional second flux transition if the NRZ data is "1". However, all clock flux transitions are redundant.

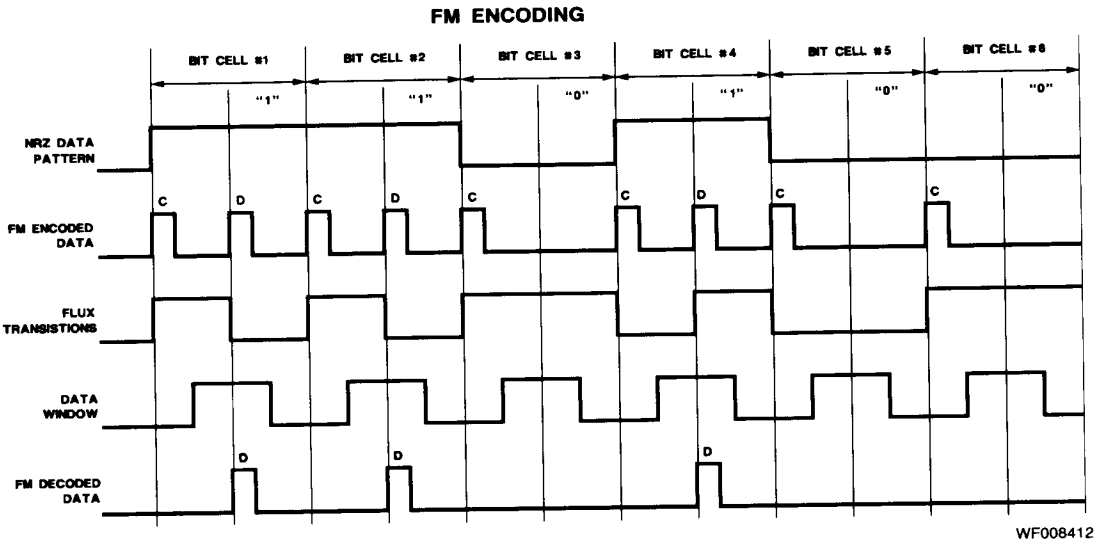
MFM (Modified Frequency Modulation) uses the flux transitions more efficiently. Here each bit cell accommodates, at most, one flux transition. Hence, MFM recording doubles the data capacity over FM recording without increasing the flux transiton density.

The rules for MFM encoding are as follows:

- Generate a pulse in the middle of the bit cell (data pulse), if a "1" is to be stored.
- Generate a pulse in the beginning of the bit cell (clock pulse), if a "0" is to be stored and the preceding bit cell also stores a "0".
- If the current bit cell stores a "0", and the preceding bit cell stores a "1", the current bit cell does not accommodate any pulses.

Because the MFM encoding only generates one flux transition per bit cell, the bit cell can be reduced to one-half of the FM bit cell, keeping the flux transition density constant. This doubles the data capacity of the disk compared to FM encoding.

For both encoding schemes the data separator regenerates a disk window which covers the position of the data pulse. For a constant flux transition rate, the MFM data window is half the size of the FM data window. This means that MFM recording demands more sophisticated data separators than FM recording.



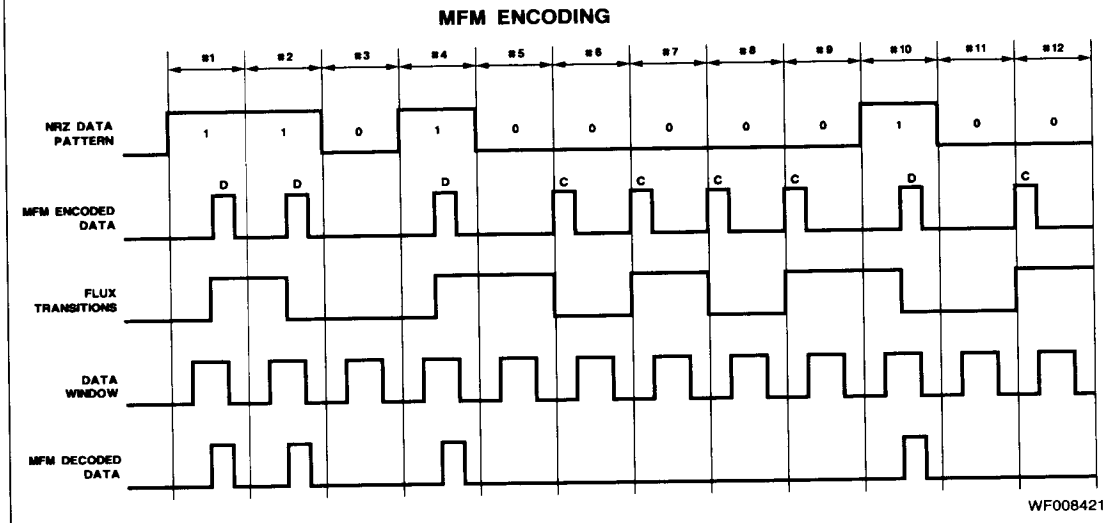


Figure 2. FM vs. MFM Encoding*

*Note: MFM encoding doubles the bit density on the disk by replacing clock bits (C) used in FM encoding with data bits (D). MFM encoding reduces the bit cell by one half.

PLL Operation

The on-chip PLL regenerates the read clock from the encoded data read from the disk. It operates by comparing the input data with a reference signal generated by a Voltage Controlled Oscillator (VCO). If the input transitions and the VCO transitions match, the loop is said to be in lock. If these sets of transitions do not match (coincide in time), then a correction signal is generated by the phase detector and is sent to the VCO to modify its output. Standard phase detectors expect a one-to-one correspondence between input transitions and VCO transitions. A disk data stream, however, contains missing pulses. If this bit stream is directly applied to the phase detector, it gives an erroneous output. For example, a repeated "...1010..." pattern would cause a standard PLL to lock to half of the frequency because only half the number of transitions exist in the bit stream.

Two approaches can correct this PLL behavior:

First, the phase detector performs a phase comparison only if a data pulse is present (i.e., within one-half bit cell time of a VCO edge). Generally this arming function involves two data

paths to the phase detector: a "prompt" path and a "delayed" path. The "prompt" path enables the phase detector for a phase comparison, which is then done by using the "delayed" path. The drawback of this scheme is that the delay must be proportional to the data rate and it requires external components such as delay lines or one-shots.

The second employs the Am9582 that integrates a proprietary PLL not sensitive to missing pulses, and requires only a minimum number of non-adjustable external components.

External Components

With the exception of a single, non-critical filter capacitor (33 nF approx.) used in the Reference PLL, all capacitors are integrated onto the Am9582.

Mixed Control of Floppy- and Hard-Disk Drives

Because all PLL parameters are adjusted automatically, one Am9582 can provide the control for both floppy- and hard-disk drives. No external components need to be switched assuming that the relative Pre-Compensation value for floppy- and hard-disk mode is identical (e.g., 1% to 20% of bit cell time). In this mixed mode it is suggested that no on-chip crystal oscillator is used. Instead, a switchable (e.g., 4 MHz for 250 kbit/sec MFM floppy-disk data rate and 5 MHz Mbit/sec MFM hard-disk data rate) TTL clock source should be connected to X_1. In this mode, X_2 is connected to GND_3 (analog ground).

Write and Read Sections

The Am9582 is divided into two basic sections — the Write Section and the Read Section. Both sections operate independently, but not concurrently.

Write Section

The Write Section encodes the NRZ data stream supplied on WRDAT into the FM or MFM format; it generates the Address Marks and it performs the optional Pre-Compensation of the MFM data.

TABLE 1. ADDRESS MARK SELECTION AND FREQUENCY SELECTION

F/$\overline{H}$	PCEN/S($\overline{D}$)	FAM_1	FAM_0	Address Mark Selected	Mode	XTAL FREQ
1	1	0	0	Index (IXAM)	FM Floppy	32 x Bit Rate FREQ
1	1	0	1	ID (IDAM)	FM Floppy	
1	1	1	0	Data (DAM)	FM Floppy	
1	1	1	1	Deleted Data (DDAM)	FM Floppy	
1	0	0	0	Index (IXAM)	MFM Floppy	16 x Bit Rate FREQ
1	0	1	0	ID or Data	MFM Floppy	
0	X	0	0	Normal A1 Address Mark	MFM Hard Disk	Bit Rate FREQ
0	X	1	1	Any Apparent Address Mark	Dump Clock** — Hard Disk	Bit Rate FREQ
0	X	1	0	None	RLL Hard Disk	Code Rate FREQ*
0	X	0	1	Any Apparent Address Mark	Dump Data — Hard Disk	Bit Rate FREQ
1	0	0	1	Any Apparent Address Mark	Dump Data — Floppy Disk	16 x Bit Rate FREQ
1	0	1	1	Any Apparent Address Mark	Dump Clock — Floppy Disk	16 x Bit Rate FREQ

* Code Rate Frequency = "2f" frequency of PLL.

**Dump is a mode whereby data (or clock) is passed to the disk controller on an apparent start of Address Mark (end of apparent Sync Field). This is to enable the recovery of sectors which could not otherwise be read due to corruption of the Address Mark.

Address Mark Generation

Each sector on the disk contains two Address Marks. They mark the start of the header and the data field. For MFM floppy and in hard-disk mode, these Address Marks are identical. For FM floppy-disk mode, these Address Marks are different (see Table 2). To make the Address Marks unique and always distinguishable from all possible data patterns, the encoding rules (either for FM or MFM) are deliberately violated when an Address Mark is generated. This is done by deleting some of the clock bits in the encoded clock/data pattern. When a sector is read back from the disk, these missing clocks are detected and the disk controller is assured that correct synchronization has taken place.

The Am9582 generates all the standard IBM Address Marks for floppy (IBM) format and hard disk (ST506/SA1000) formats. Address Mark Control (AMC) is sampled on the rising edge of WRCLK when a Write operation is taking place. The appropriate Address Mark is then inserted. At completion, Address Mark Found (AMF) is brought HIGH is acknowledgement.

The type of Address Mark generated is dependent on FAM_0, FAM_1, and the operating mode (i.e., floppy or hard, and single- or double-density). The type of Address Mark selected is listed in Table 1.

TABLE 2. ADDRESS MARKS FOR VARIOUS OPERATING MODES

SINGLE DENSITY FLOPPY

TYPE	Data Pattern	Clock Pattern	Number of Bytes
IXAM	FC	D7	1
IDAM	FE	C7	1
DAM	FB	C7	1
DDAM	F8	C7	1

DOUBLE DENSITY FLOPPY*

TYPE	Data Pattern	Clock Pattern	Number of Bytes
IXAM	C2	14	3
DAM and IDAM	A1	0A	3

HARD DISK*

TYPE	Data Pattern	Clock Pattern	Number of Bytes
DAM and IDAM	A1	0A	1

*Note: 1. The ID Address Marks and Data Address mark for double density floppy and hard disks are normally qualified by an extra byte following the Address Mark. However, these extra bytes are normally encoded (no missing clocks), which the controller can easily detect during a READ operation.

Write Pre-Compensation

Bit shifting is a phenomenon caused by the flux changes stored on the disk that interact with each other. Nearby flux changes move away from each other, creating a timing uncertainty that can cause errors when data is read. This phenomenon is more significant on the inner tracks of a disk because the flux changes are physically closer.

To overcome this interaction between flux transitions, the Write Data stream is pre-compensated; i.e., the direction of each bit shift is anticipated and the bit is moved in the opposite direction by the Am9582 before being written to the disk. When PCEN is HIGH, Pre-Compensation is enabled and each bit will be made either Early, Nominal, or Late, depending on its interaction with neighboring bits (in FM mode, PCEN has no effect). The amount of time shift between Nominal and Late is set by two external resistors on the PCDLY pins. The Pre-Compensation procedure is shown in Figures 3 and 4.

If Pre-Compensation is enabled, the pulse width of the Early and Nominal pulses are extended (see Figure 4). The rising edges of the Early, Nominal, and Late pulses show the actual Pre-Compensation. Therefore, the rising edge of Write Data should generate a flux transition on the disk drive. The falling edges of Early, Nominal, and Late are always aligned (no Pre-Compensation) and therefore should not be used.

If Pre-Compensation is not used, $PCDLY_1$ and $PCDLY_2$ should still be connected to Analog V_{CC} (V_{CC3} (either directly or via pullup resistors), for proper Reference PLL operation (required for Read and Write Sections).

For RLL codes, NRZ to RLL encoding, Write Pre-Compensation and Address Mark Detection have to be performed by an external circuitry.

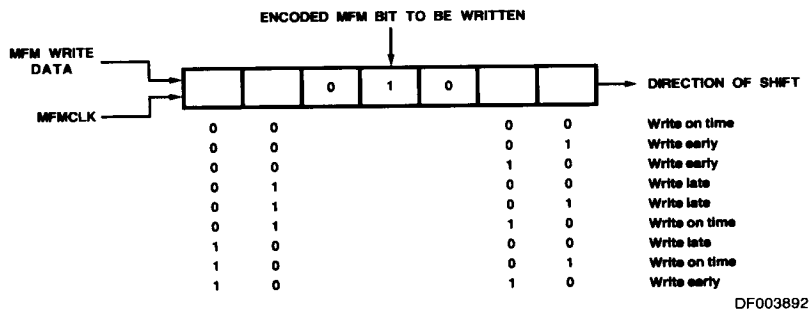
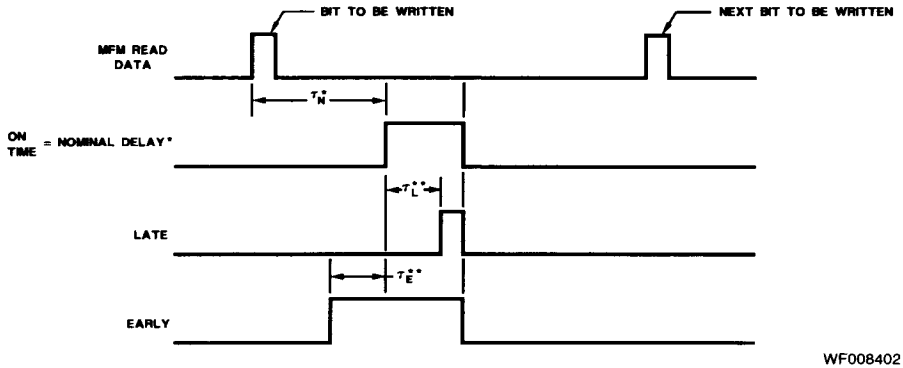


Figure 3. Write Pre-Compensation



*Nominal Delay = τ_N
**$\tau_L = \tau_E$ = 1% – 20% bit cell time

Figure 4. Bit-Shifting for Write Pre-Compensation

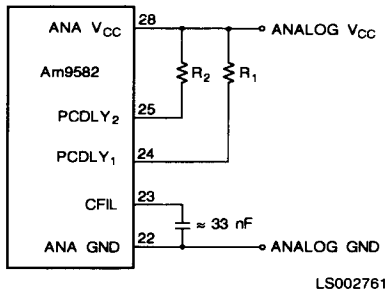
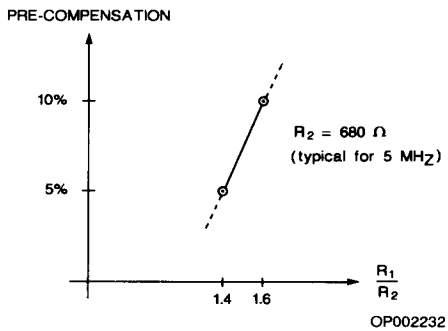


Figure 5. Discrete Components Connection



R_1 = 1K nominal; R_2 = 680 nominal

Figure 6. Suggested Resistor Values for Pre-Compensation

Read Section

The Read Section of the Am9582 consists of a data Phase-Locked Loop (PLL), Window Logic, Sync Field Detector, Address Mark Detector, MFM/FM Decoder, Synchronized Multiplexer, crystal controlled oscillator, a Reference PLL, and a Divide-by-N counter as shown in Figure 1.

Phase-Locked-Loop (PLL)

The main function of the data PLL is to provide a clock signal (shown as 2f in Figure 1) that closely tracks the MFM/FM serial data read from the disk. The 2f signal is then used to generate clock and data windows.

When the chip is in the write mode (WG Active), the PLL is synchronized to the REF CLK derived from the crystal-controlled oscillator. When data is read from the disk (RG Active), the PLL is locked to the data stream from the disk.

In RLL mode the Am9582 provides the 2f signal on the FDDAM/2f output. In this mode RD/REF CLK always provides the reference clock and therefore should not be used (see Pin Description).

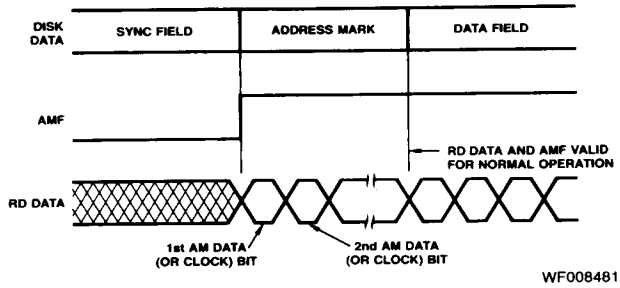


Figure 7. Dump Mode

Sync Field and Address Mark Detector

The Sync Field Detector looks for the sync field consisting of eight consecutive pulses in clock windows generated by the on-chip PLL. When this pattern is detected, the window signal polarity will be frozen. If the sync pattern is not found, the Am9582 flips the window polarity so that the Sync Detector can continue to look for the sync pattern. The apparent sync field ending is seen as a pulse in the Data Window. This action arms an Address Mark time out; i.e., after eight bit cells (or twenty-four bit cells for double-density floppy mode) an Address Mark must be found or the Am9582 is reset back to the lowest level of search where it looks for eight apparent zeros.

The detection of various Address Marks for floppies and hard disks is performed by the Address Mark Detector. The type of Address Mark detected is determined by the signals S($\overline{D}$), F/$\overline{H}$, FAM_0 and FAM_1, as shown in Table 1. In response to an active AMC, AMF will be asserted to indicate that the desired Address Mark has been found during a read operation, or an appropriate Address Mark has been written during a write operation. FDDAM is asserted in the FM floppy mode upon detection of a Floppy Deleted Data Address Mark during a Read.

Address Mark Recovery with Media Defects

In the normal operating mode the Am9582 will only detect an Address Mark if all eight/twenty-four bits match the selected Address Mark (see Table 1). In the clock/data dump mode the Am9582 can assist in the detection of damaged Address Marks. Here the Am9582 will assert AMF (Address Mark Found) as soon as it detects the first data bit (pulse in the Data Window) (see Figure 3). Selectively, the Am9582 then provides either the clock pattern which should show the missing clock (coding violation within the Address Mark) (clock dump mode) or the Address Mark data (data dump mode).

MFM/FM Decoder

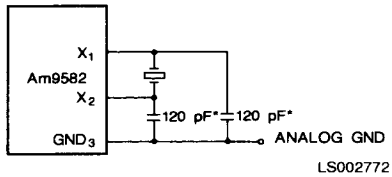
The MFM/FM Decoder converts the incoming MFM/FM serial data from the disk to NRZ data for the disk controller. If an MFM/FM pulse occurs in a Data Window, the NRZ data is decoded as a "1". If no pulse occurs in the Data Window, the NRZ data is decoded as a "0".

The RD/REF CLK pin outputs either the REF CLK derived from the crystal-controlled oscillator or the RDCLK derived from disk data. The Am9582 outputs REF CLK while writing and also while reading, until a sync field has been detected. Once the sync field is detected, the RD/REF CLK output switches over to the RDCLK without any glitches. For RLL hard disks, this output is always REF CLK.

Clock Generator

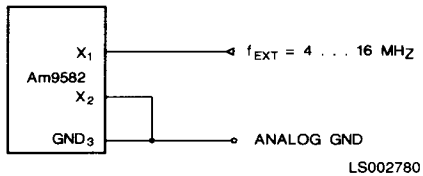
The clock Generator consists of a crystal-controlled oscillator and a frequency divider. The oscillator frequency is determined by the X_1 and the X_2 inputs (crystal or TTL-level clock source). The frequency divider divides the oscillator frequency to generate the REF CLK. The appropriate divide ratio is selected internaly, as shown in Table 1.

When the Am9582 is not reading from the disk, REF CLK keeps the PLL at the center of its tuning range. When the Am9582 is reading (RG HIGH), the PLL locks to the frequency of the data coming from the disk. When the Am9582 is writing (WG HIGH), REF CLK is output to the disk controller to provide the reference clock (Write Clock) for the write operation.

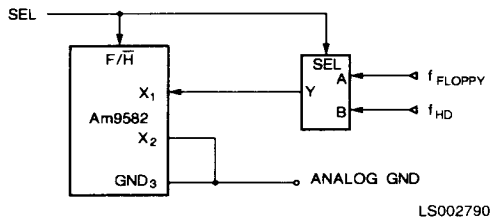


*Typical value for 5 MHz operation

Crystal Mode



External Frequency Mode



Mixed Mode (Floppy/Hard Disk)

Figure 8. Crystal Oscillator Interfacing

Write Pre-Compensation

The Am9582 performs Write Pre-Compensation for MFM encoded data only. FM encoded data do not require Pre-Compensation. The bit to be written is shifted early, or late, with respect to a nominal delay. The Am9582 selects nominal delay if data is to be written without delay, and examines an internal 7-bit register that the MFM encoded data is to be passed through.

Printed-Circuit-Board Layout Guidelines

The Am9582 contains PLL circuitry which requires a noise-free power supply to operate correctly. Therefore, Analog V_{CC} and GND should be connected to the power connector via separate supply lines. They should not be connected directly to the GND and V_{CC} plane of a multi-layer PC board. These supply lines should have separate bypass capacitors which are as close as possible to the supply inputs.

The filter capcacitor (CFIL) should be connected between the CFIL input of the Am9582 and Analog GND. The Pre-Compensation Delay resistors should be connected to Analog V_{CC}.

The crystal should be as close as possible to the crystal oscillator inputs of the Am9582 (X_1 and X_2). The two crystal capacitors should be connected to Analog GND (see Figure 7).

APPLICATIONS

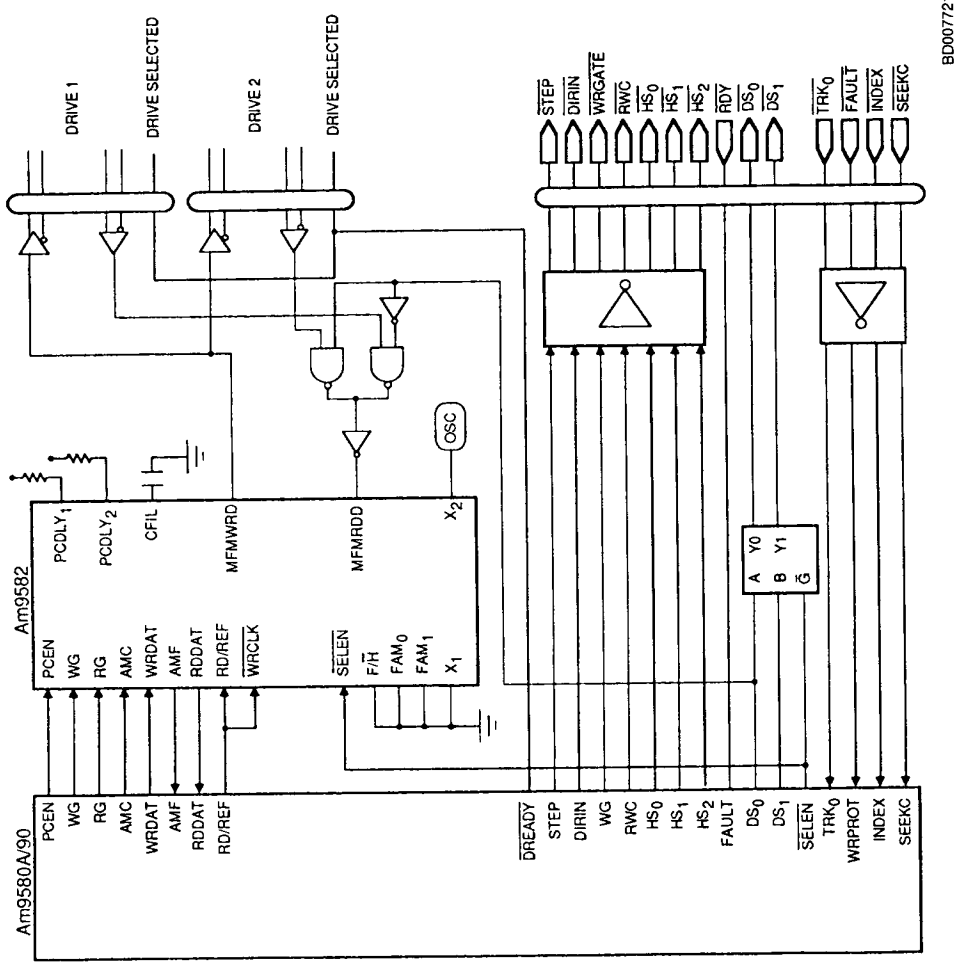


Figure 9. Typical ST-506 Interface

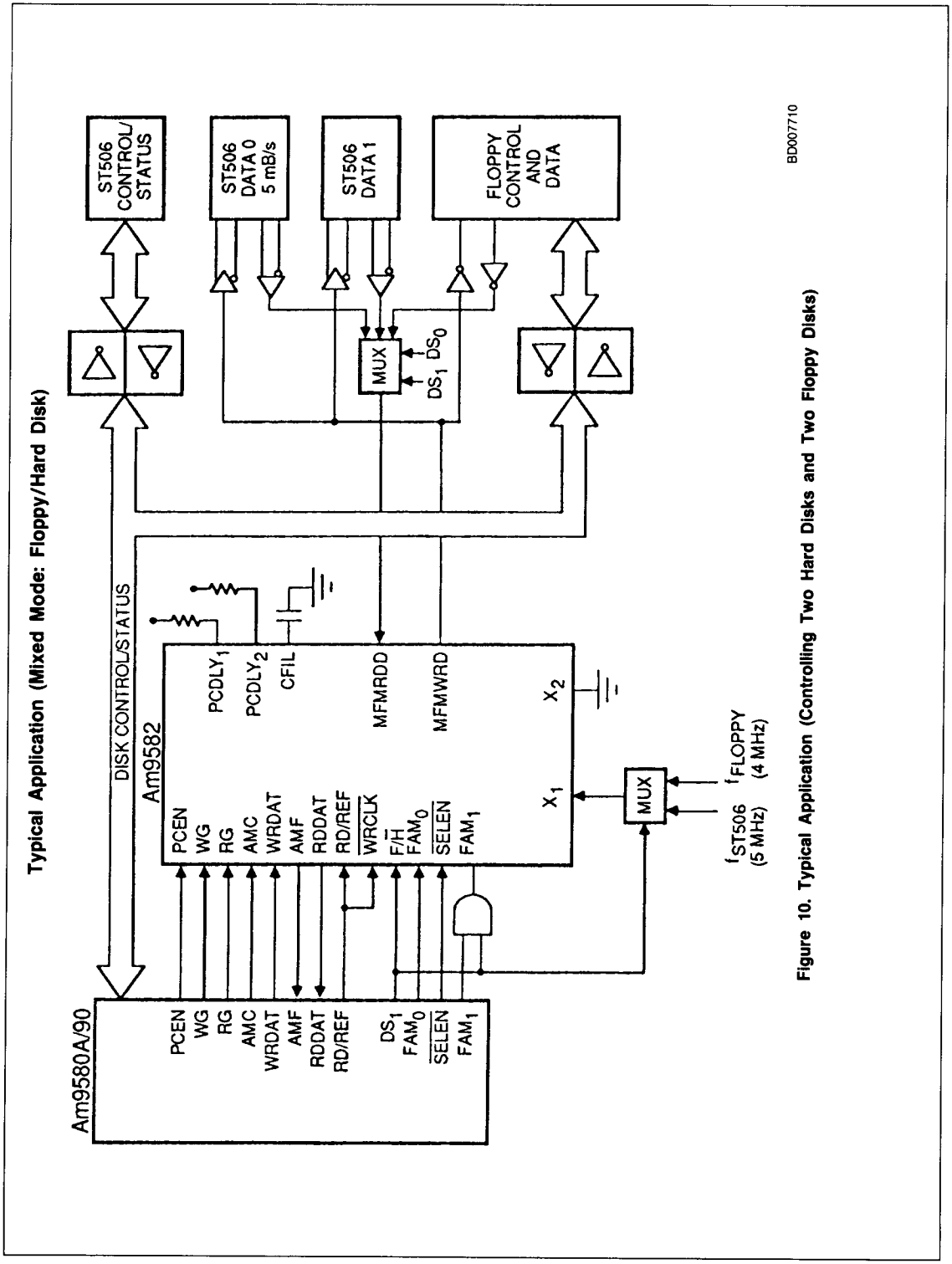


Figure 10. Typical Application (Controlling Two Hard Disks and Two Floppy Disks)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground
Potential Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to +V_{CC}
DC Input Voltage ..... −0.5 to +7.0 V
DC Output Current into Outputs ..... 30 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +50°C
Supply Voltage (V_{CC}) ..... 5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions (Note 1)			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage for All Inputs (Note 4)			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage for All Inputs (Note 4)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V	(Note 4)			−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.4 V	(Note 4)			20	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V	(Note 4)			1.0	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = Max.	V_O = 0.4 V			−50	μA
			V_O = 2.4 V			50	
I_{SC}	Output Short-Circuit Current (Note 2)	V_{CC} = Max.			−15	−50	mA
I_{CC}	Power Supply Current (Note 3)	V_{CC} = Max.	0 to +50°C (Note 3)	9582		395	mA
				9582A		300	

Notes: 1. For conditions shown as Min. or Max. use the appropriate value specified under Operating Ranges for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
3. All three-state outputs are in the high-impedance state.
4. Logic inputs (Does not include X_1, X_2, $PCDLY_n$, CFIL).

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
READ (Disk Controller Interface)					
1	t_H	RD/REF CLK HIGH Pulse Width (5 MHz)	40		ns
2	t_L	RD/REF CLK LOW Pulse Width (5 MHz)	40		ns
3	t_{CYC}	RD/REF CLK Cycle Time	T		
4	t_W (Note 3)	RG ↓ to RG ↑ Dwell Time	T		
5	t_D	RD/REF CLK ↑ to AMF ↑ (Active) Delay		20	ns
6	t_D	AMC ↓ to AMF ↓ (Inactive) Delay		40	ns
7	t_D	RD/REF CLK ↑ to RDDAT Delay		20	ns
8	t_S	Valid FAM to AMC ↑ Setup Time	10		ns
9	t_H	AMC ↑ to Valid FAM Hold Time	10		ns
10	t_D	RD/REF CLK ↑ to Valid FDDAM/2f Delay		20	ns
11	t_D	AMC ↓ to Valid FDDAM/2f Delay		40	ns
12	t_W (Note 3)	RG ↑ to RG ↓ Width	T		
13	t_W (Note 3)	AMC ↓ to AMC ↑ Dwell Time	T		
14	t_D (Note 3)	RG ↑ to AMC ↑ Delay		8T	
WRITE (Disk Controller Interface)					
15	t_H	WRCLK HIGH Pulse Width	0.5T		
16	t_L	WRCLK LOW Pulse Width	0.5T		
17	t_W	WRCLK Cycle Time	T		
18	t_W (Note 3)	WG ↓ to WG ↑ Dwell Time	T		
19	t_S	AMC ↑ to WRCLK ↑ Setup Time	10		ns
20	t_W (Note 3)	AMC ↓ to AMC ↑ Dwell Time	2T		
21	t_D	WRCLK ↑ to AMF ↑ Delay		40	ns
22	t_D	AMC ↓ to AMF ↓ Delay		40	ns
23	t_S	WRDAT Valid to WRCLK ↑ Setup Time	10		ns
24	t_H	WRCLK ↑ to WRDAT Valid Hold Time	10		ns
25	t_S	FAM Valid to AMC ↑ Setup Time	10		ns
26	t_H	AMC ↑ to FAM Valid Hold Time	10		ns
27	t_S	WG ↑ to WRCLK ↑ Setup Time	10		ns
28	t_H	WRCLK ↑ to WG ↓ Hold Time	10		ns
29	t_S	PCEN/S($\overline{D}$) Valid to WG ↑ Setup Time	−T		
30	t_H	WG ↓ to PCEN/S($\overline{D}$) Valid Hold Time	3T		
31	t_S	S($\overline{D}$) to $\overline{SELEN}$ LOW Setup Time	10		ns
32	t_H	$\overline{SELEN}$ LOW to S($\overline{D}$) Hold Time	10		ns
CRYSTAL OSCILLATOR (External Frequency Mode)					
33	t_H	X_1 HIGH Pulse Width	20		ns
34	t_L	X_1 LOW Pulse Width	20		ns
35	t_D	X_1 Cycle Time	62	250	ns
36	t_D (Note 1)	X_1 ↑ to RD/REF CLK ↑ Delay		40	ns

Notes: See notes following end of table on next page.

SWITCHING CHARACTERISTICS (Cont'd.)

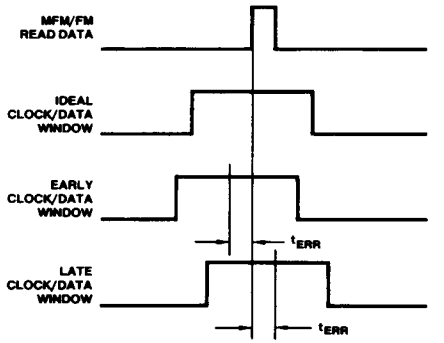
No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
READ (Disk Drive Interface)					
37	t_H	MFM/FM RDDAT HIGH Pulse Width	15		ns
38	t_L	MFM/FM RDDAT LOW Pulse Width	15		ns
WRITE (Disk Drive Interface)					
42	t_H (Note 2)	MFM/FM WRDAT HIGH Pulse Width (5 MHz)	40		ns
43	t_L (Note 2)	MFM/FM WRDAT LOW Pulse Width (5 MHz)	100		ns

Notes: 1. For REF CLK only.
2. No Pre-Compensation; tested at 5 MHz.
3. These Parameters are not part specifications.
The system should meet these numbers for optimum performance.

ANALOG CHARACTERISTICS

Data Phase-Locked-Loop Specifications

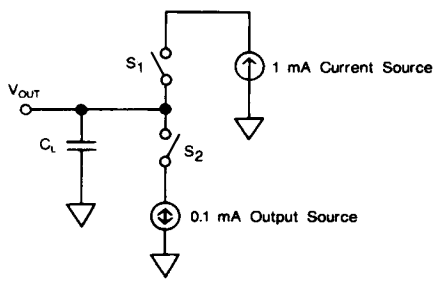
Acquisition Time*	16 x $1/f_D$ second Max.
Capture Range*	±6% of f_D Min.
Decode Window Error*	±2.5 ns or ±2% of f_D Max., whichever larger



Decode Window Error

*Note: f_D = bit rate frequency

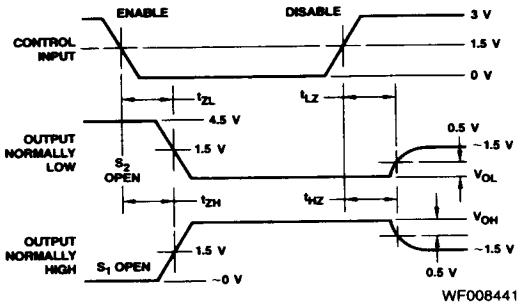
SWITCHING TEST CIRCUIT



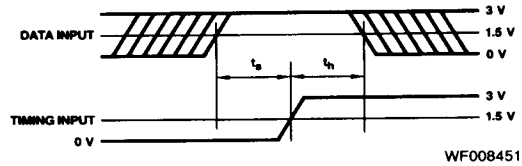
A. Outputs

Notes: 1. C_L = 50 pF, the load capacitance includes scope probe, wiring, and stray capacitance without the device in the test fixture.
2. S_1 and S_2 are open during all DC and functional testing.
3. During AC testing, switches are set as follows:
   1) For $V_{OUT} > 1.5$ V, S_1 is closed and S_2 open.
   2) For $V_{OUT} < 1.5$ V, S_1 is open and S_2 closed.

SWITCHING TEST WAVEFORMS

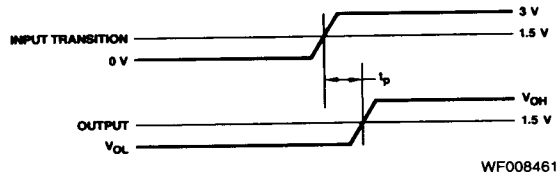


A. Enable and Disable Times

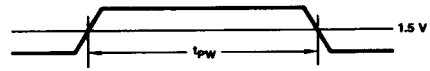


B. Setup and Hold Time Measurements

Notes: 1. Diagram shown for input control Enable-LOW and input control Disable-HIGH.
2. S_1 and S_2 of load circuit are closed except where shown.



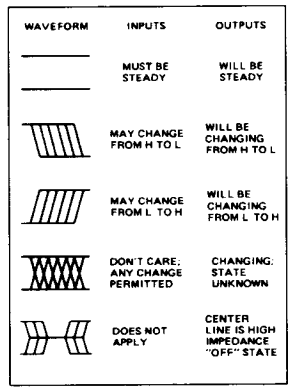
C. Propagation Delay Measurements



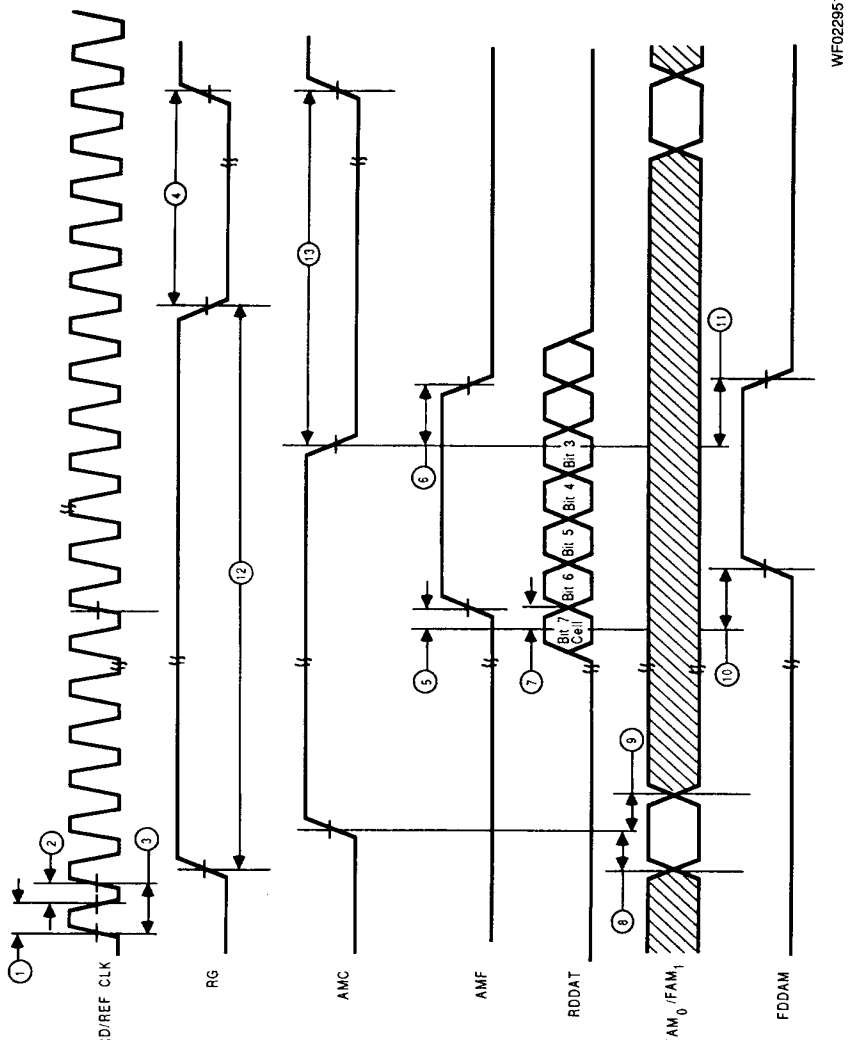
D. Pulse Width Measurements

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



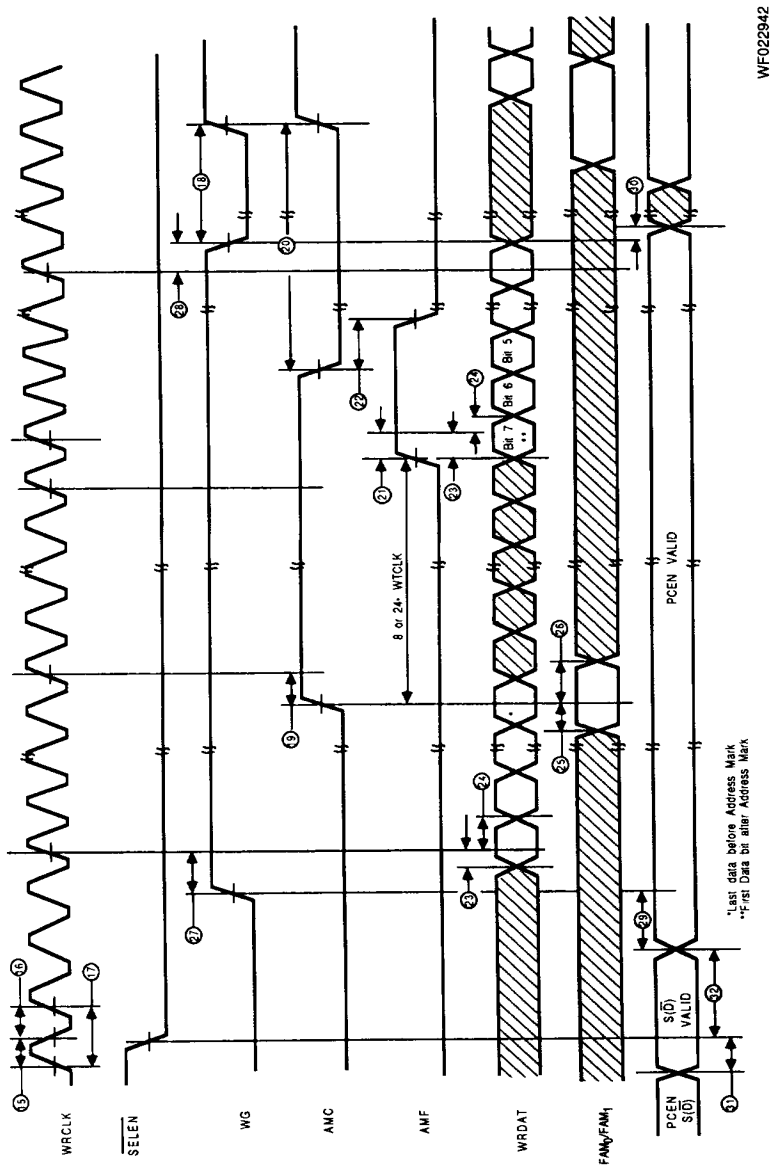
SWITCHING WAVEFORMS (Cont'd.)



WF022951

Read Timing (Disk Controller Interface)

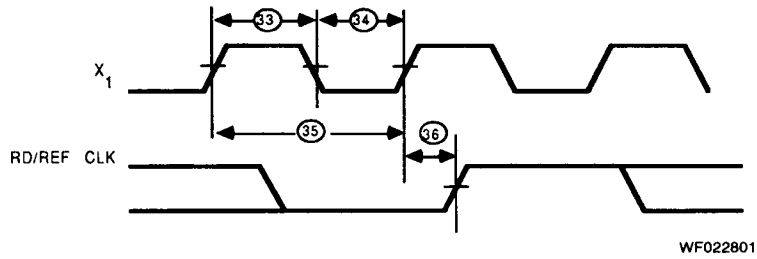
SWITCHING WAVEFORMS (Cont'd.)



WF022942

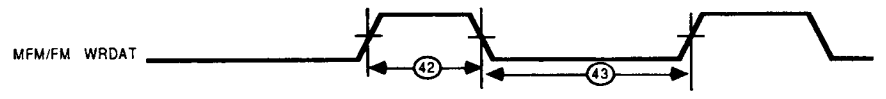
Write Timing (Disk Controller Interface)

SWITCHING WAVEFORMS (Cont'd.)



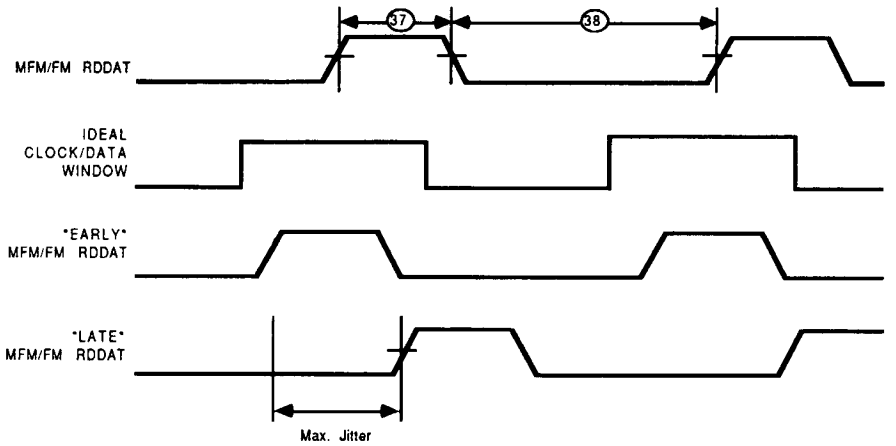
WF022801

Crystal Oscillator (External Frequency Mode)



WF022810

Write (Disk Drive Interface)

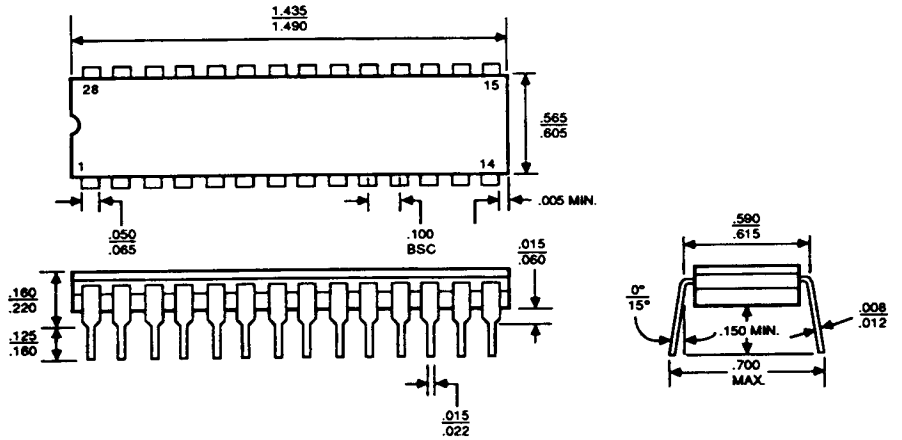


WF022822

Read (Disk Drive Interface)

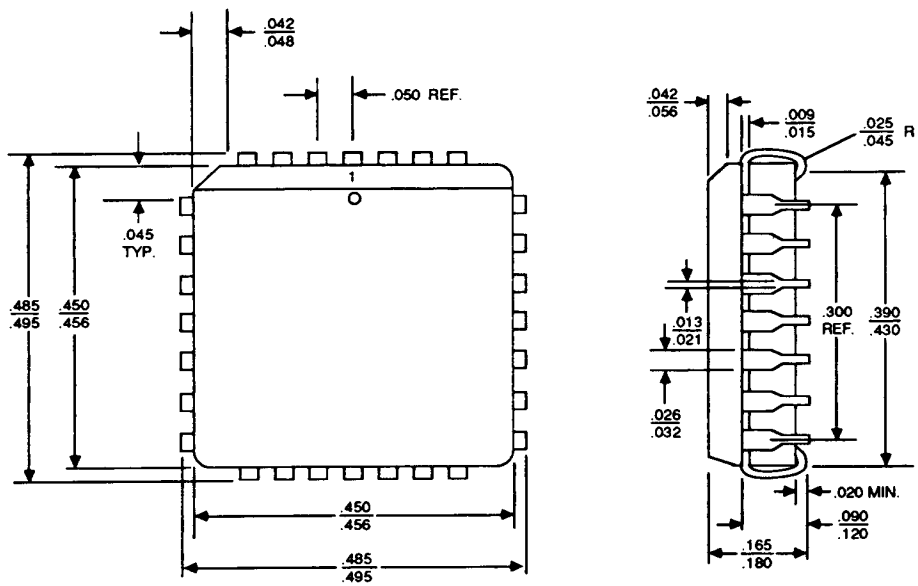
PHYSICAL DIMENSIONS*

CD 028



PID# 068376

PL 028



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*For reference only.

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