

Optocoupler-less

Isolated Flyback Converter

BD7F200HFN-LB BD7F200EFJ-LB

General Description

This product guarantees long time supply availability in the industrial instrumentation market.

BD7F200 is an optocoupler-less Isolated Flyback Converter. An optocoupler or the tertiary winding feedback circuit which was needed to obtain a stable output voltage isolated by a transformer in the conventional application becomes unnecessary, thus, the number of parts is reduced drastically, producing a small-sized and high-reliability application isolated type power supply.

Furthermore, a highly by the use of the Original Adapted-Type ON-Time Control Technology, it makes the external phase compensation parts become unnecessary, therefore a highly efficient isolated type power supply application can easily be produced.

Features

- Guaranteed long time supply availability for Industrial Applications.
- No need for an optocoupler or a transformer tertiary winding.
The output voltage can be set by two external resistors and the transformer turns ratio.
- Uses Original Adapted Type ON-Time Control Technology.
High-speed load response is realized and external phase compensation parts are unnecessary.
- Fixed switching frequency and low output ripple
- Highly efficient light load mode available (PFM operation)
- Shutdown / Enable Control
- Built-in N-Channel MOSFET
- Soft start function
- Output load compensation function
- Protection functions:
VIN Under Voltage Lock-Out (VIN UVLO)
Over Current Protection (OCP)
Thermal Shutdown Protection (TSD)

Application

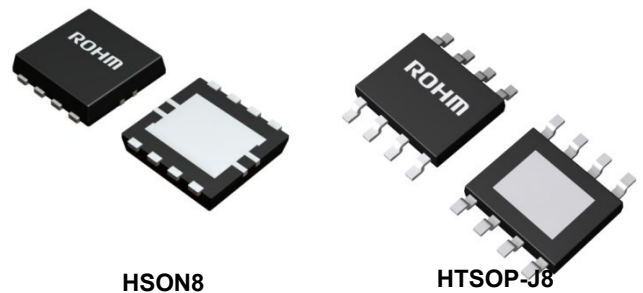
- Industrial equipment Isolated Power Supply

Key Specifications

■ Supply Voltage of Operation:	8V to 40V
■ SW Terminal Operating Voltage:	50V (Max)
■ Over Current Limit:	2.75A (Typ)
■ Switching Frequency:	400kHz (Typ)
■ Reference Voltage Accuracy:	±1.5% (Typ)
■ Quiescent Current:	0μA (Typ)
■ Operating Current:	2mA (Typ)
■ Junction Temperature of Operation:	-40°C to +125°C

Packages

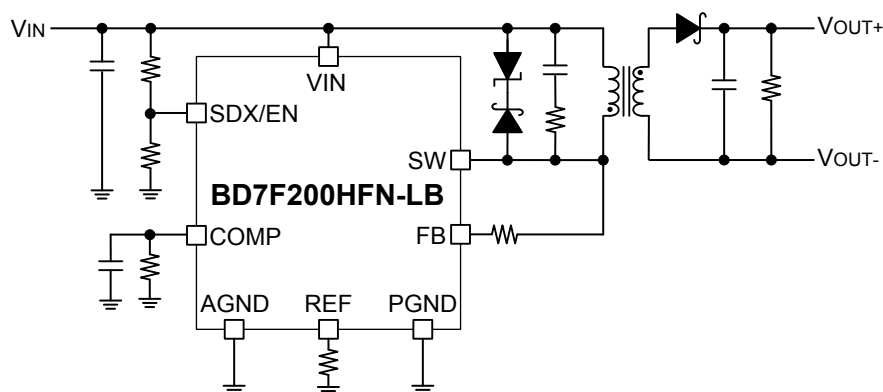
	W(Typ)	D(Typ)	H(Max)
HSO8	2.90mm	3.00mm	0.60mm
HTSOP-J8	4.90mm	6.00mm	1.00mm



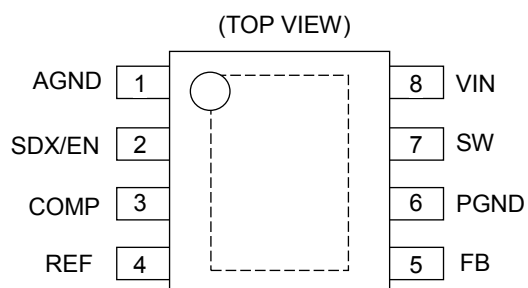
HSON8

HTSOP-J8

Typical Application Circuit



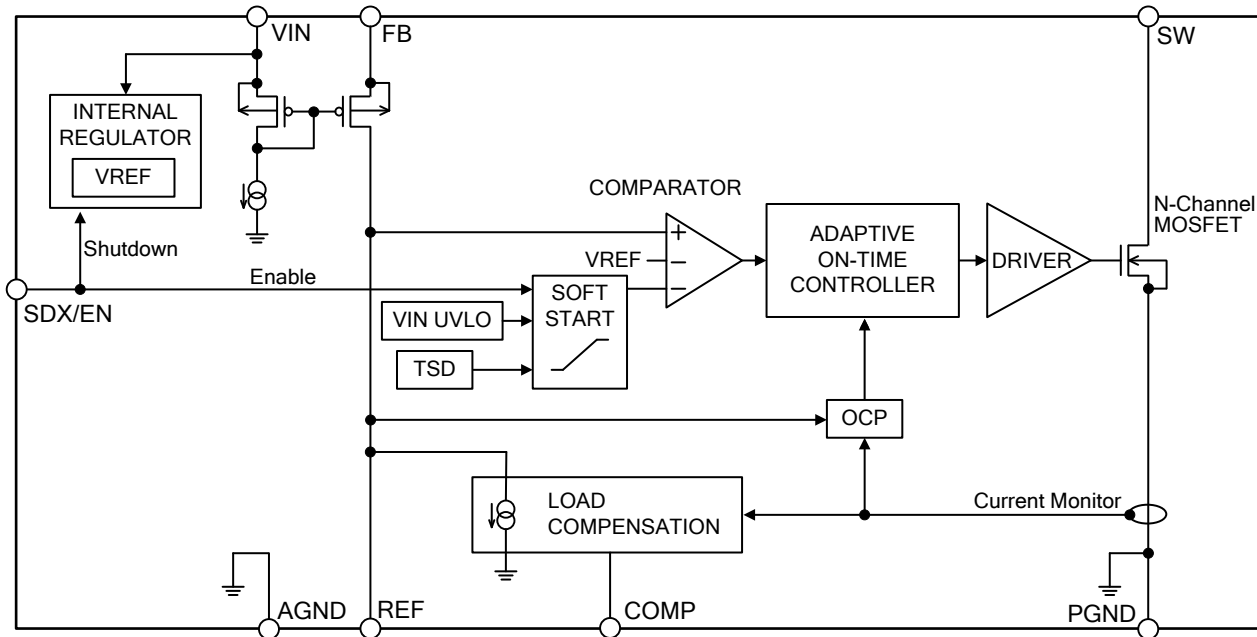
Pin Configuration



Pin Descriptions

Pin No.		Pin Name	Function
HSO8	HTSOP-J8		
1	1	AGND	Analog system GND
2	2	SDX/EN	Shutdown/Enable control
3	3	COMP	Load Current Compensation of the output voltage set up
4	4	REF	Output voltage setup
5	5	FB	Output voltage setup
6	6	PGND	Power system GND
7	7	SW	Switching Output
8	8	VIN	Power supply

Block Diagram



Description of Blocks

- INTERNAL REGULATOR**
 This is the regulator block for internal circuits.
 Also includes a reference voltage generating block (VREF).
 This block is in the shutdown state when the SDX/EN terminal is below 0.9V (Typ).
- VIN UVLO**
 This is the input low-voltage-protection block.
 If the power supply input voltage, V_{IN} , falls to below 6.2V (Typ), it will be detected and this block will be in the protection state and the SW terminal becomes Hi-Z.
 When the power supply input voltage (V_{IN}) rises to 6.9V (Typ), it automatically recovers through the soft start.
 (Hysteresis voltage: 0.7V (Typ).)
- SOFT START**
 When the SDX/EN terminal is in the enable state with more than 2.0V (Typ), this block prevents inrush current and overshoot in the rising of the output voltage by making the reference voltage of the COMPARATOR block rise slowly from 0V to VREF voltage.
 The default soft start time, t_{SS} , is designed to be 6ms (Typ) internally.
 The min off time is 750ns (Typ) when the output voltage is below 50% of the set voltage.
- COMPARATOR**
 This is the block which compares the reference voltage VREF with the REF terminal voltage which is the feedback voltage of the SW terminal voltage.
 Since the feedback loop is structured by a comparator is established, it has excellent response to load fluctuation.
- ADAPTIVE ON-TIME CONTROLLER**
 This is the block corresponding to the original adapted type ON-Time control technology.
 Switching frequency is fixed at 400kHz (Typ) under PWM Control when the load is stable.
 Under On-Time Control, when the load varies, fast load response is enabled by changing the switching frequency.
 During light load, the highly efficient PFM will operate and the self-power dissipation is suppressed by decreasing the switching frequency.
- DRIVER**
 This is the block which drives the built-in N-Channel MOSFET.

Description of Blocks - continued

7. LOAD COMPENSATION

This is the block which compensates the output voltage regulation by VF characteristic fluctuation of the secondary side output diode according to the load current.

The current which flows into the built-in N-Channel MOSFET is monitored, and the current according to the compensation quantity and the time constant which are determined by the external resistor and the capacitor of the COMP terminal is drawn from the REF terminal. The output voltage rises and is rectified when feedback current which flows into the external resistor of the REF terminal decreases and the REF terminal voltage falls.

8. TSD

This is the temperature protection block.

If the chip's junction temperature, T_j , inside the IC is above 175°C (Typ), it will be detected and this block will be in the protection state and the SW terminal becomes Hi-Z.

If T_j falls to below 150°C (Typ), it will return automatically through soft start.

9. OCP

This is the over-current protection block.

If the peak current during the ON-Time of the built-in N-Channel MOSFET reaches 2.75A (Typ), it will be detected and the N-Channel MOSFET is turned OFF.

If output voltage goes to 50% or less of the setting voltage, the peak detection current of OCP will be controlled by 1.6A (Typ). The min off time is 1.5μs (Typ) when the OCP is operated under the condition where the output voltage is 50% of the set voltage.

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Rating		Unit
		BD7F200HFN-LB	BD7F200EFJ-LB	
VIN Input Power Voltage ^(Note 1)	V _{IN}	45		V
SW Terminal Voltage	V _{SW}	60		V
SDX/EN Terminal Voltage	V _{SDX/EN}	V _{IN}		V
FB Terminal Voltage	V _{FB}	V _{IN} -0.3V to lower value of V _{IN} +0.3V or 45V		V
REF Terminal Voltage	V _{REF}	7		V
COMP Terminal Voltage	V _{COMP}	7		V
Power Dissipation	P _d	1.75 ^(Note 2)	3.75 ^(Note 3)	W
Storage Temperature Range	T _{stg}	-55 to +150		°C
Maximum Junction Temperature	T _{jmax}	150		°C

(Note 1) Not to exceed Power Dissipation (P_d).

(Note 2) Reduced by 14.0mW/°C for temperatures above 25°C (when mounted on a one-layer glass-epoxy board with 70mm × 70mm × 1.6mm dimension, 65% copper foil density)

(Note 3) Reduced by 30.0mW/°C for temperatures above 25°C (when mounted on four-layer glass-epoxy board with 70mm × 70mm × 1.6mm dimension.)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

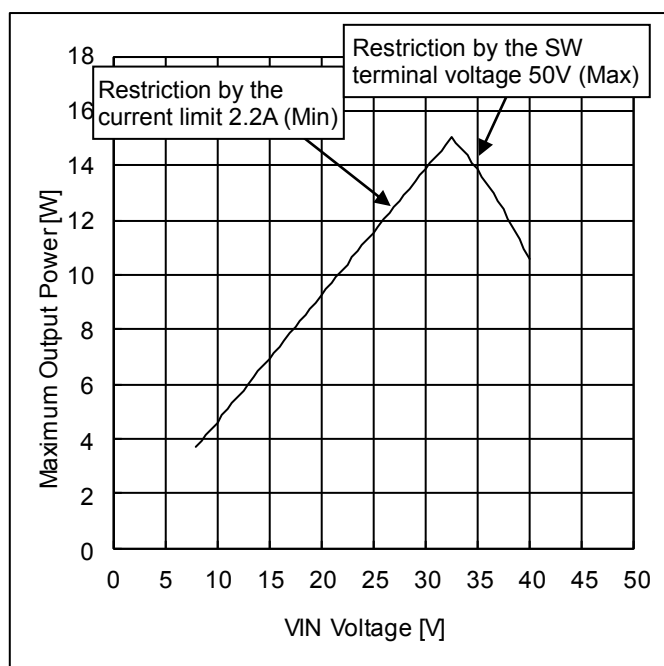
Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
VIN Input Power Voltage	V _{IN}	8	24	40	V
SW Terminal Voltage	V _{SW}	-	-	50	V
Junction Temperature ^(Note 4)	T _j	-40	-	+125	°C

(Note 4) Life time is derated at junction temperature greater than 125°C.

Electrical Characteristics (Unless otherwise specified Ta = 25°C, V_{IN} = 24V, and V_{SDX/EN} = 2.5V.)

Electrical Characteristics (Unless otherwise specified Ta = 25°C, VIN = 2+V, and VSDX/EN = 2.5V.)						
Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Power Supply						
Quiescent Current	IST	-	0	10	µA	VSDX/EN = 0V
Operating Current	ICC	-	2	4	mA	VSDX/EN = 2.5V VREF = 2V (at PFM operation)
UVLO Detection Voltage	VUVLO	5.7	6.2	6.7	V	VIN falling
UVLO Hysteresis Voltage	VUVLO_HYS	0.6	0.7	0.8	V	
SDX/EN Control						
Shutdown Voltage	VSDX	0.3	0.9	1.5	V	
Enable Voltage	VEN	1.9	2.0	2.1	V	VSDX/EN rising
Enable Hysteresis Voltage	VEN_HYS	0.15	0.2	0.25	V	
SDX/EN Input Current	ISDX/EN	-	0	1	µA	VSDX/EN=2V
Reference Voltage						
Reference Voltage	VREF	0.768	0.78	0.792	V	
Switch Characteristics						
ON-Resistance	RON	-	0.5	-	Ω	Between SW - PGND terminals
Over Current Limit	ILIMIT	2.2	2.75	3.3	A	
Switching Frequency	fSW	-	400	-	kHz	At PWM operation (Duty=40%)
Minimum ON Time	ton_MIN	-	350	-	ns	
Minimum OFF Time	toff_MIN	-	300	-	ns	
Maximum OFF Time	toff_MAX	-	20	-	µs	
Soft Start Time	tss	-	6	-	ms	0V to (VREF×90%)

Typical Performance Curves



Maximum output power is restricted in general by a current limit and the maximum operating voltage of SW terminal. Furthermore, it also changes with the characteristics of external parts (Transformer, Schottky barrier diode, Snubber circuit, etc.).

Figure 1. Maximum Output Power vs VIN Voltage

Typical Performance Curves

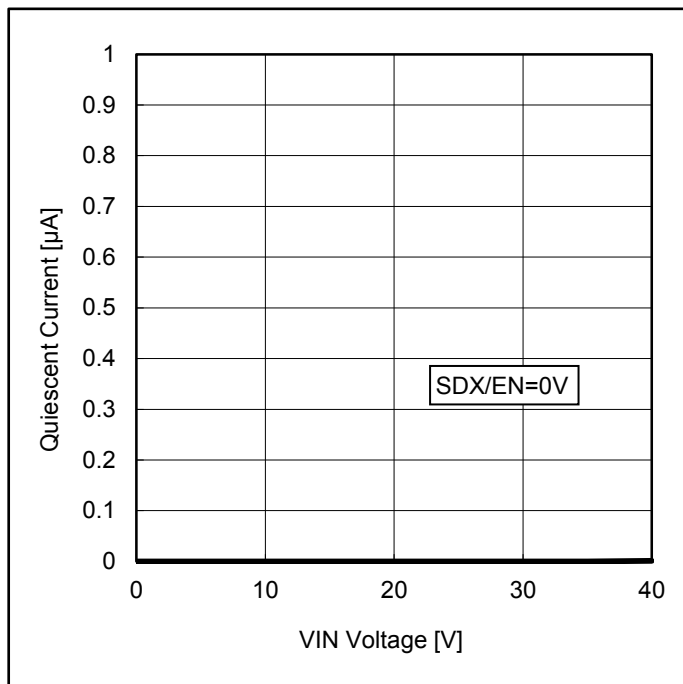


Figure 2. Quiescent Current vs VIN Voltage

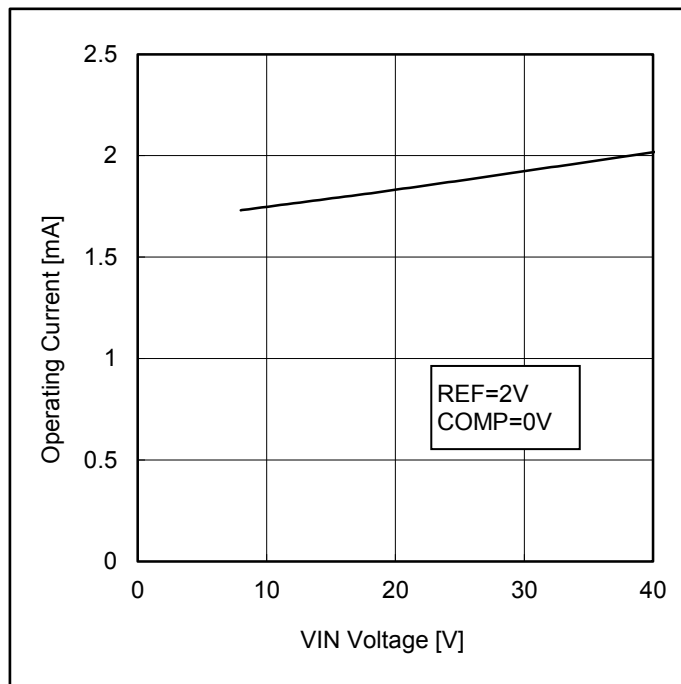


Figure 3. Operating Current vs VIN Voltage

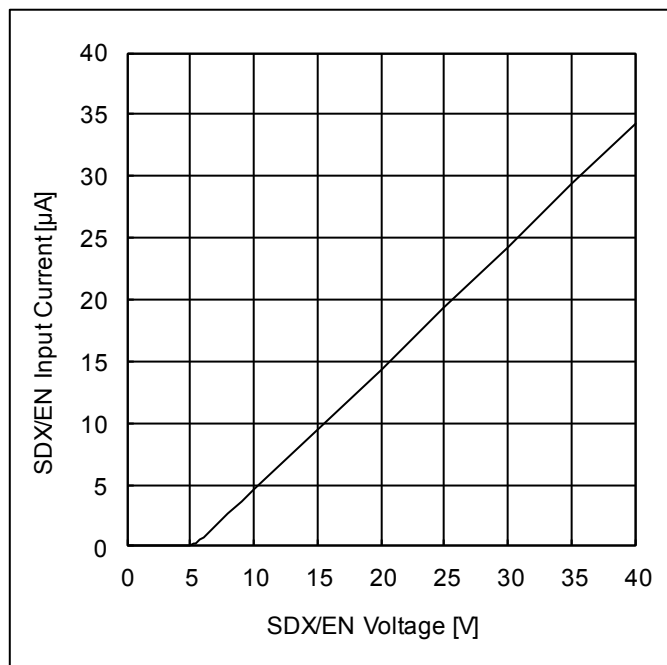


Figure 4. SDX/EN Input Current vs SDX/EN Voltage

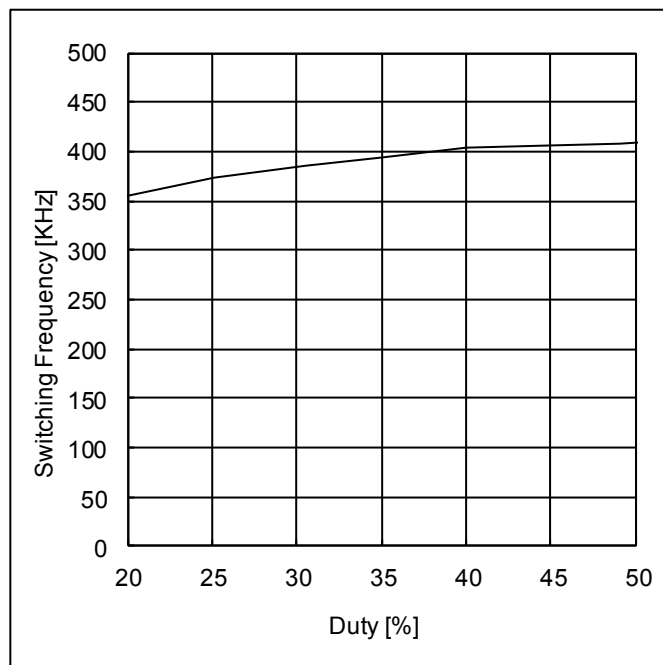


Figure 5. Switching Frequency vs Duty

Typical Performance Curves

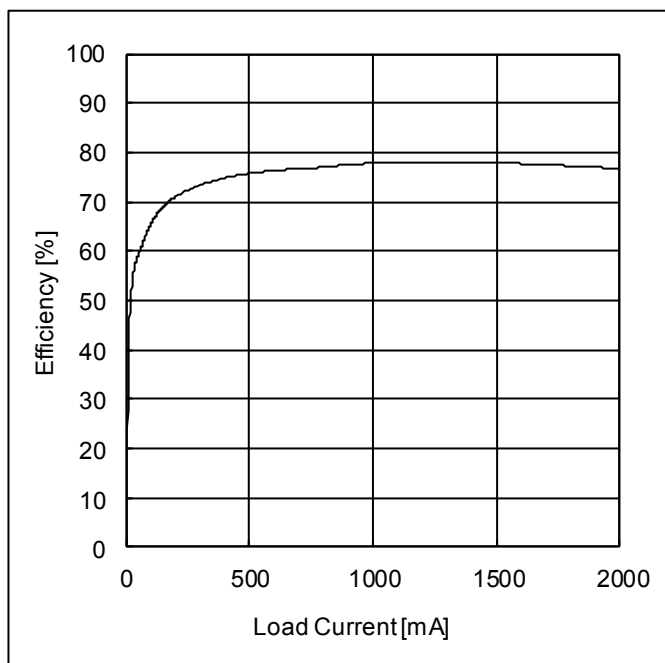


Figure 6. Efficiency vs Load Current
(24V Input, 5V Output)

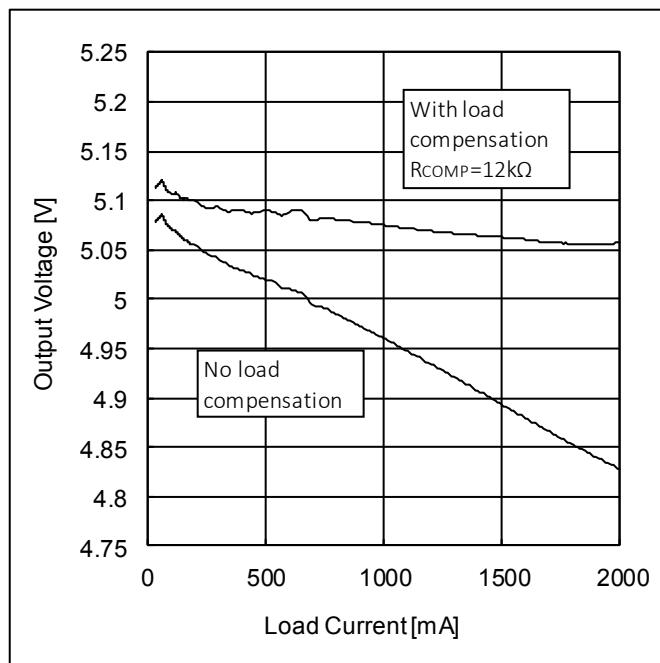


Figure 7. Output Voltage vs Load Current
(24V Input, 5V Output)

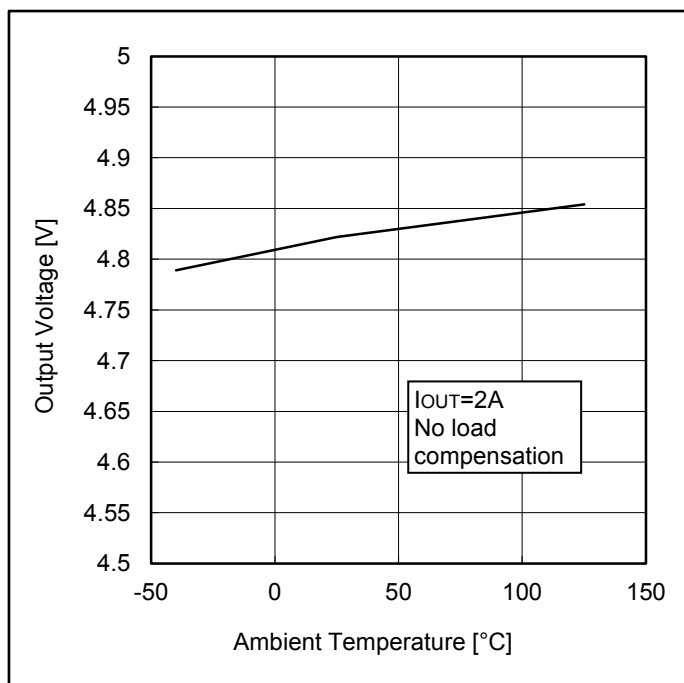


Figure 8. Output Voltage vs Ambient Temperature
(24V Input, 5V Output)

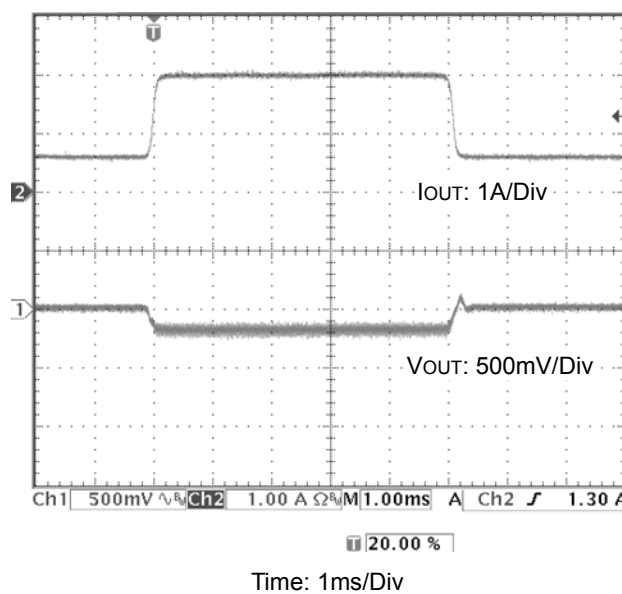
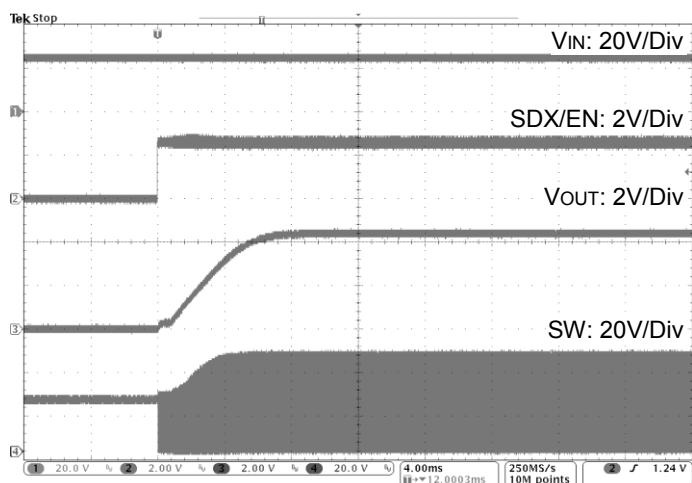


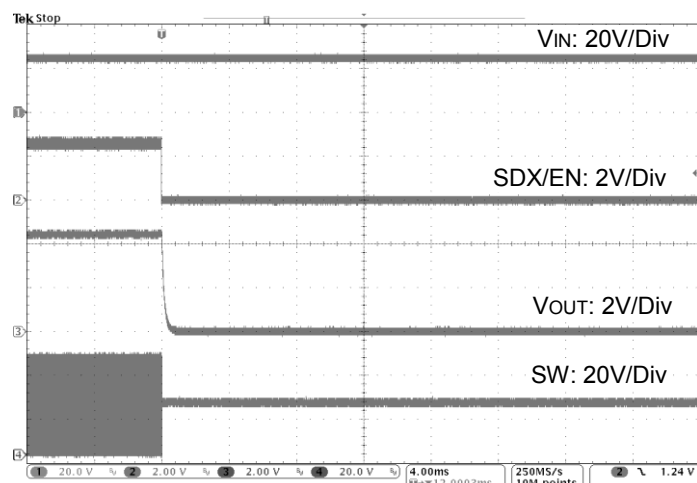
Figure 9. Load Transient Response
(24V Input, 5V Output, with Load Compensation,
and $I_{OUT} = 600\text{mA} \leftrightarrow 2\text{A}$)

Typical Performance Curves



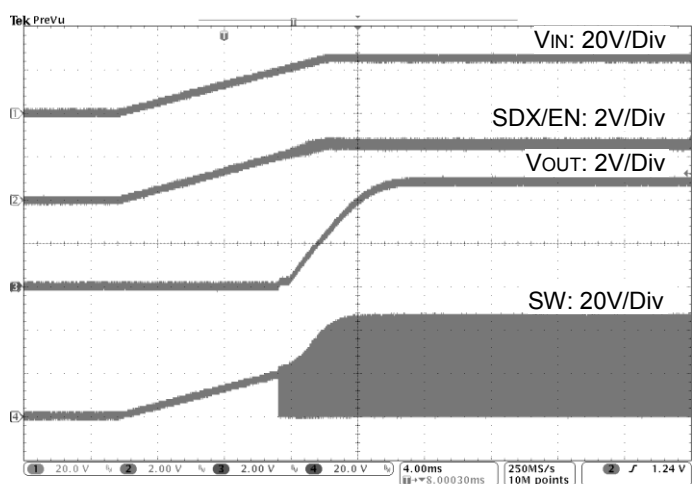
Time: 4ms/Div

Figure 10. Start Up Wave Forms(SDX/EN control)
(24V Input, 5V Output, SDX/EN=0V->2.5V)



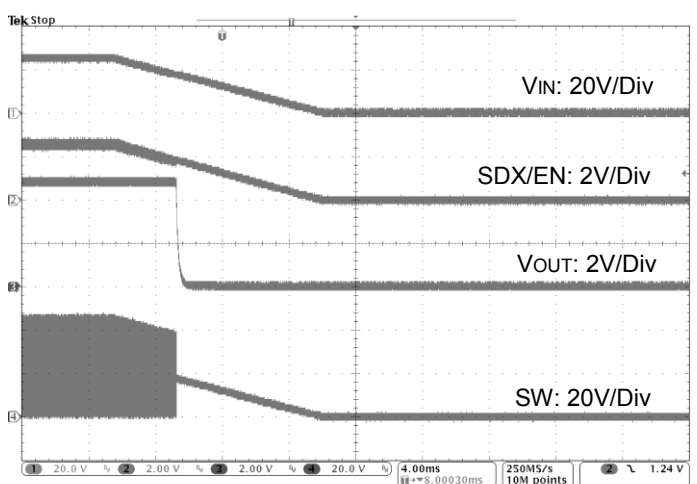
Time: 4ms/Div

Figure 11. Shutdown Waveforms (SDX/EN control)
(24V Input, 5V Output, SDX/EN=2.5V->0V)



Time: 4ms/Div

Figure 12. Start Up Wave Forms(VIN control)
(24V Input, 0V Output, VIN=0V->24V, R1=1MΩ, R2=120kΩ)



Time: 4ms/Div

Figure 13. Shutdown Waveforms(VIN control)
(24V Input, 5V Output, VIN=24V->0V, R1=1MΩ, R2=120kΩ)

Application Examples

Exercise caution with the actual system since the characteristic changes with the board layout and the types of external parts mounted, and etc.

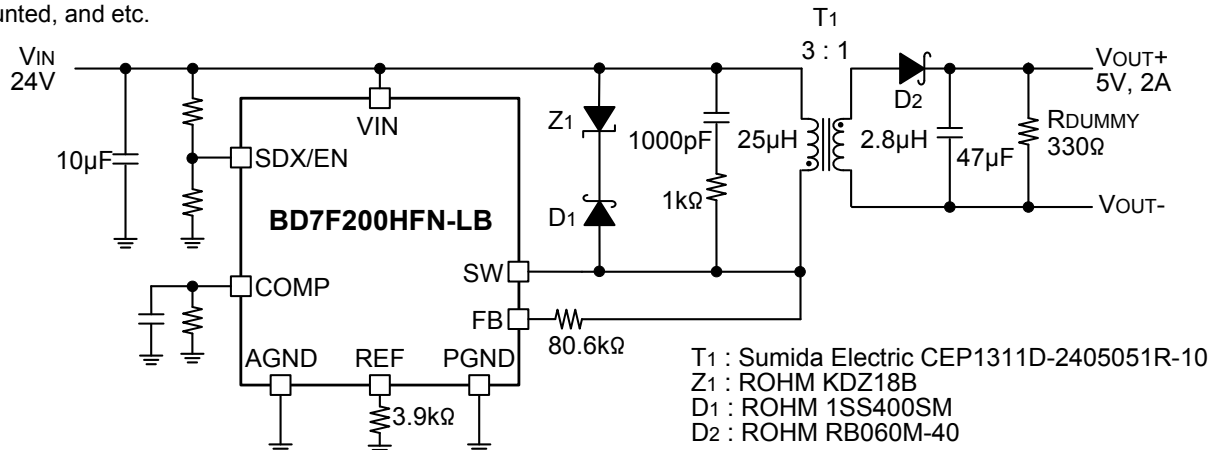


Figure 14. 24V Input, 5V Output

Table1. Recommended Transformers

Part Number	Size (W×L×H) [mm]	LP [µH]	Np : Ns	Vendor	Target Applications		
					VIN [V]	VOUT [V]	IOUT [A]
CEP1311D-2405051R-10	13.5×20.0×12.5	25	3 : 1	Sumida Electric	24	5	2

Application Information

1. Outline Operation

This product is an isolated type flyback converter without an optocoupler. An optocoupler or a transformer's tertiary winding feedback circuit which was needed to obtain a stable output voltage isolated by a transformer in the conventional application becomes unnecessary, thus, the number of parts is reduced drastically, producing a small-sized and high-reliability application isolated type power supply.

Furthermore, a highly efficient isolated type power supply application can easily be produced the use of the Original Adapted-Type ON-Time Control Technology which eliminates the need for external phase compensation parts.

The off time is determined by comparing the reference voltage inside the IC with the information which was obtained by the feedback of the secondary output voltage through primary flyback voltage.

Adapted-type ON time control,

- (1) Switching frequency is fixed at 400kHz (Typ) for PWM operation when the load stabilizes.
- (2) During load current fluctuation, the ON-Time Control will operate and the switching frequency will change, thus a high-speed load response is obtained.
- (3) During light load, high efficiency is obtained because the switching frequency decreases.

2. Timing Chart

(1) Start-up/Shut-down

Output voltage gradually turns ON through the soft start function when SDX/EN terminal rises to above 2.0V(Typ) (Enable state). When SDX/EN terminal falls below 1.8V (Typ), output voltage turns OFF (Disable state).

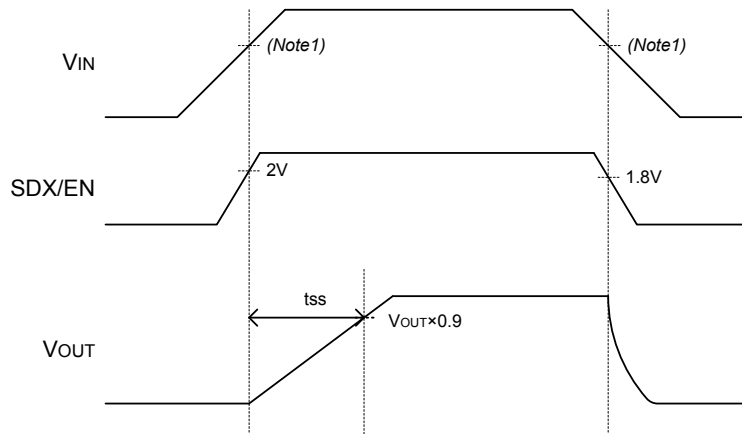


Figure 15. Start-up/Shut-down Timing Chart

(Note 1) In the control system of this IC, it has to be operated where duty is below 50%. When turning ON/OFF the IC, control the SDX/EN terminal as enable/disable under the condition where VIN fulfills below equation.

$$V_{IN} > \frac{N_p}{N_s} \times (V_{OUT} + V_F) \quad [V]$$

where:

V_{IN} is the VIN input power voltage

N_p is the number of turns in the transformer primary side

N_s is the number of turns in the transformer secondary side

V_{OUT} is the output voltage

V_F is the forward voltage of the output diode in the secondary side

If SDX/EN terminal is connected to VIN terminal, duty could be more than 50% and unexpected output voltage might occur when turning ON/OFF. Please refer to "8. Enable Voltage" on page 15 of the application information for the enable control with VIN terminal.

(2) VIN Under Voltage Lock-Out (VIN UVLO)

When the input voltage (V_{IN}) falls below 6.2V (Typ), it will be detected, followed by SW terminal becomes Hi-Z then output turns OFF.

When the input voltage (V_{IN}) rises to above 6.9V (Typ), it automatically recovers through the soft start.
(Hysteresis voltage: 0.7V (Typ))

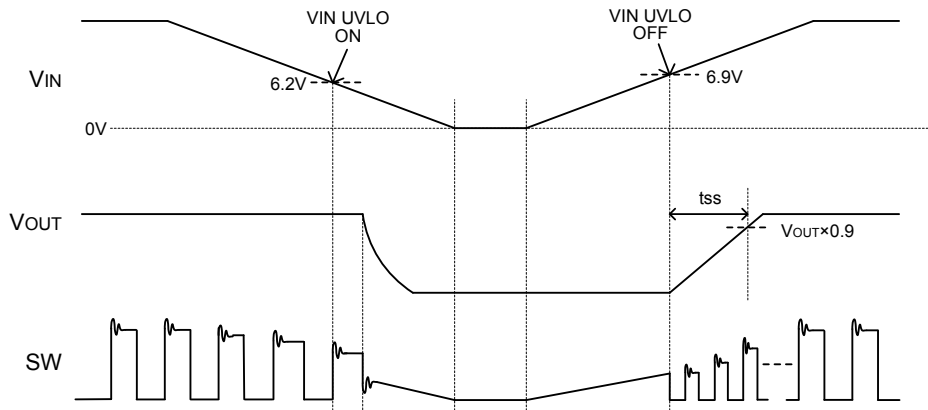


Figure 16. VIN UVLO Timing Chart

(3) Thermal Shutdown Protection (TSD)

When the internal chip (Junction) temperature exceeds $T_j=175^{\circ}\text{C}$ (Typ), it will be detected, followed by SW terminal becomes Hi-Z, then output turns OFF.

When T_j decreases below 150°C (Typ), it automatically recovers through the Soft Start.

Note that the thermal shutdown circuit is designed to shutdown the IC from thermal runaway under abnormal circumstances with the temperature exceeding $T_{jmax} = 150^{\circ}\text{C}$. It is not designed to protect or guarantee the application set. Please refrain from using this function as a protection design of the application set.

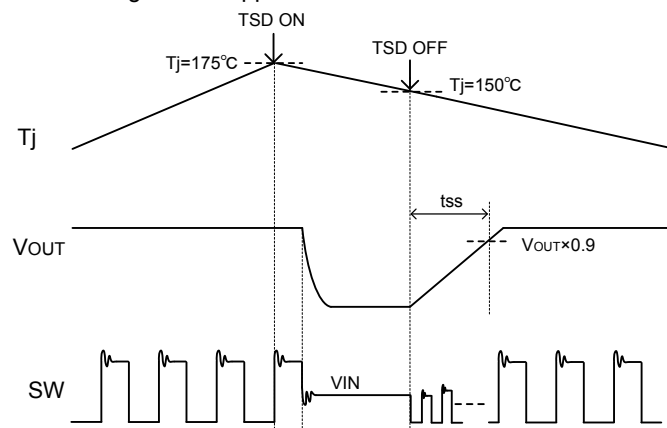


Figure 17. TSD Timing Chart

(4) Over Current Protection (OCP)

When the peak current reaches 2.75A (Typ) during the built-in N-channel MOSFET is ON, it will be detected, followed SW terminal becomes Hi-Z, then N-channel MOSFET turns OFF. It is detected per switching cycle, and output voltage decreases as ON duty is limited.

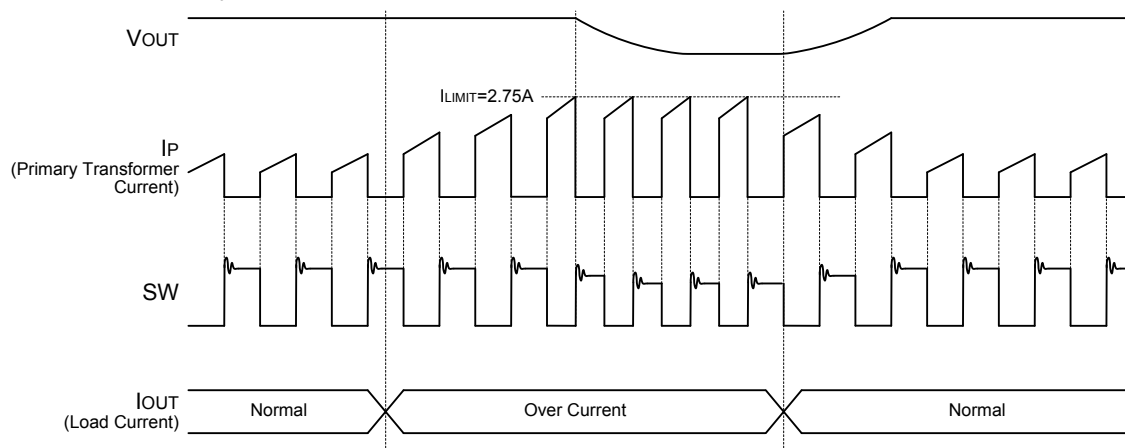


Figure 18. OCP Timing Chart

3. Output Voltage

SW terminal voltage is higher than input voltage (V_{IN}) when the built-in N-Channel MOSFET is OFF.

This primary flyback voltage (the gap between SW terminal voltage and V_{IN}) contains the information of the secondary output voltage.

SW terminal voltage can be calculated as follows:

$$V_{SW} = V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F + I_S \times ESR) \quad [V]$$

where:

V_{SW} is the SW terminal voltage

I_S is the transformer current in the secondary side

ESR is the total impedance in the secondary side
(transformer wirewound resistance of the secondary side,
PCB impedance, and etc.)

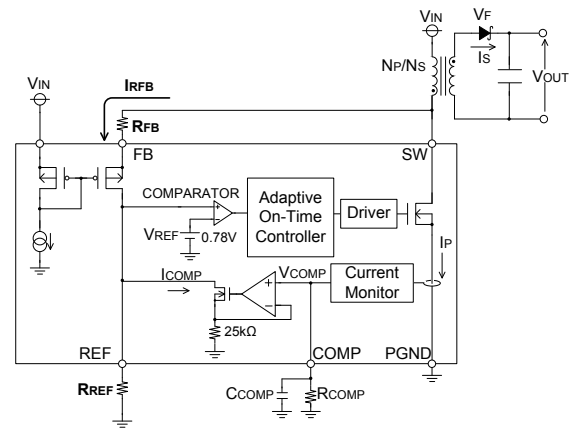


Figure 19. Control Block Diagram

This primary flyback voltage is converted to the current I_{RFB} by R_{FB} resistor. As FB terminal voltage almost equals to V_{IN} voltage due to the differential circuit of V_{IN} , I_{RFB} can be expressed by following equation:

$$\begin{aligned} I_{RFB} &= \frac{V_{SW} - V_{FB}}{R_{FB}} \\ &= \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_F + I_S \times ESR)}{R_{FB}} \quad [A] \end{aligned}$$

where:

I_{RFB} is the FB input current

V_{FB} is the FB terminal voltage

R_{FB} is the external resistance between the FB - SW terminals

REF terminal voltage can be expressed as follows since I_{RFB} flows into R_{REF} resistor.

$$V_{REF} = \frac{R_{REF}}{R_{FB}} \times \frac{N_P}{N_S} \times (V_{OUT} + V_F + I_S \times ESR) \quad [V]$$

where:

V_{REF} is the REF terminal voltage

R_{REF} is the external resistance between the REF - $AGND$ terminals

(The IC is designed on the assumption that this value is 3.9k Ω .)

The REF terminal voltage is input into the comparator and compared with the IC internal reference voltage (0.78V(Typ)). Since the loop gain of the whole system is high, the REF terminal voltage can be equal to the reference voltage in the IC. Therefore, the output voltage V_{OUT} and the REF terminal voltage V_{REF} are as follows:

$$V_{OUT} = \frac{R_{FB}}{R_{REF}} \times \frac{N_S}{N_P} \times V_{REF} - V_F - I_S \times ESR \quad [V]$$

That is, the output voltage V_{OUT} can be set by the primary and secondary side turns ratio of the transformer, and the ratio of the resistances R_{FB} and R_{REF} . V_F and ESR cause an output voltage error.

The feedback resistor R_{FB} can be expressed as follows from the relative equation with V_{OUT} :

$$R_{FB} = \frac{R_{REF}}{V_{REF}} \times \frac{N_P}{N_S} \times (V_{OUT} + V_F + I_S \times ESR) \quad [\Omega]$$

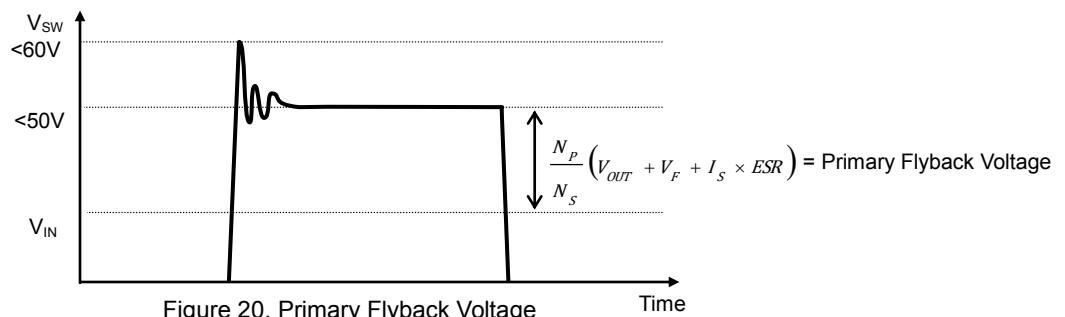


Figure 20. Primary Flyback Voltage

4. Transformer

(1) Turns Ratio

Turns ratio is the parameter which determines the output voltage, maximum output voltage, duty and SW terminal voltage. The duty of a flyback converter can be expressed by the following equation:

$$Duty = \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_F)}{V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F)}$$

Feedback voltage is monitored by the SW terminal and duty needs to be below 50% for the stable control. The minimum duty will be 20% due to the limitation of the min ON time and the turns ratio needs to fulfill below conditions:

$$\frac{1}{4} \times \frac{V_{IN}}{V_{OUT} + V_F} < \frac{N_P}{N_S} < \frac{V_{IN}}{V_{OUT} + V_F}$$

(2) Primary Side Inductance

Flyback converter has the secondary pole from the primary inductance and the secondary output capacitor. Therefore, for operational stability, selection of the primary side inductance value is important. In addition, as the primary inductance influences the maximum load, please follow below conditions:

$$\frac{1}{2} \times \frac{V_{IN}^2 \times T \times Duty^2 \times \eta}{I_{LIMIT_MIN} \times Duty \times V_{IN} \times \eta - V_{OUT_MAX} \times I_{OUT_MAX}} < L_P < \frac{2 \times Duty \times V_{IN}^2}{(V_{OUT} + V_F) \times I_{OUT_MAX} \times \pi \times f_{SW}} \quad [H]$$

where:

L_P is Primary side inductance

T is Switching output cycle

η is Efficiency

I_{LIMIT_MIN} is Minimum over current limit

I_{OUT_MAX} is Maximum Load current

f_{SW} is Switching frequency

(3) Leakage Inductance

Transformer leakage inductance causes SW terminal ringing when the built-in N-Channel MOSFET turns OFF.

A snubber circuit is recommended in order to avoid the peak voltage of the ringing from exceeding the absolute maximum rating (60V). Furthermore, after a voltage spike occurs, ringing is also caused. In order to prevent erroneous detection of the secondary output voltage, the ringing must be converged within 250ns (Typ).

When the built-in N-Channel MOSFET turns ON, reverse spike voltage in the output diode is generated. Note that this spike voltage must not exceed the diode rating voltage.

(4) Winding Resistance

Either primary or secondary winding resistance will reduce overall power efficiency. Moreover, secondary winding resistance lowers the output voltage. Therefore, a transformer with smaller winding resistance is recommended.

(5) Saturation Current

The current in the primary transformer will not be transferred to the secondary if the core is saturated due to the exceeded current. When the core is saturated, the inductance value decreases and the current drastically increases. The current in the transformer should not exceed its rated saturation current.

5. Output Capacitor

Selecting the secondary side output capacitor value is important for a stable operation. Please select the value which fulfils below condition.

$$C_{OUT} = 1.6 \times 10^{-9} \times \frac{1}{L_P} \times \left(\frac{N_P}{N_S} \times Duty \right)^2 \quad [F]$$

where:

C_{OUT} is Output capacitor

In addition, as secondary side output voltage rises through soft start time (tss), please consider below equation when choosing an output capacitor. Over current protection operates due to the inrush current especially when the capacitance value is extremely large, thus, start-up failure might occur.

$$C_{OUT} \leq \frac{1}{2} \times \frac{t_{SS} \times \left\{ \left(I_{LIM_TM_IN} \times \frac{N_P}{N_S} \right) \times (1 - Duty) - I_{OUT_MAX} \right\}}{V_{OUT}} \quad [F]$$

where:

t_{SS} is Soft start time

6. Input Capacitor

Use ceramic capacitor for the input capacitor and place the input capacitor as close as possible to VIN terminal. Please refer to the "PCB Layout Design Guidelines" on page 19 for the design as malfunctions might occur due to the layout pattern or the position of the capacitor.

As for the capacitance value of the input capacitor, the ripple voltage of VIN terminal needs to be below 4% of the input voltage.

And, make sure that ripple voltage is suppressed when load changes or start up.

7. Output Diode

Since the forward voltage V_F of the output diode becomes an error factor in the output voltage, a Schottky barrier diode of small V_F is recommended. When selecting a diode, note that forward current must not exceed the rated values. And, when the built-in N-Channel MOSFET is ON, the output diode or reverse voltage V_R decrease is expressed by the following equation:

$$V_R = V_{IN} \times \frac{N_S}{N_P} + V_{OUT} \quad [V]$$

Furthermore, ringing occurs to the reverse voltage V_R when built-in N-Channel MOSFET turns ON. Please prevent the peak voltage from exceeding the rated value of the output diode.

8. Enable Voltage

This IC is shut down when SDX/EN voltage is below 0.9V (Typ).

If the voltage becomes above 2.0V (Typ) when SDX/EN terminal voltage is rising, IC goes to enable state and starts up. (Hysteresis voltage: 0.2V (Typ))

Enable control with VIN terminal is done by dividing the VIN terminal and GND terminal with R1 and R2 resistors connecting to SDX/EN terminal, as shown in Figure 25. The enable voltage when VIN is rising can be set with the following equation:

$$V_{VIN_ENAB\overline{LE}} = \frac{2.0V \times (R_1 + R_2)}{R_2} \quad [V]$$

Disable voltage when VIN is falling can be set with the following equation:

$$V_{VIN_DISAB\overline{LE}} = \frac{1.8V \times (R_1 + R_2)}{R_2} \quad [V]$$

Since the control system of this IC needs to operate with 50% duty or less, set disable voltage which fulfils the following equation:

$$V_{VIN_DISAB\overline{LE}} \geq \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad [V]$$

Please note that the clamping element inside the IC will turn ON and the inflow current occurs if the SDX/EN terminal voltage rises above 5V.

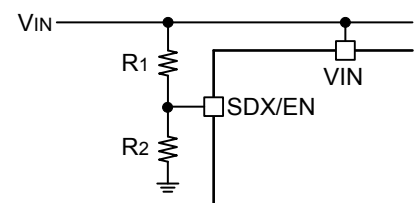


Figure .21 Enable Control with VIN terminal

9. Minimum Load Current

To achieve a stable output voltage, the built-in N-Channel MOSFET senses and feeds back information on the output voltage on the secondary side (which was isolated by the transformer) by using the SW terminal voltage on the primary side (during OFF time). Meaning, the output will not be regulated in any case unless the built-in N-Channel MOSFET is in the switching operation.

During light load, the switching operation uses minimum ON-Time. The output voltage may rise when there is a small load current since it will supply the least amount of energy to the secondary side output. Therefore, it is necessary to add a dummy resistor etc. to the output in order to secure minimum load current.

The required minimum load current (I_{OUT_MIN}) can be expressed by:

$$I_{OUT_MIN} = 7.5 \times 10^{-9} \times \left\{ \frac{V_{IN}^2}{L_P \times V_{OUT}} \right\} \quad [A]$$

10. Switching Frequency Changing Point

During light load, high efficiency is achieved by changing the switching frequency according to the load current.

The load current equation where the switching frequency begins to fall from the fixed 400kHz (Typ) is expressed following equation:

$$I_{OUT_fsw} = \frac{1}{2} \times \left\{ \frac{400kHz \times (V_{IN} \times t_{ON_MIN})^2}{L_P \times V_{OUT}} \right\} \quad [A]$$

where

t_{ON_MIN} is the Minimum On time

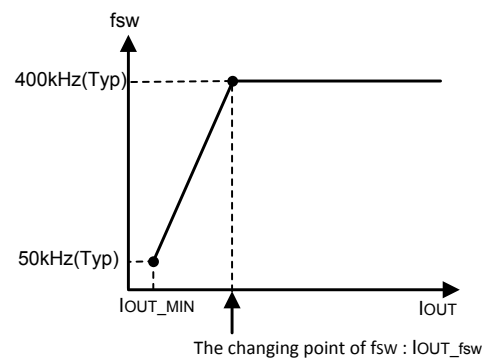


Figure 22. Switching Frequency vs Load Current Image

11. Load Compensation

The relational expression of V_{OUT} shows that V_F and ESR are the factors leading to poor load regulation. For an application which these factors cause the problem, an ideal load regulation can be obtained using load compensation function. Load compensation mechanism is explained below. In the application wherein output voltage accuracy in particular is not required, load compensation function can be cancelled by short-circuiting the COMP terminal to GND.

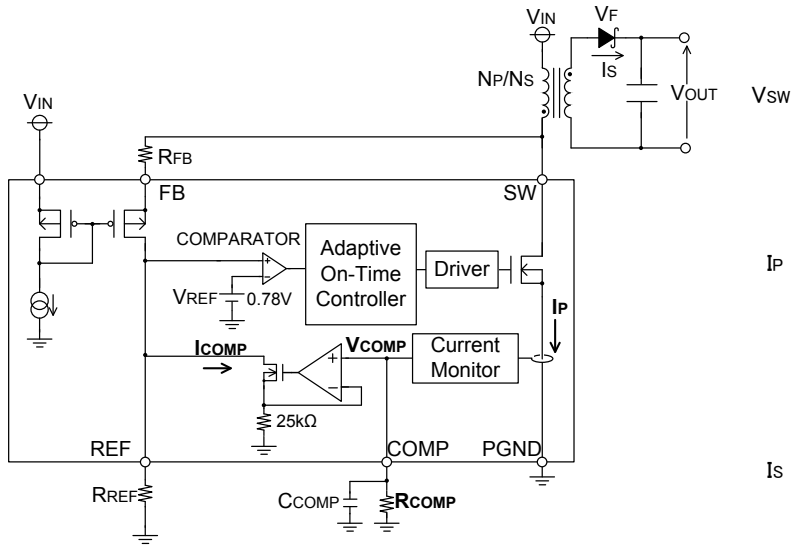


Figure 23. Load Compensation Functional Block Diagram

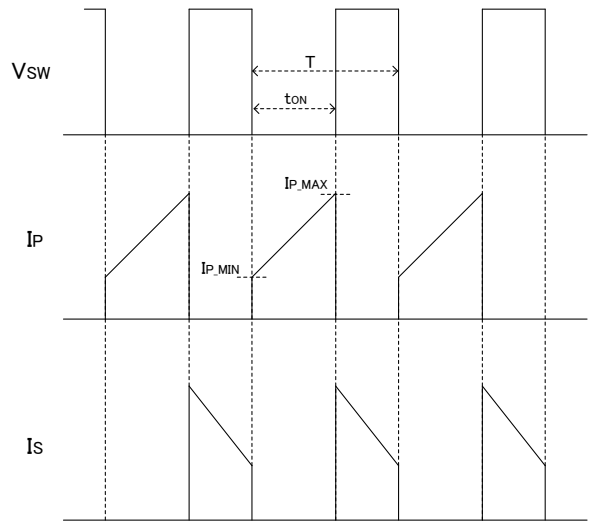


Figure 24. Monitor of the Amount of Load Compensation (Continuous Mode)

V_{OUT} voltage drop is compensated corresponding to the average current of the primary transformer current I_P .

Since I_P and I_S have a relationship as indicated in the following equation, the load compensation value is determined by assuming I_S from I_P and then adjusted by using external CR of the COMP terminal. The current of $K \cdot I_P$ is injected to the COMP terminal from the Current Monitor block in the Figure. 23 and then converted to V_{COMP} through R_{COMP} resistor externally attached to COMP terminal.

K here is the compression magnification and indicated as $1/50k$.

The upper limit of V_{COMP} operating voltage is limited in the internal circuit. Set R_{COMP} below $0.5V$.

$$I_P = \frac{N_S}{N_P} \times I_S \quad [A]$$

$$V_{COMP} = K \times I_P \times R_{COMP} \leq 0.5V$$

Steep changes in I_{COMP} may make the operation of the loop unstable.

Therefore, C_{COMP} is needed to stabilize V_{COMP} .

Recommended values of C_{COMP} are from $0.01\mu F$ to $0.1\mu F$. By the addition of C_{COMP} , V_{COMP} becomes:

$$\begin{aligned} V_{COMP} &= K \times R_{COMP} \times I_{P_AV} \\ &= K \times R_{COMP} \times \frac{I_{P_MIN} + I_{P_MAX}}{2} \times \frac{t_{ON}}{T} \quad [V] \end{aligned}$$

$$I_{COMP} = \frac{V_{COMP}}{25k\Omega} \quad [V]$$

where:

I_{P_ave} = Average transformer primary side current

R_{COMP} = External resistance for I_{COMP} adjustment

t_{ON} = ON-Time of built-in N-Channel MOSFET

How to decide the amount of load compensation and I_{COMP} setup by adjustment of R_{COMP} is explained next.

The feedback current which originally flows into R_{REF} is partially lost by I_{COMP} due to the load compensation function. As a result, in order to compensate this, the H level of V_{SW} increases and recovers the dropped output voltage.

While the load compensation function is not operating, V_{OUT} , as described previously, will now be:

$$V_{OUT} = \frac{R_{FB}}{R_{REF}} \times \frac{N_S}{N_P} \times V_{REF} - V_F - I_{S_AVE} \times ESR \quad [V]$$

where:

I_{S_AVE} is the average transformer secondary side current

When I_{COMP} occurs, the load compensation function operates and V_{OUT} becomes the following equation. The voltage V_{OUT} increases by I_{COMP} .

$$V_{OUT} = \frac{N_S}{N_P} \times \left(\frac{V_{REF}}{R_{REF}} + I_{COMP} \right) \times R_{FB} - V_F - I_{S_AVE} \times ESR \quad [V]$$

$$\frac{K \times R_{COMP} \times I_{P_AVE}}{25k\Omega} \times \frac{N_S}{N_P} \times R_{FB} = I_{S_AVE} \times R_{VF} + I_{S_AVE} \times ESR$$

In order to remove V_F and ESR by using I_{COMP} , the following equation is needed.

$$I_{COMP} \times \frac{N_S}{N_P} \times R_{FB} = V_F + I_{S_AVE} \times ESR$$

Next, linearity approximation of the change of V_F to I_S is carried out by R_{VF} , and R_{COMP} which adjusts I_{COMP} from the expression mentioned earlier is calculated.

$$\frac{K \times R_{COMP} \times I_{P_AVE}}{25k\Omega} \times \frac{N_S}{N_P} \times R_{FB} = I_{S_AVE} \times R_{VF} + I_{S_AVE} \times ESR$$

$$\frac{K \times R_{COMP}}{25k\Omega} \times \left(\frac{N_S}{N_P} \right)^2 \times R_{FB} = R_{VF} + ESR$$

$$R_{COMP} = 25k\Omega \times \frac{R_{VF} + ESR}{K \times R_{FB}} \times \left(\frac{N_P}{N_S} \right)^2 \quad [\Omega]$$

Although the setting of the theoretical value of R_{COMP} was shown, R_{VF} , ESR , and R_{FB} are dependent on the environment, such as used parts and the mounting board.

Therefore, when determining the actual value of R_{COMP} , monitor V_{OUT} in the used load current range and adjust R_{COMP} accordingly.

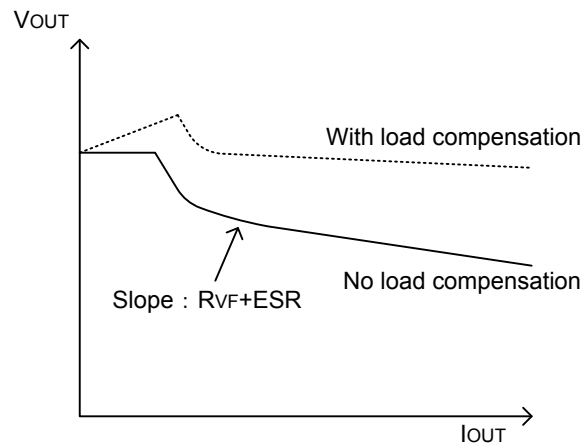
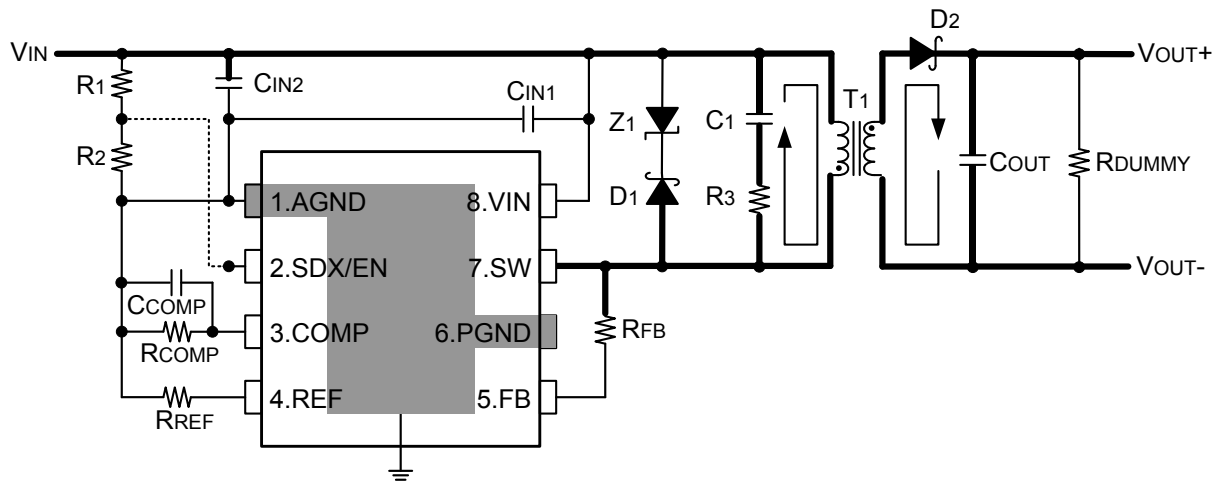


Figure 25. Load Compensation Image

PCB Layout Design Guidelines



The dotted line is the image of the wiring in another layer.

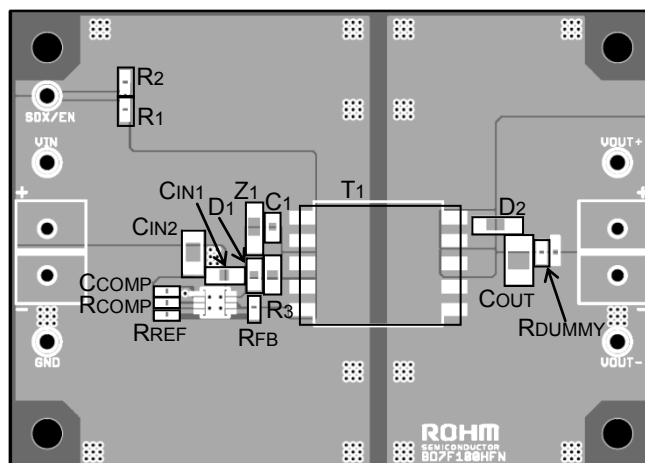
Figure 26. Application Circuit Block Diagram

PCB layout greatly affects the stable operation of the IC. Depending on the layout, the specs of the IC might not be secured or IC might not operate correctly.

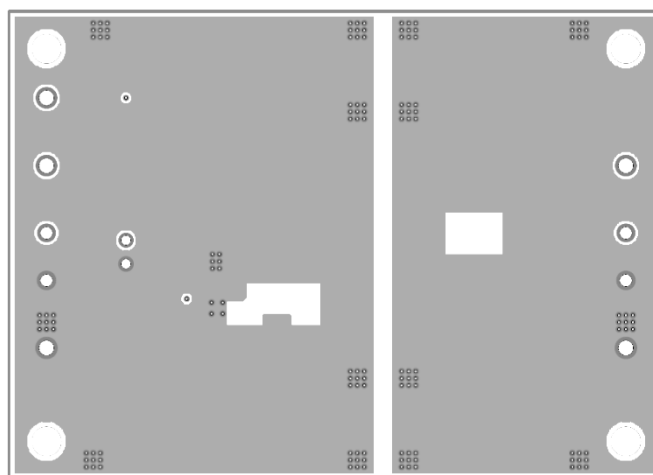
Please take the following points into consideration when designing the PCB layout.

1. Place input ceramic capacitors C_{IN1} and C_{IN2} as close as possible to VIN terminal on the same PCB surface with IC.
2. Shorten the thick line as short as possible with wide width pattern.
3. Place R_{REF} as close as possible to REF terminal.
4. Place R_{FB} as close as possible to FB terminal.
5. Place transformer T_1 close to SW terminal and make the current loop indicated as an arrow (primary side) short. In addition, make the pattern of the SW node as thick and short as possible.
6. Place output diode D_2 close to SW terminal and make the current loop indicated as an arrow (secondary side) short.
7. In case of multilayer board, do not place GND layer or VOUT- node pattern in the internal layer that is just below the SW node pattern and D_2 anode pattern.
8. R_{COMP} and C_{COMP} are for load compensation function. Short the COMP terminal to the GND when the load compensation function is not used.
9. Connect the exposed die pad to the GND plane.
10. Please note that temperature of the IC increase as BD7F200 has higher output power than BD7F100.

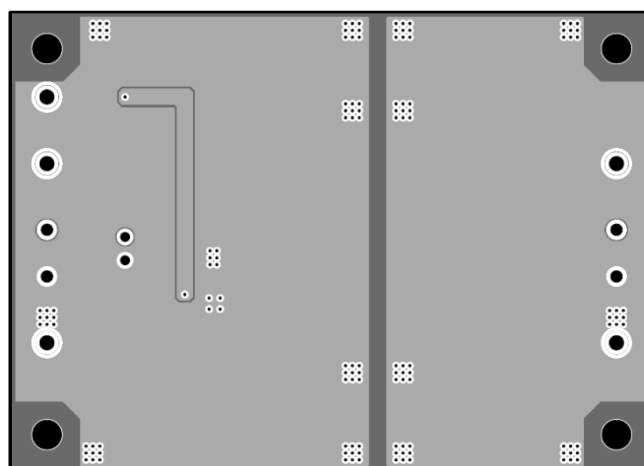
Reference Layout Pattern



Top Layer

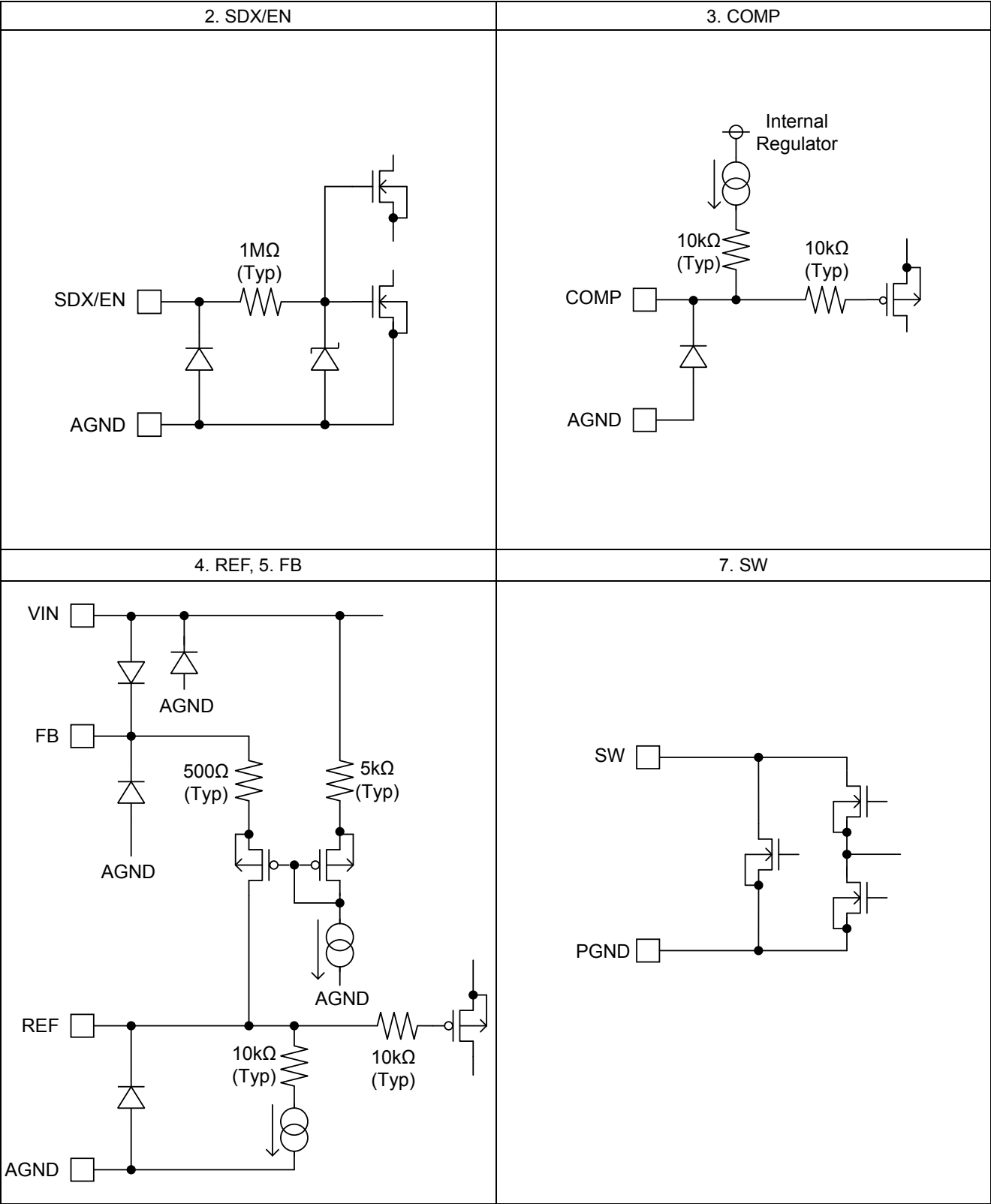


Middle Layer



Bottom Layer

I/O equivalent circuits



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

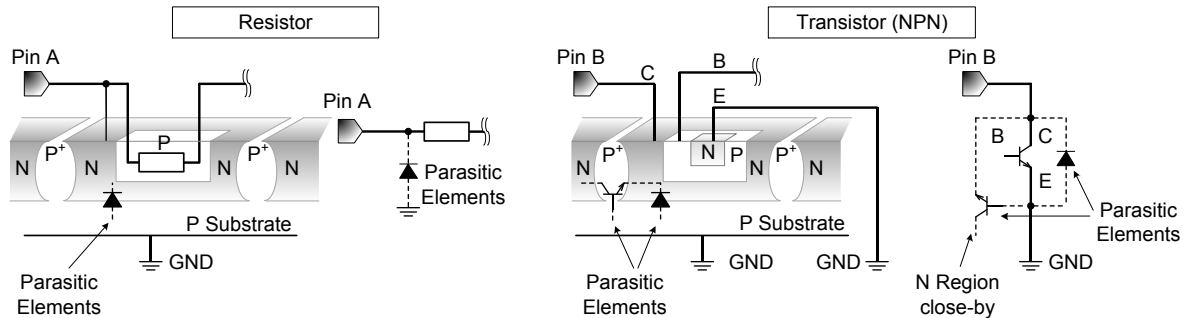


Figure 27. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

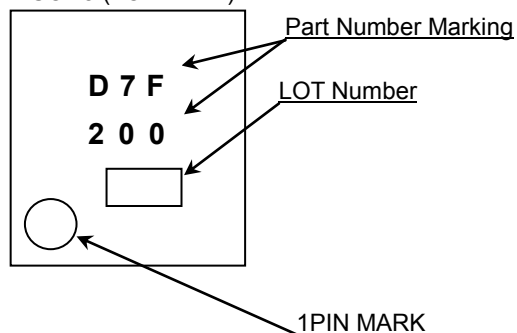
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

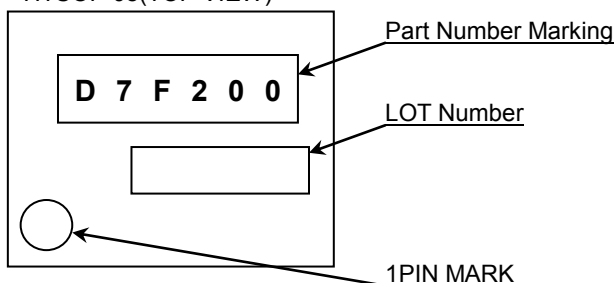
B D 7 F 2 0 0 H F N										-	LBTR		
Part Number										Package		Product class	
										HFN:HSO8		LB: For industrial applications	
										EFJ:HTSOP-J8		Packing, forming specification	
												TR: Embossed tape and reel	
												2500pcs (HSO8)	
												HR: Embossed tape and reel	
												250pcs (HSO8)	
												E2: Embossed tape and reel	
												3000pcs (HTSOP-J8)	
												H2: Embossed tape and reel	
												250pcs (HTSOP-J8)	

Marking Diagrams

HSO8 (TOP VIEW)



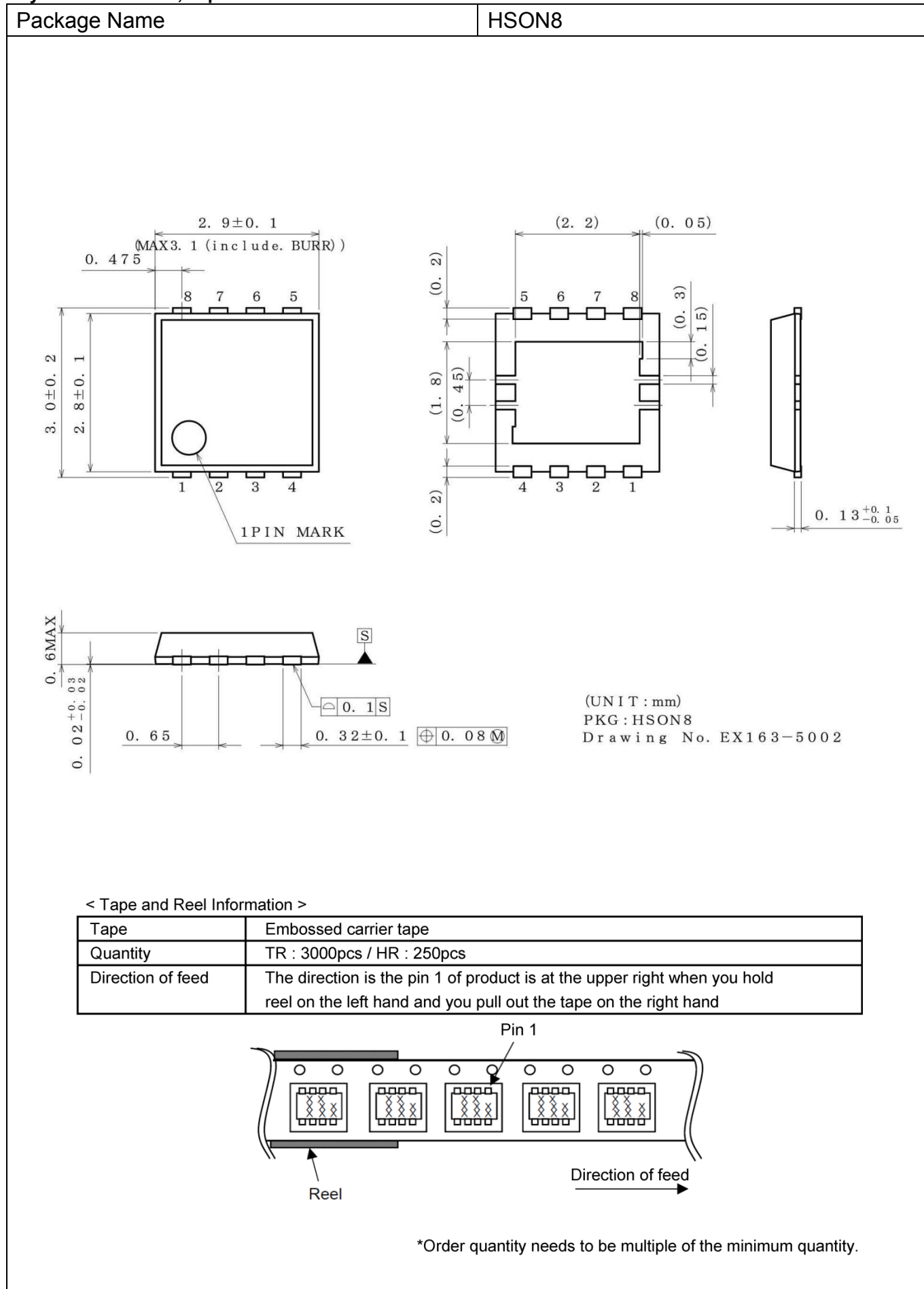
HTSOP-J8(TOP VIEW)



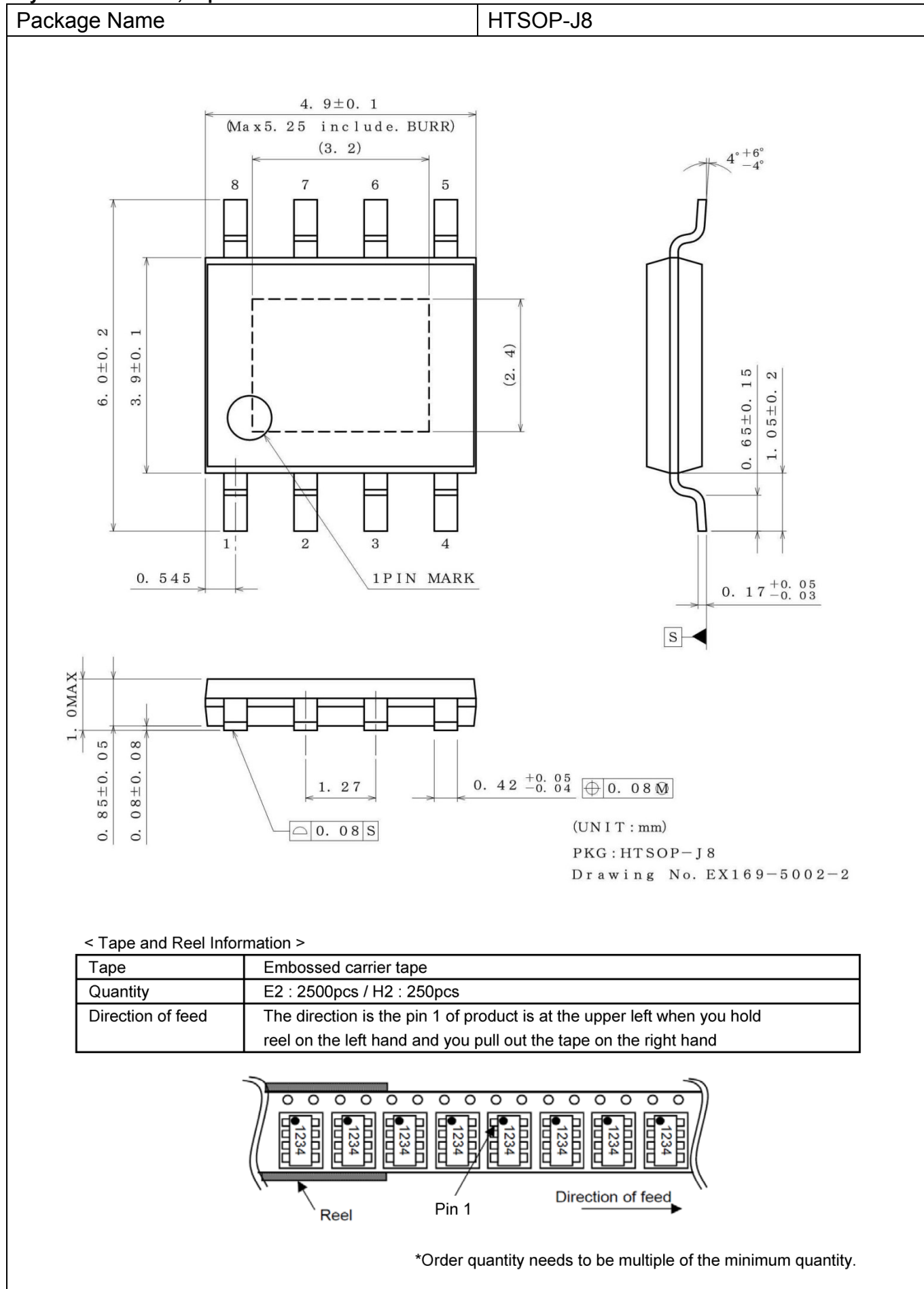
Line up

Package	Orderable Part Number
HSO8	BD7F200HFN-LBTR
	BD7F200HFN-LBHR
HTSOP-J8	BD7F200EFJ-LBE2
	BD7F200EFJ-LBH2

Physical Dimension, Tape and Reel Information



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
10.Mar.2016	001	New production
24.Mar.2016	002	Add BD7F200EFJ-LB(HTSOP-J8 Package)
17.April.2017	003	P.4 Modified FB terminal absolute voltage P.24 Add small lots format P.25 P.26 Add small lots format

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [d] the Products are exposed to high Electrostatic
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