M2764/M27128
(Military Temperature Range)
E2764/E27128
(Military Temperature Range)
2764/27128 EPROM
November 1989

Features

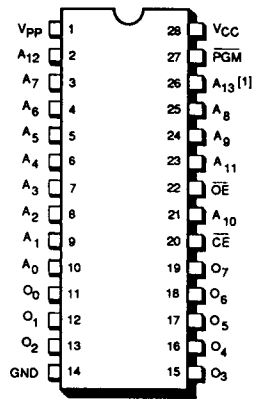
- **Military and Extended Temperature Range**
  - –55°C to +125°C: M2764
  - –55°C to +125°C: M27128
  - –40°C to +85°C: E2764/E27128
- **200 ns Access Times at –55°C to +125°C**
- **Programmed Using Intelligent Algorithm**
- **21 V V_{PP} Programming Voltage**
- **JEDEC Approved Bytewide Pin Configuration**
  - 2764 8K x 8 Organization
  - 27128 16K x 8 Organization
- **Low Power Dissipation**
  - 120 mA Active Current
  - 40 mA Standby Current
- **Silicon Signature®**

Description

SEEQ's 2764 and 27128 are ultraviolet light erasable EPROMs which are organized 8K x 8 and 16K x 8 respectively. They are specified over the military and extended temperature range and have access times as fast as 200 ns over the V_{CC} tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 120 mA and 40 mA respectively. The 200 ns allows higher system

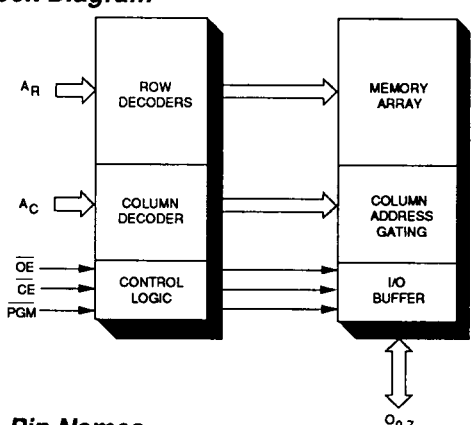
Pin Configuration

DUAL-IN-LINE
TOP VIEW
2764/27128



PIN 26 IS A NO CONNECT
ON THE DIP 2764.

Block Diagram



Mode Selection

MODE \ PINS	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon Signature*	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Silicon Signature: A_0 is toggled, A_9 = 12V, and all other addresses are at a TTL low.

Silicon Signature is a registered trademark of SEEQ Technology, Inc.

Pin Names

A_C	ADDRESSES – COLUMN (LSB)
A_R	ADDRESSES – ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS
$\overline{PGM}$	PROGRAM

efficiency by eliminating the need for wait states in today's 8 - or 16-bit micro-processors.

Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to V_{PP} and a TTL "0" to pin 27 (program pin). They may be programmed with an intelligent algorithm that is now available on commercial programmers. This faster time improves manufactoring throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, the 27128 and the 2764 may be programmed using the conventional 50 ms programming specification of older generation EPROMs.

Incorporated on the 27128 and 2764 is Silicon Signature. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage ..... −65°C to +150°C
Under Bias ..... −65°C to +135°C
All Inputs and Outputs
with Respect to Ground ..... +7 V to −0.6 V
V_{PP} During Programming
with Respect to Ground ..... +22 V to −0.6 V
Voltage on A_9
with Respect to Ground ..... +15.5 V to −0.6 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2764 M27128	E2764 E27128
V_{CC} Supply Voltage[1]	5V ± 10%	5V ± 10%
Temperature Range (Read Mode)	(Case) −55°C to +125°C	(Ambient) −40°C to 85°C
V_{PP} During Programming	21 ± 0.5 V	21 ± 0.5 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{IN}	Input Leakage Current		10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current		10	µA	$V_{OUT} = V_{CC}$ Max.
I_{PP}[2]	V_{PP} Current Read Mode		5	mA	$V_{PP} = V_{CC}$ Max.
	Prog. Mode (25°C)		30	mA	V_{PP} = 21.5 V
I_{CC1}[2]	V_{CC} Standby Current		40	mA	$\overline{CE} = V_{IH}$
I_{CC2}[2]	V_{CC} Active Current		120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA

NOTES:
1. V_{CC} must be appied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current is the sum of I_{CC} and I_{PP}.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec) E/M2764-20 E/M27128-20 Min.	Max.	E/M2764-25 E/M27128-25 Min.	Max.	E/M2764-35 E/M27128-35 Min.	Max.	M2764-45 Min.	Max.	Test Conditions
t_{AA}	Address Access Time		200		250		350		450	$\overline{CE}=\overline{OE}=V_{IL}$
t_{CE}	Chip Enable to Data Valid		200		250		350		450	$\overline{OE}=V_{IL}$
t_{OE}[2]	Output Enable to Data Valid		75		100		125		150	$\overline{CE}=V_{IL}$
t_{DF}[3]	Output Enable to Output Float	0	60	0	85	0	105	0	130	$\overline{CE}=V_{IL}$
t_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable, whichever occured first	0		0		0		0		$\overline{CE}=\overline{OE}=V_{IL}$

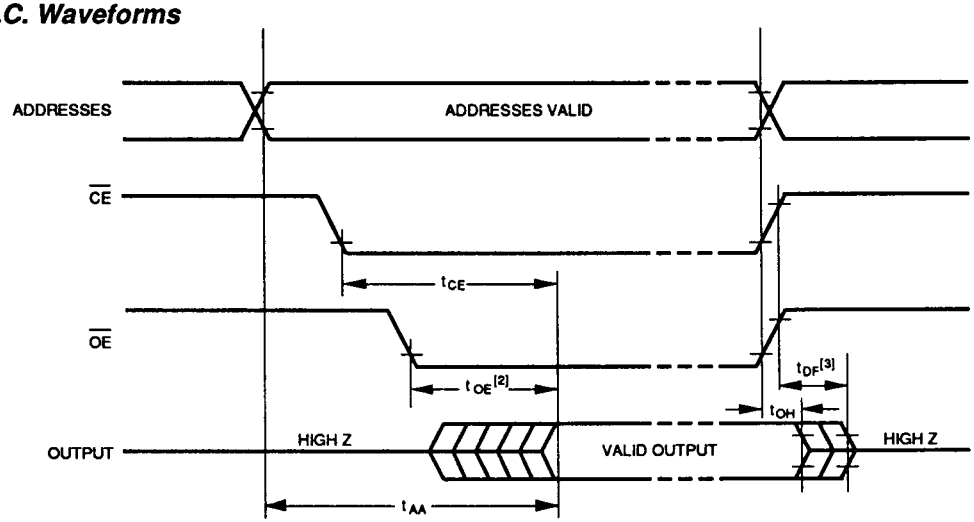
Capacitance [1]

Symbol	Parameter	Typ.	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0 V

Equivalent A.C. Test Conditions [4]

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20 ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. This parameter is sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
4. These are equivalent test conditions and actual test conditions are dependent on the tester.

Erasure Characteristics

The 2764 and 27128 are erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e. intensity x exposure time, for erasure is a minimum of 15 watt-second/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROMs Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. Silicon Signature allows programmers to match the programming specifications against the product which is to be programmed. If there is verification, the the programmer proceeds programming.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling (using TTL) the column address A_0. There are 2 bytes of data available. The data (see Table 2) appears on outputs O_0 to O_6, with O_7 used as an odd parity bit. This mode is functional at 25° ± 5°C ambient temperature.

Table 2. Silicon Signature Bytes

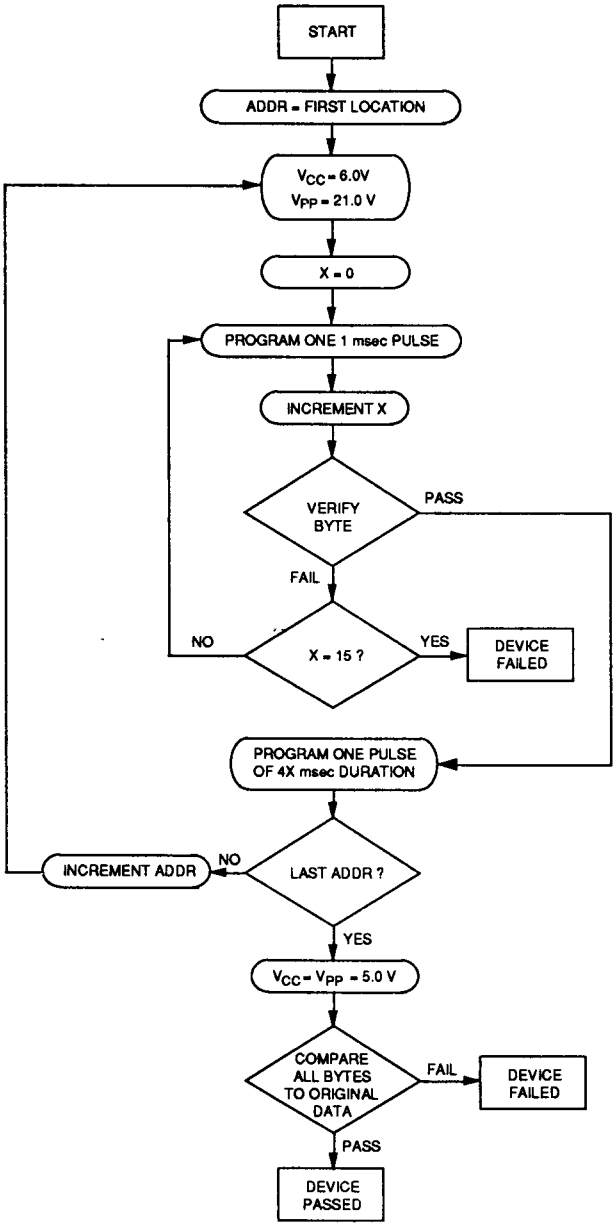
	A0	Data Hex
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)		
2764	V_{IH}	40
27128	V_{IH}	C1

Programming

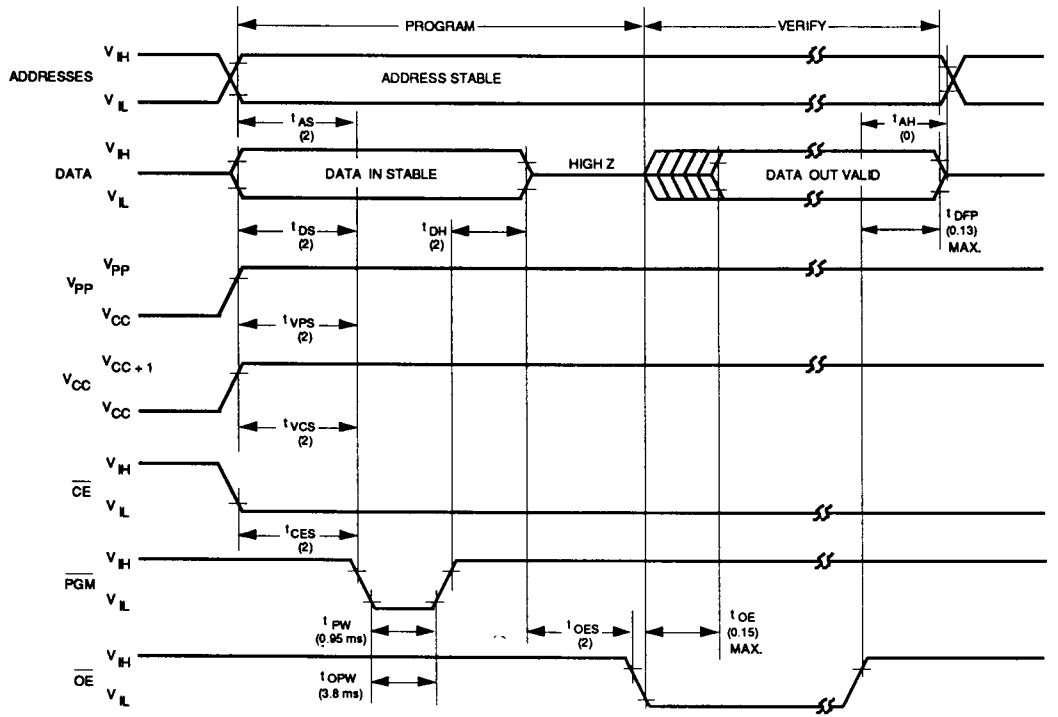
The EPROMs may be programmed using an intelligent algorithm or with a conventional 50 msec programming pulse. The intelligent algorithm improves the total programming time by approximately 10 times over the conventional 50 msec algorithm.

The intelligent algorithm requires V_{CC} = 6V and V_{PP} = 21V during byte programming. The initial program pulse width is one millisecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 4 times the number of one millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A maximum of 15 one millisecond pulses per byte should be applied to each address. When the intelligent algorithm cycle has been completed, all bytes must be read at $V_{CC} = V_{PP} = 5V$.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. All times shown in ( ) are minimum and in µsec unless otherwise specified.
2. The input timing reference level is .8V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Intelligent Algorithm

AC Programming Charateristics

TA =25° ± 5°C, V_{CC}[1,4] = 6.0 V ± 0.25 V, V_{PP} = 21 V ± 0.5 V

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			µs
t_{OES}	$\overline{OE}$ Setup Time	2			µs
t_{DS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{DH}	Data Hold Time	2			µs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			µs
t_{VCS}	V_{CC} Setup Time	2			µs
t_{PW}[2]	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[3,4]	$\overline{PGM}$ Overprogram Pulse Width	3.8		63	ms
t_{CES}	$\overline{CE}$ Setup Time	2			µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Initial Program Pulse width tolerance is 1 msec ± 5 %.
3. The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
4. For 50 ms programming, V_{CC} = 5 V ± 5%, T_{PW} = 50 ms ± 10 %, and T_{OPW} is not applicable.

Ordering Information