L6722

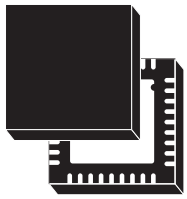
3 Phase controller for DC/DC converters

Features

- 2A integrated gate drivers
- 0.8V reference
- 1% output voltage accuracy
- Adjustable reference offset
- Precise current sharing and OCP across LS MOSFETS
- Constant over current protection
- Feedback disconnection
- LSLESS allows managing pre-bias startup
- Preliminary of protection
- Oscillator internally fixed at 100kHz, externally adjustable
- Power good
- Integrated remote sense buffer
- VFQFPN36 package with exposed pad

Applications

- Memory supply for server and workstation MBs
- High density DC / DC converters
- High current pol



VFQFPN36

Description

L6722 implements a three-phase step-down controller with 120º phase-shift between each phase with integrated high-current drivers in a compact VFQFPN36 package with exposed pad.

L6722 manages output voltages down to 0.8V with ±1% output voltage accuracy over line and temperature variations. Additional programmable offset can be added to the reference voltage with a single external resistor in order to perform margining tests.

The controller assures fast protection against load over current and over / under voltage. In case of over-current the system works in Constant Current mode until UVP. Preliminary OVP allows full load protection in case of startup with failed HS. Feedback-disconnection protection prevents from damaging the load in case of misconnections in the remote sense. Pre-bias start-up is also managed thanks to LSLESS.

Combined use of DCR and RdsON current sensing assures precision in voltage positioning (by reading droop current across inductors DCR) and safe current sharing and OCP per each phase (by reading the current across LS RdsON). Droop function can be anyway disabled to perform precise and load-insensitive regulation.

Order codes

Part number	Package	Packing
L6722	VFQFPN36	Tube
L6722TR	VFQFPN36	Tape & Reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical application circuit

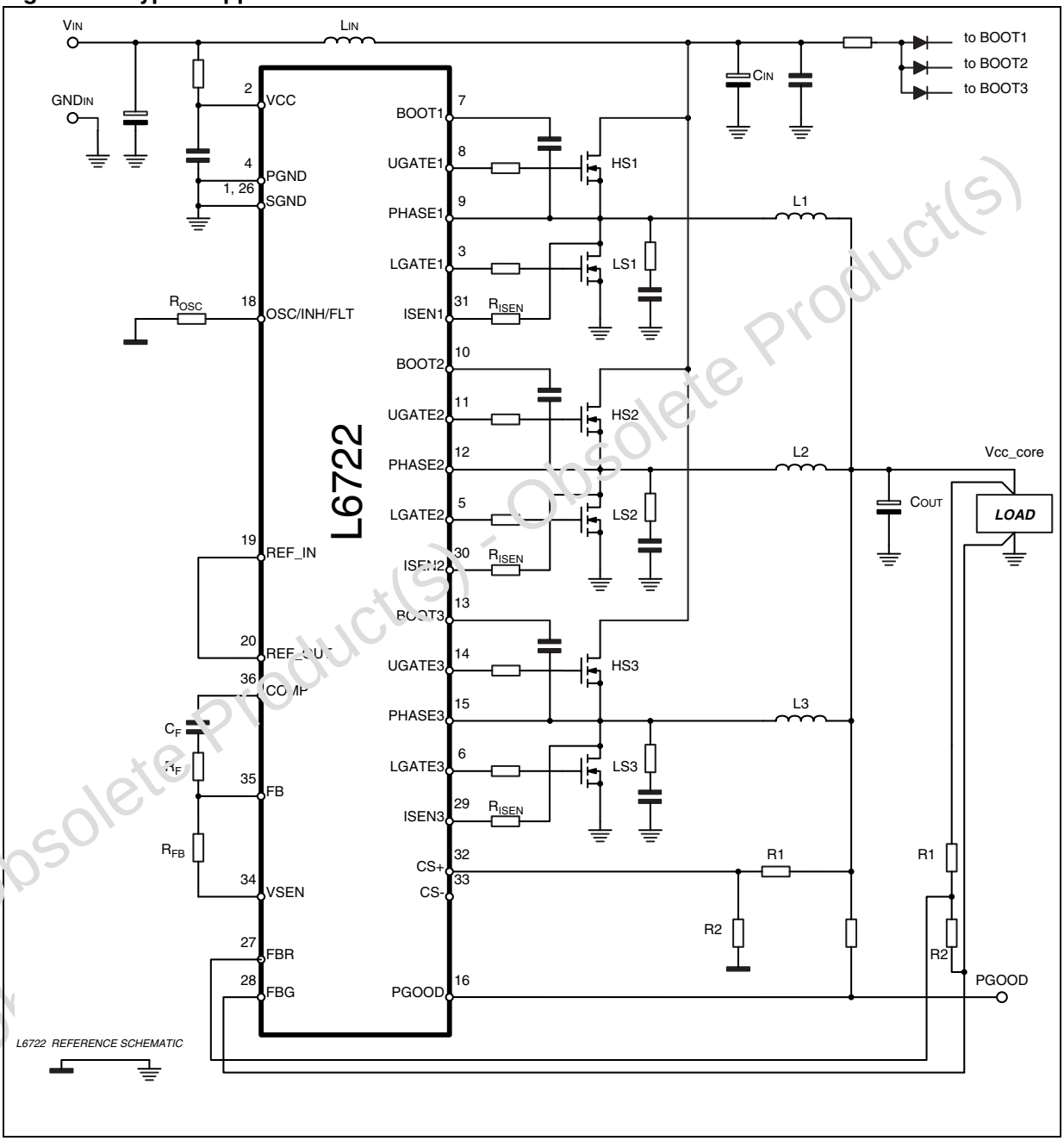
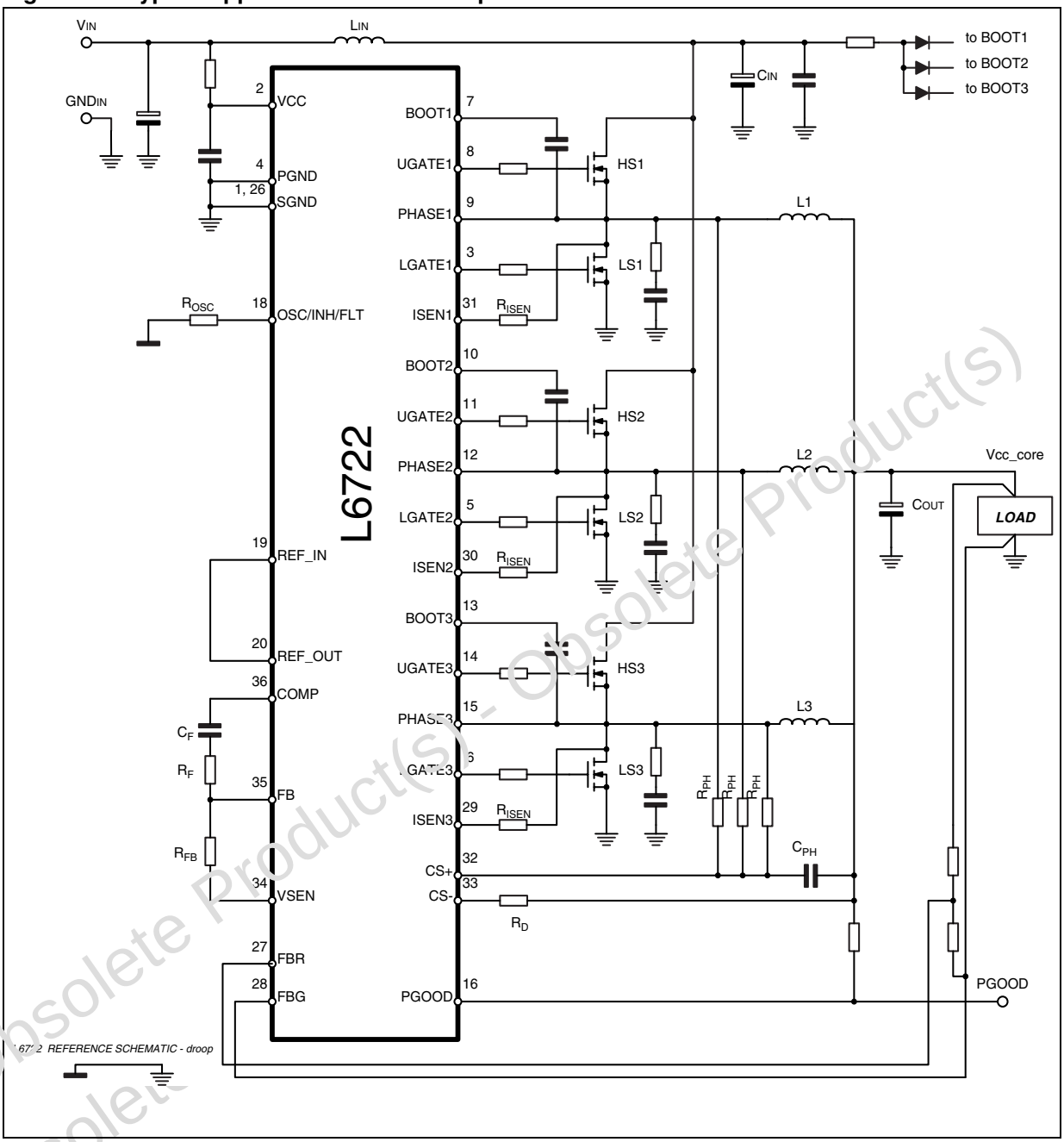
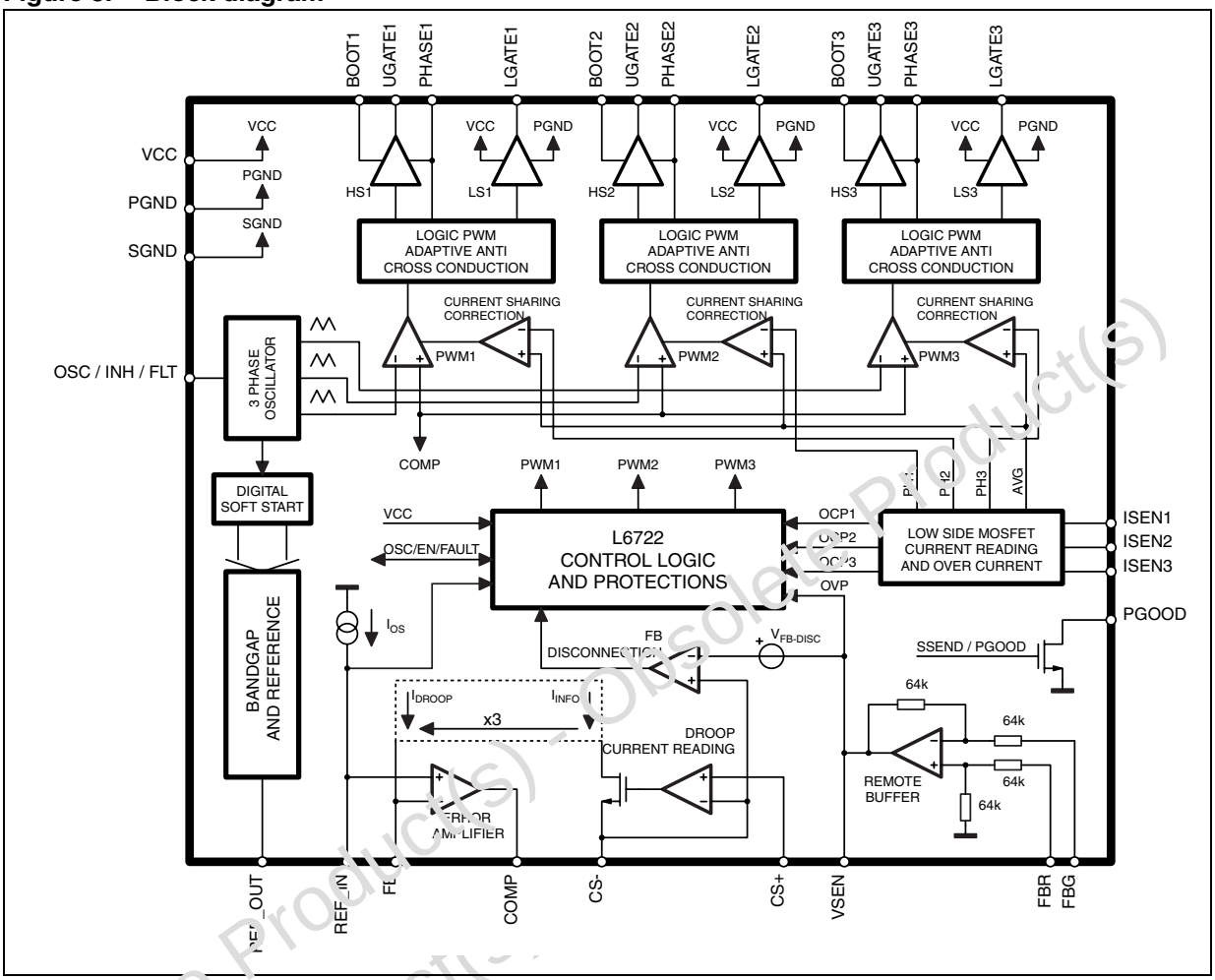


Figure 2. Typical application circuit - droop enabled



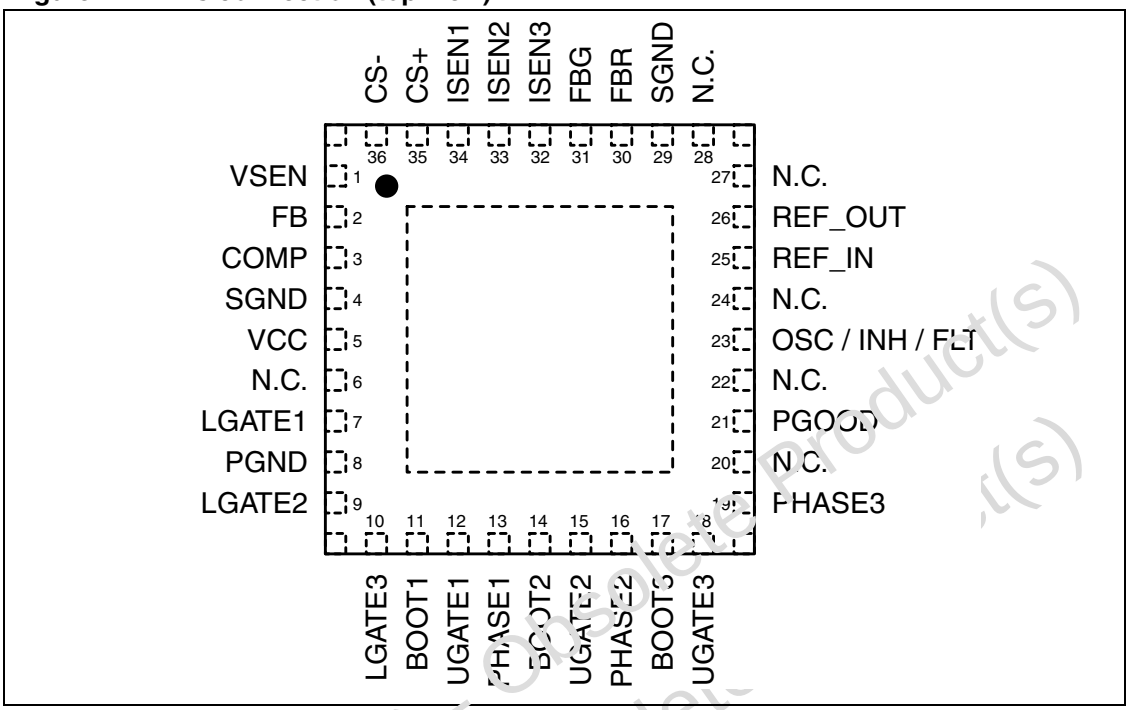
1.2 Block diagram

Figure 3. Block diagram



2 Pins description and connection diagrams

Figure 4. Pins connection (top view)



2.1 Pin description

Table 1. Pins description

Pin#	Name	Function
1	VSEN	Remote Buffer Output. It manages OVP and UVP protections and PGOOD. See *Section 9* for details.
2	FB	Error Amplifier Inverting Input. Connect with a resistor R_{FB} vs. VSEN and with an R_F - C_F vs. COMP.
3	COMP	Error Amplifier Output. Connect with an R_F - C_F vs. FB. The device cannot be disabled by pulling down this pin.
4	SGND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
5	VCC	Device Power Supply as well as LS driver supply. Operative voltage is 12V ±15%. Filter with at least 1µF MLCC vs. ground.
6	N.C.	Not Internally Bonded.
7	LGATE1	Channel 1 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
8	PGND	LS Driver return path. Connect to Power ground Plane.

Table 1. Pins description (continued)

Pin#	Name	Function
9	LGATE2	Channel 2 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
10	LGATE3	Channel 3 LS Driver Output. A small series resistor helps in reducing device-dissipated power.
11	BOOT1	Channel 1 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE1 and provide necessary Bootstrap diode. A small series resistor before the boot diode helps in reducing Boot capacitor overcharge.
12	UGATE1	Channel 1 HS driver output. A small series resistors helps in reducing device-dissipated power.
13	PHASE1	Channel 1 HS driver return path. It must be connected to the HS1 mosfet source and provides return path for the HS driver of channel 1.
14	BOOT2	Channel 2 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE2 and provide necessary Bootstrap diode. A small series resistor before the boot diode helps in reducing Boot capacitor overcharge.
15	UGATE2	Channel 2 HS driver output. A small series resistors helps in reducing device-dissipated power.
16	PHASE2	Channel 2 HS driver return path. It must be connected to the HS2 mosfet source and provides return path for the HS driver of channel 2.
17	BOOT3	Channel 3 HS driver supply. Connect through a capacitor (100nF typ.) to PHASE3 and provide necessary Bootstrap diode. A small series resistor before the boot diode helps in reducing Boot capacitor overcharge.
18	UGATE3	Channel 3 HS driver output. A small series resistors helps in reducing device-dissipated power.
19	PHASE3	Channel 3 HS driver return path. It must be connected to the HS3 mosfet source and provides return path for the HS driver of channel 3.
20	N.C.	Not Internally Bonded.
21	PGOOD	Open Drain Output set free after SS has finished and pulled low when VSEN is lower than the relative threshold. Pull up to a voltage lower than 5V (typ), if not used it can be left floating.
22	N.C.	Not Internally Bonded.

Table 1. Pins description (continued)

Pin#	Name	Function
23	OSC / INH / FLT	Three functional pin: ***OSC:*** It allows programming the switching frequency F_{SW} of each channel: the equivalent switching frequency at the load side results in being tripled. Frequency is programmed according to the resistor connected from the pin vs. SGND or VCC with a gain of 4kHz/µA (see relevant section for details). Leaving the pin floating programs a switching frequency of 100kHz per phase (300kHz on the load). ***INH:*** Forced low, the device stops operations with all mosfets OFF: all the protections are disabled except for *Preliminary over voltage*. It resets the device from any latching condition. ***FLT:*** The pin is forced high (5V) to signal an OVP FAULT: to recover from this condition, cycle VCC or the OSC pin. See *Section 10* for details.
24	N.C.	Not Internally Bonded.
25	REF_IN	REFrence INput for the regulation. Connect directly or through a resistor to the REF_OUT pin. See *Section 7.1* for details.
26	REF_OUT	REFrence OUTput. Connect directly or through a resistor to the REF_IN pin. See *Section 7.1* for details.
27, 28	N.C.	Not Internally Bonded.
29	SGND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
30	FBR	Remote Buffer Non Inverting Input. Connect to the positive side of the load to perform remote sense. See *Section 12* for proper layout of this connection.
31	FBG	Remote Buffer Inverting Input. Connect to the negative side of the load to perform remote sense. See *Section 12* for proper layout of this connection.
32 to 34	ISEN3 to ISEN1	LS Current Sense Pins. These pins are used for current balance phase-to-phase as well as for the system OCP. Connect through a resistor Rg to the relative PHASEx pin. See *Section 6* and *Section 9.6* for details.
35	CS+	Droop Current Sense non-inverting input. Connect through R-C network to the main inductors. See *Section 7.1* for details.
36	CS-	Droop Current Sense inverting input. Connect through resistor R_D to the main inductors common node. See *Section 7.1* for details. This pin also monitor the feedback disconnection. See *Section 9.4* for details.
PAD	THERMAL PAD	Thermal pad connects the Silicon substrate and makes good thermal contact with the PCB to dissipate the power necessary to drive the external mosfets. Connect to the PGND plane with several VIAs to improve thermal conductivity.

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal Resistance Junction to Ambient (Device soldered on 2s2p PC Board)	30	°C/W
T_{MAX}	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-40 to 150	°C
T_J	Junction Temperature Range	-40 to 125	°C
P_{TOT}	Maximum Power Dissipation at T_A = 25°C	3.5	W

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	to PGND	15	V
V_{BOOTx} - V_{PHASEx}	Boot Voltage	15	V
V_{UGATEx} - V_{PHASEx}		15	V
	LGATEx, PHASEx, to PGNDx	-0.3 to VCC + 0.3	V
	All other Pins to PGNDx	-0.3 to 7	V
V_{PHASEx}	Positive Peak Voltage; T<20ns @ 600kHz	26	V
	Negative Peak Voltage	TBD	V

3.2 Electrical characteristics

Table 4. Electrical characteristics
(V_{CC} = 12V±15%, T_J = 0°C to 70°C unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC Supply current	HGATEx and LGATEx = OPEN BOOTx = 12V		17		mA
I_{BOOTx}	BOOTx Supply Current	HGATEx = OPEN; PHASEx to PGNDx; BOOTx = 12V		0.7		mA
$UVLO_{VCC}$	VCC Turn-ON	VCC Rising			9.2	V
	VCC Turn-OFF	VCC Falling	7			V
$UVLO_{OVP}$	Pre-OVP Turn-ON	VCC Rising			3.8	V
	Pre-OVP Turn-OFF	VCC Falling	3			V
Oscillator and inhibit						
F_{SW}	Main Oscillator Accuracy	OSC = OPEN OSC = OPEN; T_J = 0°C to 125°C	90		110	kHz
INH_{IL}	Disable Thresholds		0.5			V
d_{MAX}	Maximum Duty Cycle	OSC = OPEN; I_{ISENx} = 0µA		80		%
		OSC = OPEN; I_{ISENx} = 35µA		40		%
ΔV_{OSC}	PWMx Ramp Amplitude			3		V
FLT	Voltage at Pin OSC	OVP Active		5		V

Table 4. Electrical characteristics (continued)
(V_{CC} = 12V±15%, T_J = 0°C to 70°C unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Reference						
k_{REF}	Output Voltage Accuracy	FBR = V_{OUT}; FBG = GND_{OUT};	-1		1	%
Error amplifier and remote buffer						
A_0	EA DC Gain			80		dB
SR	Slew Rate	COMP = 10pF to SGND		15		V/µs
	RB DC Gain			1		V/V
CMRR	Remote Buffer Common Mode Rejection Ratio			40		dB
Differential current sensing and offset						
I_{OCTH}	Over Current Threshold			35		µA
k_{IDROOP}	Droop Current Deviation	I_{DROOP} = 0 to 105µA; R_D=5.1kΩ	-3		3	µA
I_{OFFSET}	Offset Current		10	12	14	µA
Gate drivers						
t_{RISE_UGATEx}	HS Rise Time	BOOTx - PHASEx = 10V; C_{UGATEx} to PHASEx = 3.3nF		15		ns
I_{UGATEx}	HS Source Current	BOOTx - PHASEx = 10V		1.5		A
R_{UGATEx}	HS Sink Resistance	BOOTx - PHASEx = 12V		2.5		Ω
t_{RISE_LGATEx}	LS Rise Time	VCC = 10V; C_{LGATEx} to PGNDx = 5.6nF		20		ns
I_{LGATEx}	LS Source Current	VCC = 10V		1.5		A
R_{LGATEx}	LS Sink Resistance	VCC = 12V		1.8		Ω
Protections						
OVP		VSEN Rising	1.085	1.120	1.155	V
Pre-OVP	Preliminary Over voltage Protection	FBR Rising		1.25		V
		Hysteresis		300		mV
$V_{FB\text{-}DISC}$	FB Disconnection	V_{CS-} Rising, above VSEN		1.375		V
UVP	Under Voltage Protection	VSEN Falling, vs. REF_IN	-250	-300	-350	mV
PGOOD	PGOOD Threshold	VSEN Falling, vs. REF_IN	-100	-150	-200	mV
V_{PGOOD}	Voltage Low	I = -4mA			0.4	V

4 Device description

L6722 is multi-phase PWM controller with embedded high current drivers that provides complete control logic and protections for a high performance step-down DC-DC voltage regulator. Multi-phase buck is the simplest and most cost-effective topology employable to satisfy the increasing current demand of the modern high current DC/DC converters and POLs requirements. It allows distributing equally load and power between the phases using smaller, cheaper and most common external power mosfets and inductors. Moreover, thanks to the equal phase-shift between each phase, the input and output capacitor count results in being reduced. Phase interleaving causes in fact input rms current and output ripple voltage reduction and show an effective output switching frequency increase: the 100kHz free-running frequency per phase, externally adjustable through a resistor, results multiplied on the output by the number of phases.

The device comes with a fixed 0.8V reference that guarantee the output regulated voltage to be within ±1%; the output voltage is then adjustable through a resistor divider between FBR and FBG. OFFSET may be added to the main reference so allowing the device to be tested for margining during the system production. In addition, droop function may be enabled to perform precise voltage positioning according to the delivered current.

SS is performed by increasing the reference in 2048 clock cycles in closed loop regulation.

L6722 provides a complete set of protections to avoid damaging the load in any operative and non-operative conditions:

- Over-Voltage protection protects the load from dangerous over stress latching immediately the lower driver ON and driving high the FAULT pin.
- Preliminary OVP protection also allows the device to protect the load from dangerous OVP when VCC is not above the UVLO threshold.
- UVP protection latches the device and drives high the FAULT pin.
- Over-Current protection is provided with an OC threshold for each phase; when set, it causes the device to enter in constant current mode until the latched UVP.
- Low-Side-Less start-up allows the device to perform soft-start over pre-biased output avoiding dangerous current return through the main inductors as well as negative spike at the load side and allowing the device to work in redundant systems.

A compact VFQFPN36 package with exposed thermal pad allows dissipating the power to drive the external mosfet through the system board.

5 Driver section

The integrated high-current drivers allow using different types of power MOS (also multiple MOS to reduce the equivalent RdsON), maintaining fast switching transition.

The drivers for the high-side mosfets use BOOTx pins for supply and PHASEx pins for return. The drivers for the low-side mosfets use the VCC pin for supply and PGND pin for return.

The controller embodies a anti-shoot-through and adaptive dead-time control to minimize low side body diode conduction time maintaining good efficiency saving the use of Schottky diodes: when the high-side mosfet turns off, the voltage on its source begins to fall; when the voltage reaches 2V, the low-side mosfet gate drive is suddenly applied. When the low-side mosfet turns off, the voltage at LGATEx pin is sensed. When it drops below 1V, the high-side mosfet gate drive is suddenly applied. If the current flowing in the inductor is negative, the source of high-side mosfet will never drop. To allow the low-side mosfet to turn-on even in this case a watchdog controller is enabled: if the source of the high-side mosfet doesn't drop, the low side mosfet is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: 5V, 12V bus or any bus that allows the conversion (See *Section 7.3*) can be chosen freely.

5.1 Power dissipation

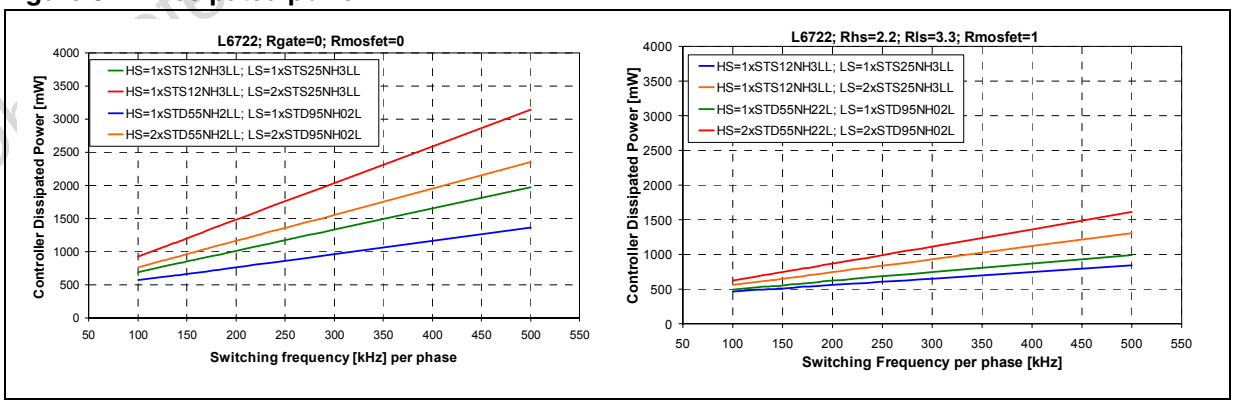
L6722 embeds high current mosfet drivers for both high side and low side mosfets: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature. In addition, since the device has an exposed pad to better dissipate the power, the thermal resistance between junction and ambient consequent to the layout is also important: thermal pad need to be soldered to the PCB ground plane through several VIAs in order to facilitate the heat dissipation.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device Power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow (assuming to supply HS and LS drivers with the same VCC of the device):

$$P_{DC} = V_{CC} \cdot (I_{CC} + 3 \cdot I_{BOOTx})$$

Figure 5. Dissipated power



- Drivers' power is the power needed by the driver to continuously switch on and off the external mosfets; it is a function of the switching frequency and total gate charge of the selected mosfets. It can be quantified considering that the total power P_{SW} dissipated to switch the mosfets (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic mosfet resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation. The total power dissipated to switch the mosfets results:

$$_{SW} = 3 \cdot F_{SW} \cdot (Q_{GHS} \cdot V_{BOOT} + Q_{GLS} \cdot V_{CC}$$

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

6 Current sharing loop and current reading

L6722 embeds two separate Current-Reading circuitries used to perform Current-Sharing and OCP through ISENx pins and Voltage-Positioning through CS+ and CS- pins (See *Section 7*).

Current-sharing control-loop and connections are reported in *Figure 6*: the current read through the I_{SENx} pins is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / 3$ is internally built into the device. The error between the read current I_{INFOx} and the reference I_{AVG} is then converted into a voltage that with a proper gain is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

The current flowing trough each phase is read using the voltage drop across the low-side mosfets R_{dsON} or across a sense resistor in its series and it is internally converted into a current. The trans-conductance ratio is issued by the external resistor R_{ISEN} placed outside the chip between I_{SENx} and the reading point (usually the LS mosfet Drain).

The current sense circuit tracks the current information for a time T_{TRACK} centered in the middle of the LS conduction time and holds the tracked information during the rest of the period. The current that flows from the I_{SENx} pin is the current information used by the device to perform current sharing and OCP and it is given by:

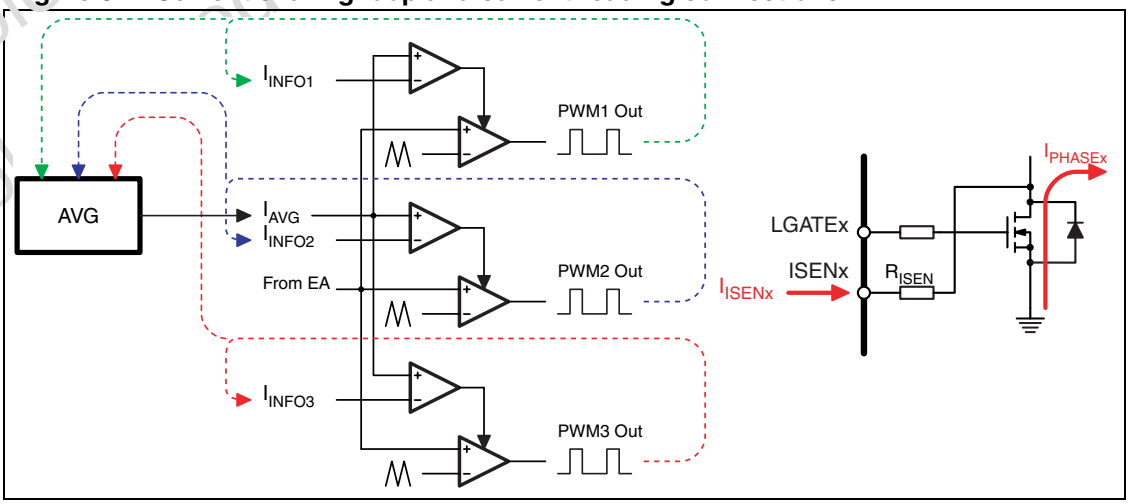
$$I_{ISENx} = \frac{R_{dsON}}{R_{ISEN}} \cdot I_{PHASEx} = I_{INFOx}$$

where R_{dsON} is the ON resistance of the low side mosfet and R_{ISEN} is the trans-conductance resistor connected between the ISENx pins and the LS Drain; I_{PHASEx} is the current carried by the relative phase and I_{INFOx} is the current information signal reproduced internally.

R_{ISENx} is designed according to the Over Current Protection: see *Section 9.6* for details.

Caution: Asymmetries in the R_{ISENx} values are allowed in order to create intentional current-unbalance so that one phase can carry higher currents or support different cooling. To increase the current in any of the phases, the value of the related R_{ISEN} can be slightly increased starting from the theoretical value extracted from the above reported relationships. Start from the coolest phase first to get the thermal balance.

Figure 6. Current sharing loop and current reading connections



7 Output voltage positioning

Output voltage positioning is performed by programming the external resistor divider and by correctly designing Droop Function and Offset to the reference (Optional). The output voltage is then driven by the following relationship (See *Figure 7*):

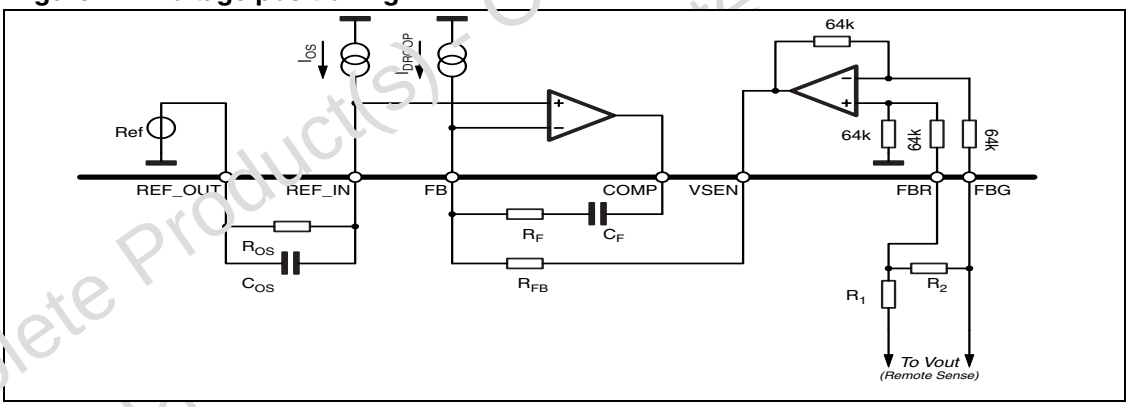
$$V_{OUT} = (Ref) \cdot \frac{R1 + R2}{R2}$$

Both DROOP and OFFSET function can be disabled: see *Section 7.1* and *Section 7.2* for details.

L6722 embeds a Remote Sense Buffer to sense remotely the regulated voltage without any additional external components. In this way, the output voltage programmed is regulated between the remote buffer inputs compensating for board and connector losses. The device senses the output voltage remotely through the pins FBR and FBG (FBR is for the regulated voltage sense while FBG is for the ground sense) and reports this voltage internally at VSEN pin with unity gain eliminating the errors. Keeping the FBR and FBG traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

When regulating output voltages higher than the reference, it is possible to insert a resistor divider between FBR, FBG and the regulated voltage as reported in *Figure 7*. In this case it is important for the external divider to have a value negligible with respect to the remote buffer impedance that has 64k resistors.

Figure 7. Voltage positioning

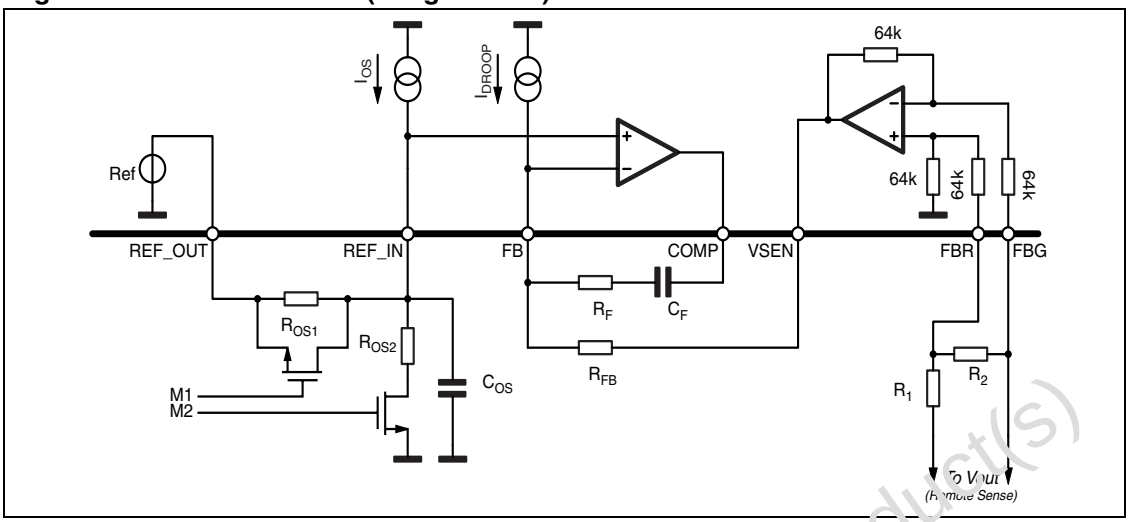


7.1 Offset and margining-mode (optional)

Positive / negative offset can be added to the programmed reference by connecting proper network resistor between the REF_OUT and REF_IN pins. In this way is possible to manage margining-mode by adding small offsets (positive or negative) to the regulated voltage, in order to test the loading-circuitry in different operative conditions to check for the reliability of the system designed.

Referring to *Figure 8*, a constant current (I_{OS}=12µA) is sourced from the REF_IN pin as soon as the device is enabled. By correctly designing R_{OS1} and R_{OS2}, positive and negative offset may be added to the reference voltage according to the status of the control signals M1 and M2. Different operating conditions can be then considered:

Figure 8. Offset definition (margin mode)



- No Offset (M1=1; M2=0)
- Positive Margin (M1=0; M2=0) $V_{REFIN} = Ref + I_{OS} \cdot R_{OS1}$
- Negative Margin (M1=0; M2=1) $V_{REFIN} = (Ref + I_{OS} \cdot R_{OS1}) \cdot \frac{R_{OS2}}{R_{OS1} + R_{OS2}}$

Offset resistors may be simply defined as follow:

$$R_{OS1} = \frac{V_{TARGET-POS} - Ref}{I_{OS}} \qquad R_{OS2} = R_{OS1} \cdot \frac{V_{TARGET-POS}}{V_{TARGET-POS} - V_{TARGET-NEG}}$$

where $V_{TARGET-POS}$ and $V_{TARGET-NEG}$ are the target voltages for positive and negative margin mode.

Offset current is always sourced from REF_IN pin: to avoid having steps during soft-start, the introduction of C_{OS} is required. The resulting time-constant need to be negligible with respect to the soft-start time as well as long enough to smooth the initial step. Typical values are in the range of few tens / hundreds of nF.

Offset function can be easily disabled by shorting REF_IN and REF_OUT together.

Warning: Maximum offset must be limited to less than 200mV to avoid setting the OVP protection resulting in a maximum +25% margin.

7.2 Droop function (optional)

This method "recovers" part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current: a static error proportional to the output current causes the output voltage to vary according to the sensed current.

Figure 9 shows the Current Sense Circuit used to implement the Droop Function. The current flowing across the three inductors is read through the R_{PH} - C_{PH} filter across CS+ and CS- pins. R_D programs a transconductance gain and generates a current I_{CS} proportional to the average of the currents of the three phases. The current I_{CS} is then mirrored and, multiplied by three, sourced by the FB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope.

Time constant matching between the inductor (L / DCR) and the current reading filter ($R_{PH} \cdot C_{PH}$) is required to implement a real equivalent output impedance of the system so avoiding over and/or under shoot of the output voltage as a consequence of a load transient. In fact, considering the scheme reported on *Figure 9*, it is possible to observe that:

$$s = \frac{I_{OUT}}{3} \cdot \frac{1 + s \cdot L / DCR}{1 + s \cdot R_{PH} \cdot C_{PH} / 3} \cdot \frac{DC}{R_{}}$$

By applying the time constant matching concept, it results:

$$\frac{L}{DCR} = \frac{R_{PH} \cdot C_{PH}}{3} \Rightarrow I_{CS} = \frac{I_{OUT}}{3} \cdot \frac{DCR}{R_D}$$

The device forces $I_{DROOP} = I_{CS} \times 3$, proportional to the read current, into the feedback resistor R_{FB} implementing the load regulation dependence. The output characteristic vs. load current is then given by (Offset disabled):

$$_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_D} \cdot I_{OUT} = VID - R_{L} \cdot I_{O}$$

Where R_{LL} is the resulting load-line resistance implemented by the system.

The whole power supply can be then represented by a "real" voltage generator with an equivalent output resistance R_{LL} and a voltage value of VID.

R_{FB} resistor can be then designed according to the R_{LL} specifications as follow:

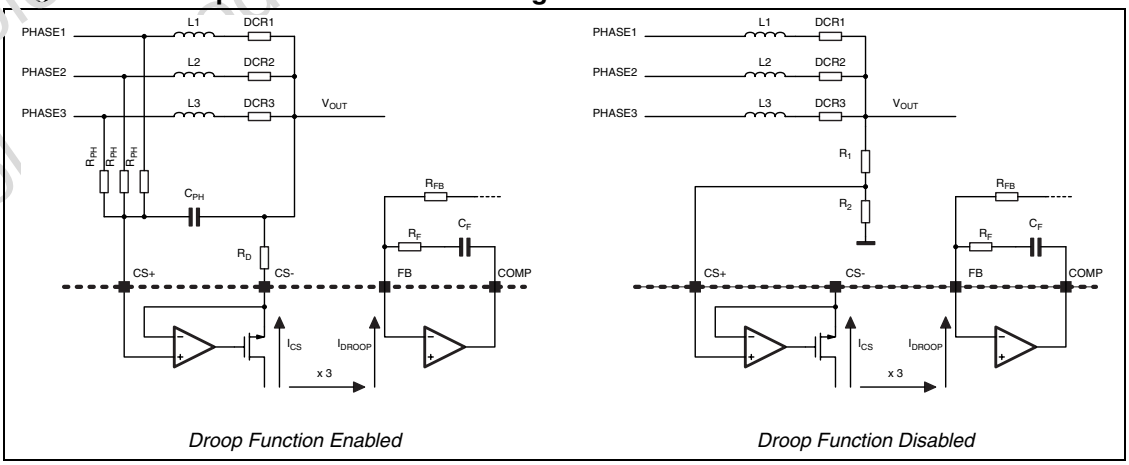
$$R_{FB} = R_{LL} \cdot \frac{R_D}{DCR}$$

Warning: Droop function is operational for output voltages up to 1.8V.

Caution: Droop function is optional, in case it is not desired, the Current Sense circuit can be tricked so that the device always read a null current. To do this, it is enough connecting CS+ directly to the output voltage leaving CS- unconnected. The reaction will keep CS+ and CS- at the same voltage, always reading a null current and also assuring the FB disconnection protection to be effective. To aovid setting the FB-disconnection protection, it is also suggested to connect CS+ to local-V_{OUT} through the same resistor divider used as external divider (See *Figure 1*).

To disable also the FB disconnection protection, CS+ can be directly connected to VSEN or SGND.

Figure 9. Droop function current reading network



7.3 Maximum duty cycle limitation

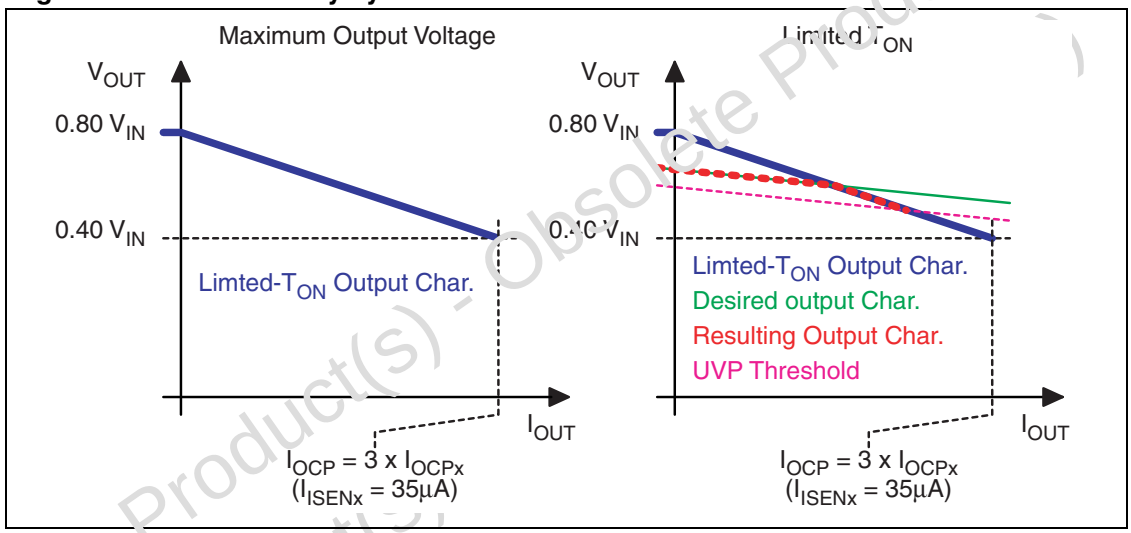
To provide proper time for current-reading in order to equalize the current carried by each phase, the device implements a duty-cycle limitation. This limitation is not fixed but it is linearly variable with the current delivered to the load as follow:

$$T_{ON(max)} = \begin{cases} 0.80 \cdot T_{SW} & I_{ISENx} = 0\mu A \\ 0.40 \cdot T_{SW} & I_{ISENx} = 35\mu A \end{cases}$$

Duty Cycle limitation is variable with the delivered current to provide fast load transient response at light load as well as assuring robust over-current protection.

Figure 10 shows the maximum output voltage that the device is able to regulate considering the T_{ON} limitation imposed by the previous relationship. If the desired output characteristic crosses the limited-T_{ON} maximum output voltage, the output resulting voltage will start to drop after the cross-point. In this case, the output voltage starts to decrease following the resulting characteristic (dotted in *Figure 10*) until UVP is detected or anyway until I_{ISENx} = 35µA.

Figure 10. Maximum duty-cycle limitation



8 Soft start

L6722 implements a soft-start to smoothly charge the output filter avoiding high in-rush currents to be required to the input power supply. The device increases the reference from zero up to the programmed value in 2048 clock periods and the output voltage increases accordingly with closed loop regulation. At the end of the digital Soft-Start, PGOOD signal is set free.

Protections are active during this phase; Under Voltage is enabled when the reference voltage reaches 0.6V while Over Voltage is always enabled with a threshold dependent on the selected Operative Mode

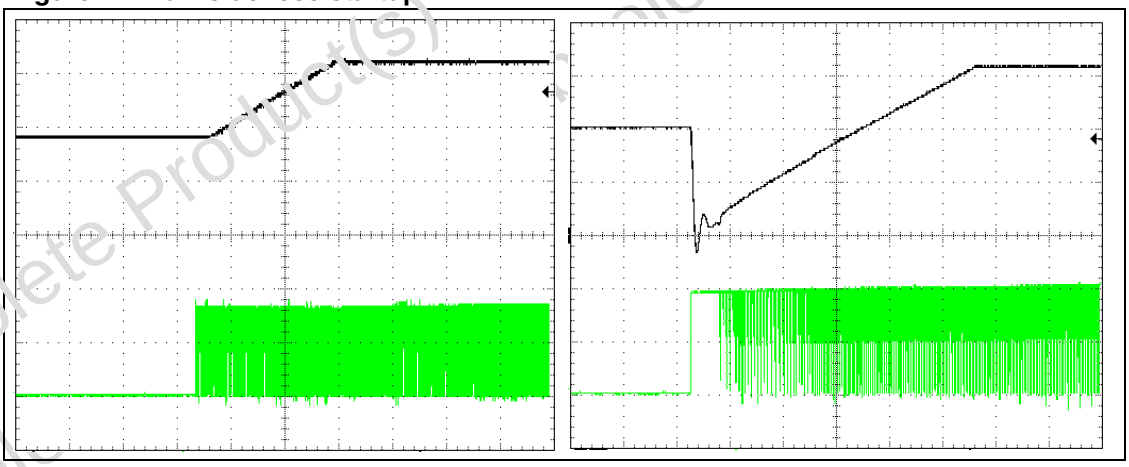
The device implements Soft-Start only when all the power supplies are above their own turn-on thresholds and the INH pin is set free.

8.1 Low-side-less startup for pre-bias output

To manage pre-biased output start-up and in order to avoid any kind of negative undershoot and dangerous return from the load, L6722 performs a special sequence in enabling LS driver to switch: during the soft-start phase, the LS driver results disabled (LS=OFF) until the HS starts to switch. This avoid the dangerous negative spike on the output voltage that can happen if starting over a pre-biased output (See *Figure 11*).

This particular feature of the device masks the LS turn-on only from the control-loop point of view: protections are still allowed to turn-on the ls mosfet in case of over-voltage if needed.

Figure 11. low-side-less startup



9 Output voltage monitor and protections

L6722 monitors through pin VSEN the regulated voltage and compares this voltage with the one present at the REF_IN pin to manage the OVP, UVP and PGOOD conditions. Protections are active also during soft-start (See *Section 8* for details).

9.1 Under voltage

If the output voltage monitored by VSEN drops more than -300mV below the programmed reference for more than one clock period, the device turns off all mosfets and latches the condition: to recover it is required to cycle Vcc or the INH pin.

UVP is active when the device is enabled, after the reference reaches 0.6V.

9.2 Over voltage

When the voltage sensed by VSEN overcomes the OVP threshold, the controller permanently switches on all the low-side mosfets and switches off all the high-side mosfets in order to protect the load. The FLT pin is driven high (5V) and power supply or INH pin cycling is required to restart operations.

OVP is active as soon as the device is enabled.

9.3 Preliminary over voltage

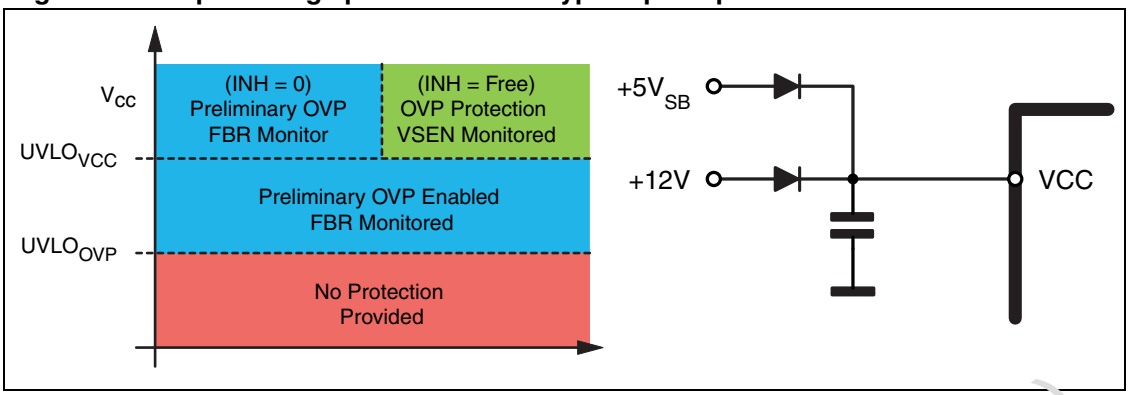
To provide a protection while VCC is below the $UVLO_{VCC}$ threshold and when the device is disabled is fundamental to avoid damage to the load in case of failed HS mosfets. In fact, since the device is supplied from the 12V bus, it is basically “blind” for any voltage below the turn-on threshold ($UVLO_{VCC}$). In order to give full protection to the load, a Preliminary-OVP protection is provided while VCC is within $UVLO_{VCC}$ and $UVLO_{OVP}$.

This protection turns-on the low side mosfets as long as the FBR pin voltage is greater than 1.25V with a 300mV hysteresis. When set, the protection drives the LS mosfet with a gate-to-source voltage depending on the voltage applied to VCC. This protection depends also on the INH pin status as detailed in *Figure 12*.

A simple way to provide protection to the output in all conditions when the device is OFF (then avoiding the unprotected red region in *Figure 12*-Left) consists in supplying the controller through the 5VSB bus as shown in *Figure 12*-Right: 5VSB is always present before +12V and, in case of HS short, the LS mosfet is driven with 5V assuring a reliable protection of the load.

Pre-OVP is active when the device is disabled and when $UVLO_{OVP} < VCC < UVLO_{VCC}$.

Figure 12. output voltage protections and typical principle connections



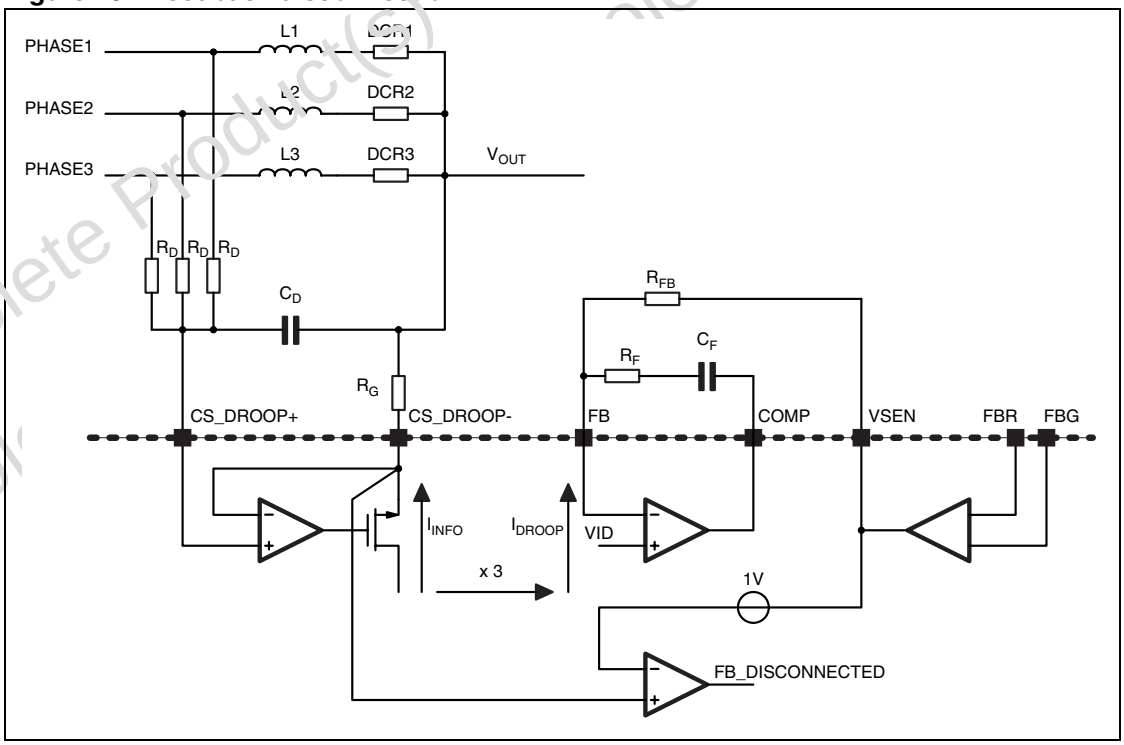
9.4 Feedback disconnection

Output voltage i monitored by the device in two different points:

- Remotely, through the remote buffer, across VSEN
- Locally across the CS- pin (negligibly offset by $R_D \cdot I_{CS}$).

By comparing the voltage present at these two different locations, L6722 is able to understand if the output voltage feedback is connected. When CS- is more than 1.375V higher than VSEN, (See *Figure 13*) the device stops switching with the low side mosfets permanently ON and drives high the FAULT pin. The condition is latched until VCC or INH cycled.

Figure 13. Feedback disconnection



9.5 PGOOD

It is an open-drain signal set free after the soft-start sequence has finished. It is pulled low when the output voltage drops below -150mV of the programmed voltage.

9.6 Over-current protection

The Over Current threshold has to be programmed, by designing the R_{ISENx} resistors, to a safe value, in order to be sure that the device doesn't enter OCP during normal operations. This value must take into consideration also the process spread and temperature variations of the sensing elements as well as the minimum value $I_{OCTH(min)}$ of the threshold as follow:

$$Rg = \frac{I_{OCPx(max)} \cdot R_{dsON(max)}}{I_{OCTH(min)}}$$

where I_{OCPx} is the current measured by the current reading circuitry when the device enters Quasi-Constant-Current.

Since the device reads the current across Low Side mosfets, it limits the bottom of the inductor current entering in constant current until setting UVP as below explained. I_{OCPx} must be calculated starting from the corresponding output current value $I_{OUT(OCP)}$ as follow since the device holds the valley current information:

$$I_{OCPx} = \frac{I_{OUT(OCP)}}{3} - \frac{\Delta I_{PP}}{2}$$

where $I_{OUT(OCP)}$ is still the output current value at which the device enters Quasi-Constant-Current, and I_{PP} is the inductor current ripple in each phase. In particular, since the device limits the valley of the inductor current, the ripple entity, when not negligible, impacts on the real OC threshold value and must be considered.

The device detects an Over Current condition for each phase when the current information I_{ISENx} overcomes the fixed threshold of I_{OCTH}. When this happens, the device keeps the relative LS mosfet on, also skipping clock cycles, until the threshold is crossed back and I_{ISENx} results being lower than the I_{OCTH} threshold (this implies that the device limits the bottom of each inductor current ripple). After exiting the OC condition, the LS mosfet is turned off and the HS is turned on with a duty cycle driven by the PWM comparator.

Keeping the LS on, skipping clock cycles, causes the on-time subsequent to the exit from the OC condition, driven by the control loop, to increase. The device enters in Quasi-Constant-Current operation: the low-side mosfets stays ON until the current read becomes lower than I_{OCPx} ($I_{INFOx} < I_{OCTH}$) skipping clock cycles. The high side mosfet can be then turned ON with a T_{ON} imposed by the control loop after the LS turn-off and the device works in the usual way until another OCP event is detected.

This means that the average current delivered can slightly increase in Quasi-Constant-Current operation since the current ripple increases. In fact, the ON time increases due to the OFF time rise because of the current has to reach the I_{OCPx} bottom. The worst-case condition is when the ON time reaches its maximum value.

When this happens, the device works in Real Constant Current and the output voltage decrease as the load increase. Crossing the UVP threshold causes the device to latch driving high the OSC pin.

It can be observed that the peak current (I_{PEAK}) is greater than I_{OCPx} but it can be determined as follow:

$$I_{PEAK} = I_{OCPx} + \frac{V_{IN} - V_{OUT(min)}}{L} \cdot T_{ON(max)} = I_{OCPx} + \frac{V_{IN} - V_{OUT(min)}}{L} \cdot 0.40 \cdot T_{SW}$$

Where V_{outMIN} is the UVP threshold, (inductor saturation must be considered). When that threshold is crossed, all mosfets are turned off, the FAULT pin is driven high and the device stops working. Cycle the power supply or the INH pin to restart operation.

The maximum average current during the Constant-Current behavior results:

$$I_{MAX,\ tot} = 3 \cdot I_{MAX} = 3 \cdot \left(I_{OCPx} + \frac{I_{PEAK} - I_{OCPx}}{2} \right)$$

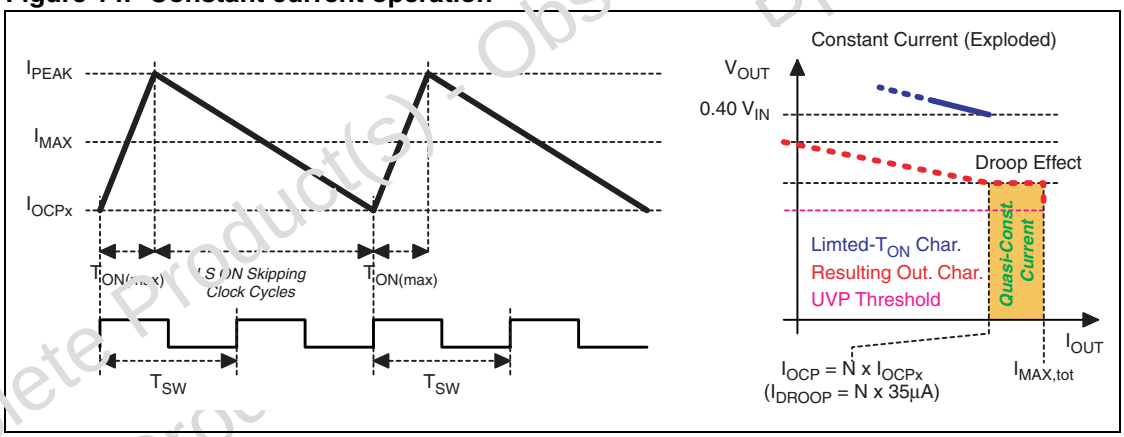
in this particular situation, the switching frequency for each phase results reduced. The ON time is the maximum allowed $T_{ON(max)}$ while the OFF time depends on the application:

$$T_{OFF} = L \cdot \frac{I_{PEAK} - I_{OCPx}}{V_{OUT}} \qquad f = \frac{1}{T_{ON(max)} + T_{OFF}}$$

The trans-conductance resistor R_{ISENx} can be designed considering that the device limits the bottom of the inductor current ripple and also considering the additional current delivered during the quasi-constant-current behavior as previously described in the worst case conditions.

$$R_{ISENx} = \frac{I_{OCPx(max)} \cdot R_{dsON(max)}}{I_{OCTH(min)}} \text{ where } I_{OCPx} = \frac{I_{OUT(OCP)}}{3} - \frac{\Delta I_{PP}}{2}$$

Figure 14. Constant current operation



10 Oscillator

The internal oscillator generates the triangular waveform for the PWM charging and discharging with a constant current an internal capacitor. The switching frequency for each channel, F_{SW}, is internally fixed at 100kHz so that the resulting switching frequency at the load side results in being tripled (300kHz).

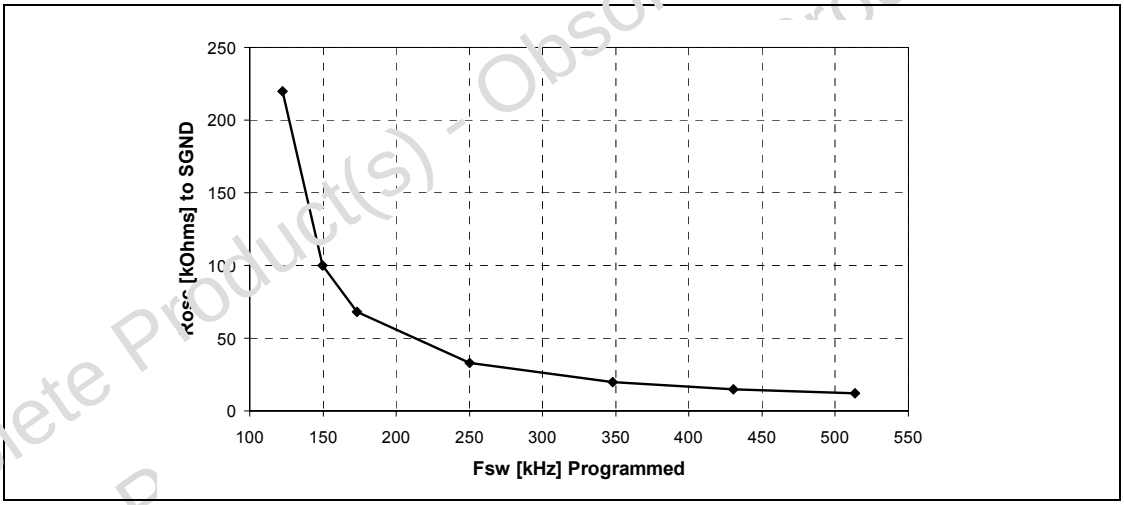
The current delivered to the oscillator is typically 25µA (corresponding to the free running frequency F_{SW}=100kHz) and it may be varied using an external resistor (R_{OSC}) connected between the OSC pin and SGND. Since the OSC pin is fixed at 1.24V, the frequency is varied proportionally to the current sunk from the pin considering the internal gain of 4KHz/µA.

In particular connecting R_{OSC} to SGND the frequency is increased according to the following relationship:

$$R_{OSC} \text{ vs. SGND } F_{SW} = 100kHz + \frac{1.240V}{R_{OSC}(k\Omega)} \cdot 4\frac{kHz}{\mu A} = 100kHz + \frac{4.96 \cdot 10^6}{R_{OSC}(k\Omega)}$$

Caution: Maximum programmable switching frequency per phase must be limited to 500kHz to avoid current reading errors causing, as a consequence, current sharing errors. Anyway, device power dissipation must be checked prior to design high switching frequency systems.

Figure 15. R_{OSC} vs. Switching frequency

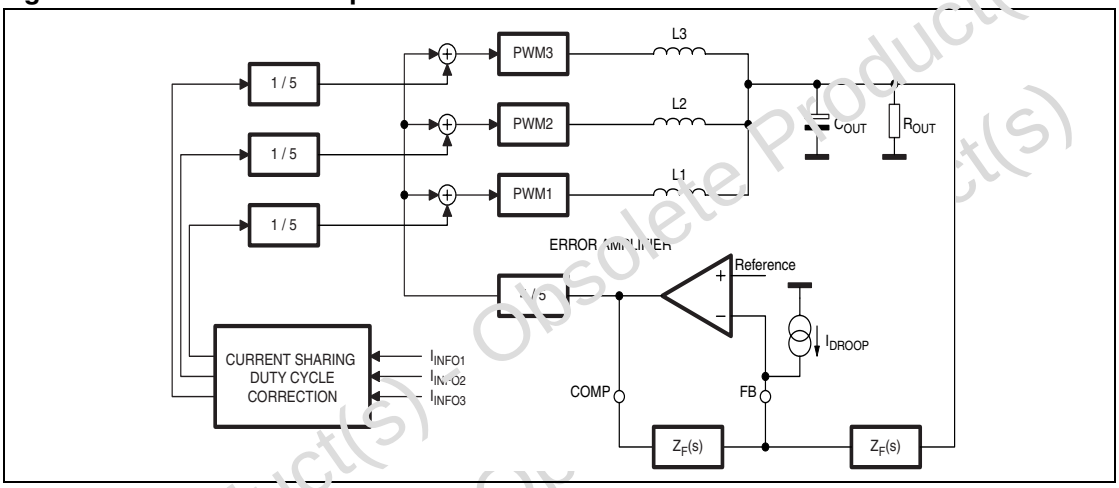


11 System control loop compensation

The control loop is composed by the Current Sharing control loop (See *Figure 16*) and the Voltage control loop. Each loop gives, with a proper gain, the correction to the PWM in order to minimize the error in its regulation: the Current Sharing control loop equalize the currents in the inductors while the Voltage control loop fixes the output voltage equal to the reference. *Figure 16* shows the block diagram of the system control loop.

The system Control Loop is reported in *Figure 17*. The current information I_{DROOP} sourced by the DROOP pin flows into R_{FB} implementing the dependence of the output voltage from the read current (when DROOP is enabled).

Figure 16. Main control loop



The system can be modeled with an equivalent single phase converter which only difference is the equivalent inductor L/3 (where each phase has an L inductor).

The Control Loop gain results (obtained opening the loop after the COMP pin):

$$G_{LOOP}(s) = -\frac{PWM \cdot Z_F(s) \cdot (R_{DROOP} + Z_P(s))}{[Z_P(s) + Z_L(s)] \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

Where:

- $R_{DROOP} = \frac{DCR}{Rg} \cdot R_{FB}$ is the equivalent output resistance determined by the droop function;
- $Z_P(s)$ is the impedance resulting by the parallel of the output capacitor (and its ESR) and the applied load R_O;
- $Z_F(s)$ is the compensation network impedance;
- $Z_L(s)$ is the parallel of the three inductor impedance;
- A(s) is the error amplifier gain;

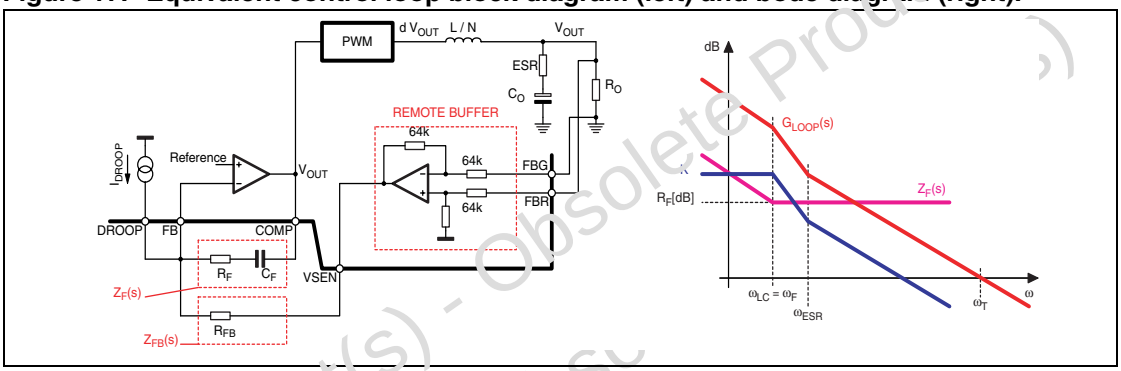
- $PWM = \frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}}$ is the PWM transfer function where ΔV_{OSC} is the oscillator ramp amplitude and has a typical value of 4V.

Removing the dependence from the Error Amplifier gain, so assuming this gain high enough, and with further simplifications, the control loop gain results:

$$)OP(s) = -\frac{4}{5} \cdot \frac{V_{IN}}{\Delta V_{OSC}} \cdot \frac{Z_F(s)}{R_{FB}} \cdot \frac{R_O + R_{DROOP}}{R_O + \frac{R_L}{3}} \cdot \frac{1 + s \cdot C_O \cdot (R_{DROOP} // R_O + ESR)}{s^2 \cdot C_O \cdot \frac{L}{3} + s \cdot \left[\frac{L}{3 \cdot R_O} + C_O \cdot ESR + C_O \cdot \frac{R_L}{3}\right]}$$

The system Control Loop gain (See *Figure 17*) is designed in order to obtain a high DC gain to minimize static error and to cross the 0dB axes with a constant -20dB/dec slope with the desired crossover frequency ω_T. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles; both the poles are fixed once the output filter is designed (LC filter resonance ω_{LC}) and the zero (ω_{ESR}) is fixed by ESR and the Droop resistance.

Figure 17. Equivalent control loop block diagram (left) and bode diagram (right).



To obtain the desired shape an R_F-C_F series network is considered for the $Z_F(s)$ implementation. A zero at $\omega_F=1/R_FC_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero ω_F in correspondence with the L-C resonance assures a simple -20dB/dec shape of the gain.

In fact considering the usual value for the output filter, the LC resonance results to be at frequency lower than the above reported zero.

Compensation network can be simply designed placing $\omega_F=\omega_{LC}$ and imposing the cross-over frequency ω_T as desired obtaining (always considering that ω_T might be not higher than 1/10th of the switching frequency F_{SW}):

$$= \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \frac{5}{4} \cdot \omega_T \cdot \frac{L}{3 \cdot (R_{DROOP} + ESR} C_F = \frac{\sqrt{C_O \cdot \frac{L}{3}}}{R_F}$$

11.1 Compensation network guidelines

The Compensation Network design assures to having system response according to the cross-over frequency selected and to the output filter considered: it is anyway possible to further fine-tune the compensation network modifying the bandwidth in order to get the best response of the system as follow:

- Increase R_F to increase the system bandwidth accordingly;
- Decrease R_F to decrease the system bandwidth accordingly;

- Increase C_F to move ω_F to low frequencies increasing as a consequence the system phase margin.

Having the fastest compensation network gives not the confidence to satisfy the requirements of the load: the inductor still limits the maximum dI/dt that the system can afford. In fact, when a load transient is applied, the best that the controller can do is to “saturate” the duty cycle to its maximum (d_{MAX}) or minimum (0) value. The output voltage dV/dt is then limited by the inductor charge / discharge time and by the output capacitance.

12 Layout guidelines

Since the device manages control functions and high-current drivers, layout is one of the most important things to consider when designing such high current applications. A good layout solution can generate a benefit in lowering power dissipation on the power paths, reducing radiation and a proper connection between signal and power ground can optimize the performance of the control loops.

Two kind of critical components and connections have to be considered when layouting a VR based on L6722: power components and connections and small signal components connections.

12.1 Power components and connections

These are the components and connections where switching and high continuous current flows from the input to the load. The first priority when placing components has to be reserved to this power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) these interconnections must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, i.e. the power transistors, must be close one to the other. The use of multi-layer printed circuit board is recommended.

Figure 18 shows the details of the power connections involved and the current loops. The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred, MLCC are suggested to be connected near the HS drain.

Use proper VIAs number when power traces have to move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, reproducing the same high-current trace on more than one PCB layer will reduce the parasitic resistance associated to that connection.

Connect output bulk capacitor as near as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace also adding extra decoupling capacitors along the way to the load when this results in being far from the bulk capacitor bank.

Gate traces must be sized according to the driver RMS current delivered to the power mosfet. The device robustness allows managing applications with the power section far from the controller without losing performances. Anyway, when possible, it is suggested to minimize the distance between controller and power section.

12.2 Small signal components and connections

These are small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply (See *Figure 18*). Locate the bypass capacitor (VCC and Bootstrap capacitor) close to the device and refer sensible components such as frequency and offset setup resistors to SGND. Star grounding is suggested: connect SGND to PGND plane in a single point to avoid that drops due to the high current delivered causes errors in the device behavior.

Remote Sense Connection must be routed as parallel nets from the FBG/FBR pins to the load in order to avoid the pick-up of any common mode noise. Connecting these pins in points far from the load will cause a non-optimum load regulation, increasing output tolerance.

Locate current reading components close to the device. It's also important to minimize any offset in the measurement and, to get a better precision, to connect the traces as close as possible to the sensing elements.

Caution: **Boot capacitor extra charge**. Systems that do not use Schottky diodes in parallel to the low-side mosfet might show big negative spikes on the phase pin. This spike can be limited as well as the positive spike but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the abs. max. ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by:

- adding a small resistor in series to the boot diode (one resistor can be enough for all the three diodes if placed upstream the boot diode anode, see *Figure 18*)
- using non-capacitive boot diodes (such as standard diodes).

Figure 18. Power connections and related connections layout (same for all phases).

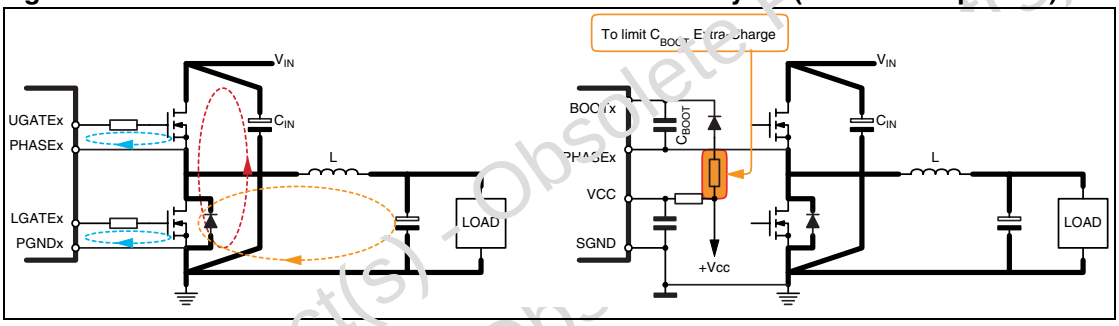
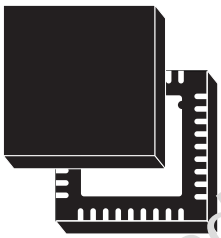


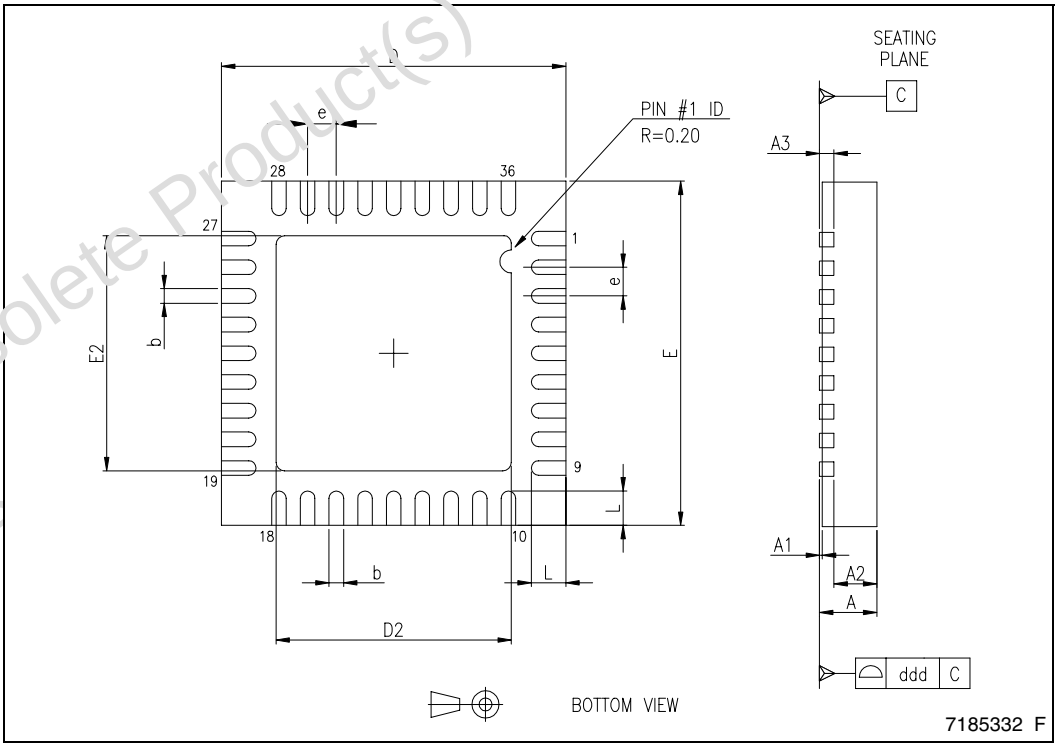
Figure 19. VFQFPN36 Mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.800	0.900	1.000	0.031	0.035	0.039
A1		0.020	0.050		0.0008	0.0019
A2		0.650	1.000		0.025	0.039
A3		0.250			0.01	
b	0.180	0.230	0.300	0.007	0.009	0.012
D	5.875	6.000	6.125	0.231	0.236	0.241
D2	1.750	3.700	4.250	0.069	0.146	0.167
E	5.875	6.000	6.125	0.231	0.236	0.241
E2	1.750	3.700	4.250	0.069	0.146	0.167
e	0.450	0.500	0.550	0.018	0.020	0.022
L	0.350	0.550	0.750	0.014	0.022	0.029
ddd			0.080			0.003

OUTLINE AND MECHANICAL DATA



VFQFPN-36 (6x6x1.0mm)
Very Fine Quad Flat Package No lead



13 Revision history

Table 5. Revision history

Date	Revision	Changes
14-Apr-2006	1	Initial release.

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