Single-Chip 5V Wireless Power Transmitter IC for TX-A5 and A11

Product Datasheet

IDTP9035A

Features

- **5W Solution for Wireless Power Consortium (WPC)-compliant power transmitter design A5/A11**
- **Conforms to WPC specification version 1.1 specifications**
- **5V Operating Input Voltage**
- **Uses External Full-Bridge Inverter.**
- **Closed-Loop Power Transfer Control between Base Station and Mobile Device**
- **Demodulates and Decodes WPC-Compliant Message Packets**
- **Integrated RESET Function**
- **Proprietary Back-Channel Communication**
- **I²C Interface**
- **Open-Drain LED Indicator Outputs**
- **Over-Temperature/Current Protection**
- **Security and Encryption up to 64 bits**
- **Foreign Object Detection (FOD)**

Applications

- **WPC-Compliant Wireless Charging Base Stations**
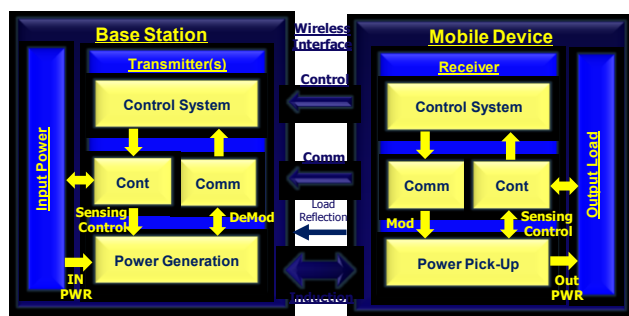
Package: 6x6-48 TQFN (See page 28)
Ordering Information (See page 29)

Description

The IDTP9035A is a highly-integrated WPC-compliant wireless power transmitter IC for power transmitter design A5 and A11. The device operates with a 5V (±5%) adaptor, and utilizes an external full-bridge inverter to provide a highly-efficient solution for A5/A11 transmitter applications. It controls the transferred power by modulating the switching frequency of the full-bridge inverter from 110kHz to 205kHz at a fixed 50% duty cycle specified by the WPC specification for an A5/A11 transmitter. It contains logic circuits required to demodulate and decode WPC-compliant message packets sent by the mobile device to adjust the transferred power.
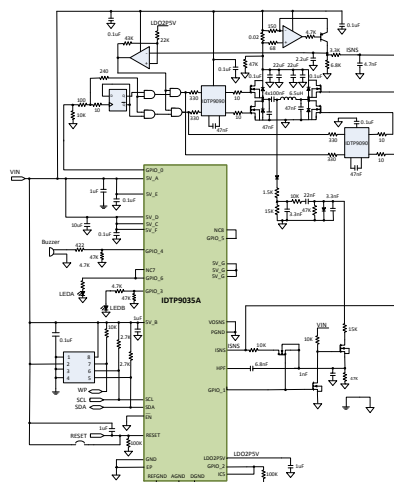
The IDTP9035A is an intelligent device that periodically pings the area surrounding the base station to detect a mobile device for charging while minimizing idle power. Once the mobile device is detected and authenticated, the IDTP9035A continuously monitors all communications from the mobile device, and adjusts the transmitted power accordingly by varying the switching frequency of the half-bridge inverter.
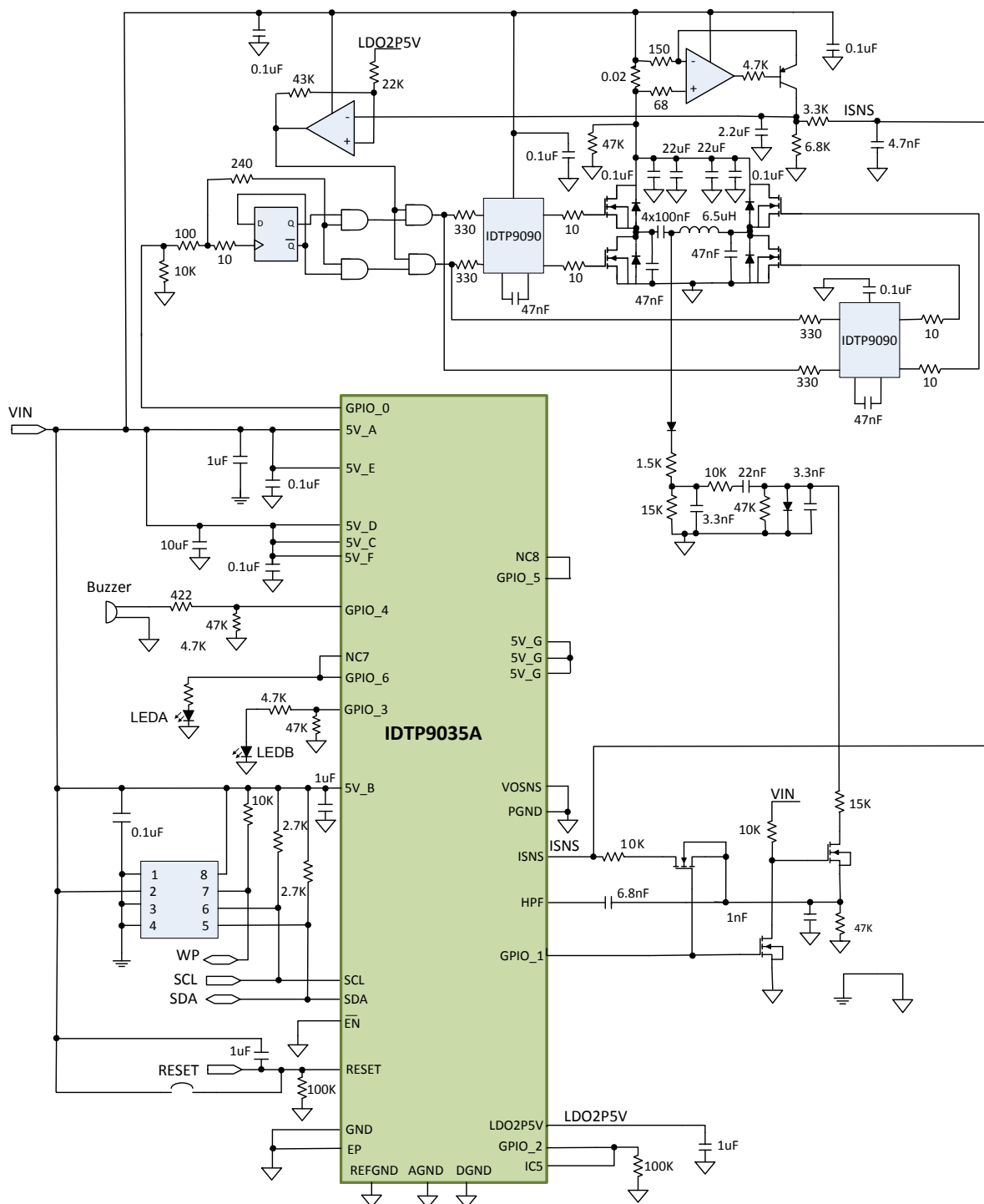
The IDTP9035A features a proprietary back-channel communication mode which enables the device to communicate with IDT's wireless power receiver solutions (e.g. IDTP9020). This feature enables additional layers of capabilities relative to standard WPC requirements.

This device also features optional security and encryptions to securely authenticate the receiver before transferring power. This feature is available when an IDTP9020 is used for the receiver.

The device includes over-temperature/current protection and a Foreign Object Detection (FOD) method to protect the base station and mobile device from overheating in the presence of a metallic foreign object. It manages fault conditions associated with power transfer and controls status LEDs to indicate operating modes.

Typical Application Circuit

TYPICAL APPLICATION CIRCUIT

Figure 1. IDTP9035A Simplified Application Schematic

Note 1: NPO/C0G-type ceramic capacitor.
Note 2: For PCB layout, use single-point reference ("star" ground), refer to design schematic in Figure 9).
Note 3: The 220uF bulk capacitors are necessary for proper operation of the transmitter.

ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the IDTP9035A at absolute maximum ratings is not implied. Application of the absolute maximum rating conditions affects long-term reliability.

Table 1. Absolute Maximum Ratings Summary. All voltages are referred to ground, unless otherwise noted.

PINS	RATING	UNITS
5V_A, 5V_B, 5V_C, 5V_D, 5V_E, 5V_F, 5V_G. **THESE PINS MUST BE CONNECTED TOGETHER AT ALL TIMES.**	-0.3 to 6.0	V
$\overline{EN}$, IC_1, IC_2, SW5, GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_6, HPF, ISNS, RESET, SCL, SDA, VOSNS	-0.3 to VIN+0.3	V
LDO2P5V, XIN, XOUT	-0.3 to 2.75	V
AGND, DGND, PGND, REFGND	-0.3 to +0.3	V

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	RATING	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient (NTG48 - TQFN)	30.8	°C/W
θ_{JC}	Thermal Resistance Junction to Case (NTG48 - TQFN)	14.6	°C/W
θ_{JB}	Thermal Resistance Junction to Board (NTG48 - TQFN)	0.75	°C/W
T_J	Operating Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Note 4: For the NTG48 package, connecting the 4.1 mm X 4.1 mm EP to internal/external ground planes with a 5x5 matrix of PCB plated-through-hole (PTH) vias, from top to bottom sides of the PCB, is recommended for improving the overall thermal performance.

Table 3. ESD Information

TEST MODEL	PINS	RATINGS	UNITS
HBM	All pins.	±2000	V
CDM	All pins.	±500	V

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, 5V_A = 5V_B = 5V_C = 5V_D = 5V_E = 5V_F = 5V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics

SYMBOL		DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Inverter Controller							
V_{IN}		Input Supply Operating Voltage Range[1]		4.75		5.25	V
I_{IN}[2]	I_{IN_A}	Standby Input Current	After power-up sequence complete, average including pinging.		20		mA
F_{SW_LOW}		Switching Frequency at SW	WPC Operating Range, in compliance with WPC requirements	110			kHz
F_{SW_HIGH}						205	kHz
Inverter OCP							
I_{IN_OCP}		Over-Current Protection Trip Point	V_{IN} = 5V, cycle-by-cycle protection.	4	5.5	7	A
Low Drop Out Regulator (For Biasing Internal Circuitry Only)[3]							
LDO2P5V[3]							
$V_{LDO2P5V\_IN}$		Input Voltage Range	Supplied from BUCK5VT		5		V
$V_{LDO2P5V}$		Output Voltage	I_{Load} = 2mA		2.5		V
I_{OUT}		External Load				5	mA
Thermal Shutdown							
T_{SD}		Thermal Shutdown	Temperature Rising Threshold		140		°C
			Temperature Falling Threshold		110		
$\overline{EN}$							
V_{IH}					900		mV
V_{IL}					550		mV
$I_{\overline{EN}}$		$\overline{EN}$ input current	$V_{\overline{EN}}$ = 5V		7.5		µA
General Purpose Inputs / Outputs (GPIO)							
V_{IH}		Input Threshold High		3.5			V
V_{IL}		Input Threshold Low				1.5	V
I_{LKG}		Input Leakage		-1		+1	µA
V_{OH}		Output Logic High	I_{OH}=-8mA	4			V
V_{OL}		Output Logic Low	I_{OL}=8mA			0.5	V

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, 5V_A = 5V_B = 5V_C = 5V_D = 5V_E = 5V_F = 5V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
RESET						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
SCL, SDA (I²C Interface)						
f_{SCL}	Clock Frequency	EEPROM loading, Step 1, IDTP9035A as Master		100		kHz
f_{SCL}	Clock Frequency	EEPROM loading, Step 2, IDTP9035A as Master		300		kHz
f_{SCL}	Clock Frequency	IDTP9035A as Slave	0		400	kHz
$t_{HD;STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD;DAT}$	Data Hold Time	I²C-bus devices	10			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition		100			ns
T_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line				100	pF
C_{BIN}	SCL, SDA Input Capacitance			5		pF
V_{IL}	Input Threshold Low	When powered by device 5V			1.5	V
V_{IH}	Input Threshold High		3.5			V
I_{LKG}	Leakage Current		-1.0		1.0	µA
V_{OL}	Output Logic Low (SDA)	I_{PD}= 2mA (Note 1)			0.5	V

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, 5V_A = 5V_B = 5V_C = 5V_D = 5V_E = 5V_F = 5V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Analog-to-Digital Converter						
N	ADC Conversion Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			62.5		KSPS
Channel	Number of Channels at ADC MUX input			8		
ADC_{CLK}	ADC Clock Frequency			1		MHz
V_{IN_FS}	Full-Scale Input Voltage			2.5		V
Microcontroller						
F_{CLOCK}	Clock Frequency			40		MHz
V_{MCU}	MCU Supply Voltage from internal 2.5V LDO			2.5		V

Note 1 5V_A = 5V_B = 5V_C = 5V_D = 5V_E = 5V_F = 5V_G. These pins must be connected together at all times.

Note 2: This current is the sum of the input currents for 5V_A = 5V_B = 5V_C = 5V_D = 5V_E = 5V_F = 5V_G.

Note 3: LDO2P5V is intended only as an internal device supply and must not be loaded.

BLOCK DIAGRAM
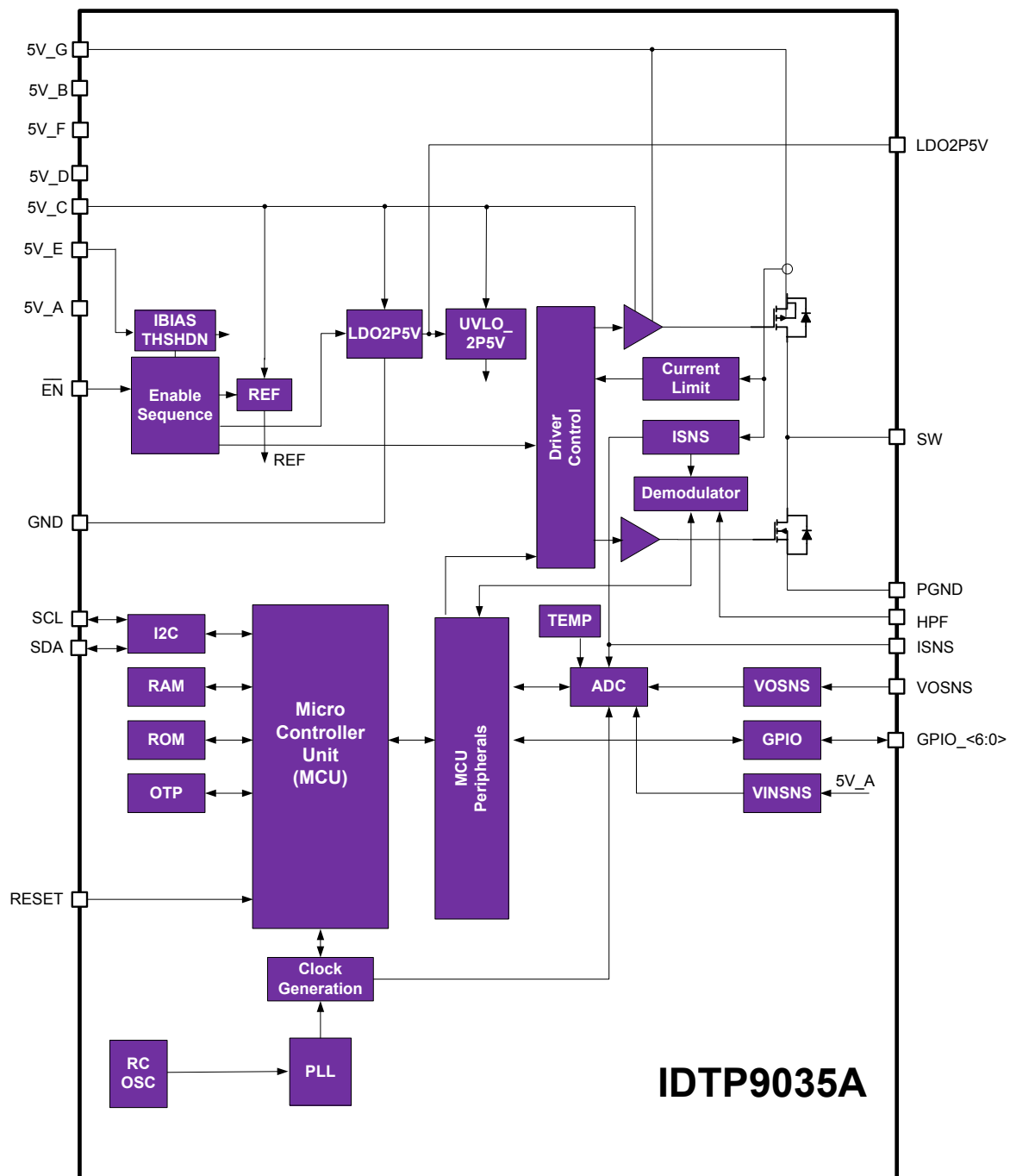
Figure 2. IDTP9035A Internal Functional Block Diagram
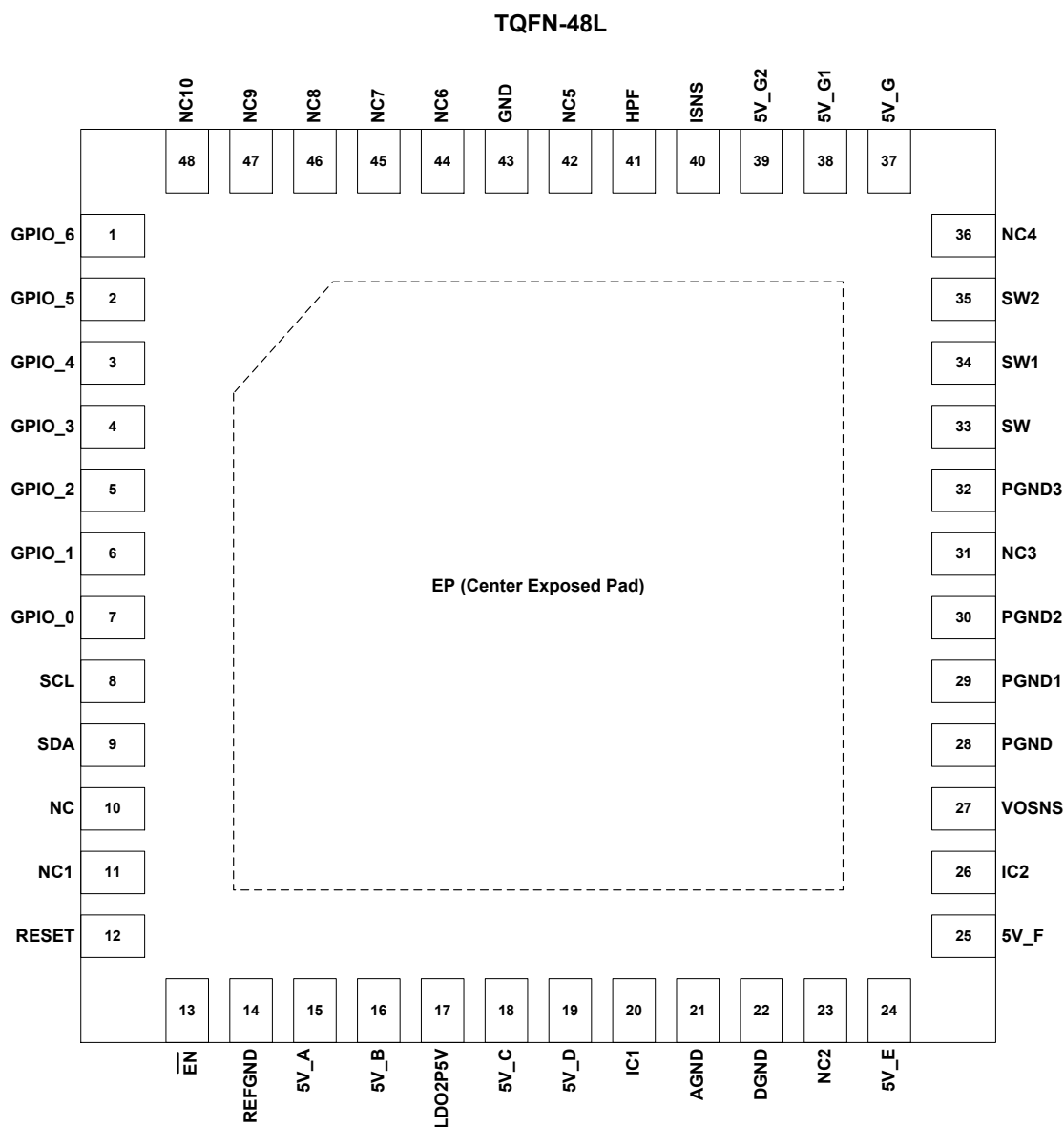
PIN CONFIGURATION

TQFN-48L

Figure 3. IDTP9035A Pin Configuration (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm, 0.4mm pitch)

PIN DESCRIPTION

Table 5. IDTP9035A NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
1	GPIO_6	I/O	General purpose input/output 6, configured as an output. Must be connected to NC7.
2	GPIO_5	I/O	General purpose input/output 5, configured as an output. Must be connected to NC8.
3	GPIO_4	I/O	General purpose input/output 4, configured as an output.
4	GPIO_3	I/O	General purpose input/output 3, configured as an output.
5	GPIO_2	I/O	General purpose input/output 2, configured as an input. Must be connected to NC9.
6	GPIO_1	I/O	General purpose input/output 1, configured as an input.
7	GPIO_0	I/O	General purpose input/output 0, configured as an output.
8	SCL	I/O	I²C clock
9	SDA	I/O	I²C data
10	NC	NC	Internally connected. Must be connected to GND.
11	NC1	NC	Internally connected. Must be left unconnected.
12	RESET	I	Active-high chip reset pin. A 1µF ceramic capacitor must be connected between this pin and LDO5V, and a 100kΩ resistor to GND.
13	$\overline{EN}$	I	Active-low enable pin. Device is suspended and placed in low current (sleep) mode when pulled high. Tie to GND for stand-alone operation.
14	REFGND	-	Signal ground connection. Must be connected to AGND.
15	5V_A[1]	I	A 0.1µF ceramic capacitor must be connected between this pin and GND. This pin must be connected to pins 16, 18, 19, 24, 25, 37, 38, and 39.
16	5V_B[1]	I	A 1µF ceramic capacitor must be connected between this pin and GND. This pin must be connected to pins 15, 18, 19, 24, 25, 37, 38, and 39.
17	LDO2P5V[2]	O	2.5V LDO output. A 1µF ceramic capacitor must be connected between this pin and GND.
18	5V_C[1]	I	2.5V LDO input. A 10µF and a 0.1µF ceramic capacitor must be connected between this pin and GND. This pin must be connected to pins 15, 16, 19, 24, 25, 37, 38, and 39.
19	5V_D[1]	I	Power and digital supply input to internal circuitry. This pin must be connected to pins 15, 16, 18, 24, 25, 37, 38, and 39.

Table 5. IDTP9035A NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
20	IC1	NC	Internal connection. Must be left unconnected.
21	AGND	-	Analog ground connection. Connect to signal ground. Must be connected to REFGND.
22	DGND	-	Digital ground connection. Must be connected to GND.
23	NC2	NC	Not internally connected.
24	5V_E[1]	I	Power supply input. Connect 0.1µF and 1µF ceramic capacitors between this pin and PGND. This pin must be connected to pins 15, 16, 18, 19, 25, 37, 38, and 39.
25	5V_F[1]	I	This pin must be connected to pins 15, 16, 18, 19, 24, 37, 38, and 39.
26	IC2	NC	Internal connection. Must be left unconnected.
27	VOSNS	I	Output voltage sense.
28	PGND	-	Power ground.
29	PGND1	-	Power ground.
30	PGND2	-	Power ground.
31	NC3	NC	Not internally connected.
32	PGND3	-	Power ground.
33	SW	O	Internal inverter switch node. Not used. Pins 33, 34, and 35 must be connected together
34	SW1	O	
35	SW2	O	
36	NC4	NC	Not internally connected.
37	5V_G[1]	I	Internal inverter power supply input. Not used.
38	5V_G1[1]	I	
39	5V_G2[1]	I	
40	ISNS	O	ISNS output signal

Table 5. IDTP9035A NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
41	HPF	I	High pass filter input
42	NC5	NC	Internal connection, must be connected to GND.
43	GND	-	Ground
44	NC6	NC	Internal connection, must be connected to GND.
45	NC7	NC	Internal connection, must be connected to GPIO6.
46	NC8	NC	Internal connection, must be connected to GPIO5.
47	NC9	NC	Internal connection, must be connected to GPIO2.
48	NC10	NC	Internal connection, do not connect.
EP	Center Exposed Pad	Thermal	EP is on the bottom of the package and must be electrically tied to GND. For thermal performance, solder to a large copper pad embedded with a pattern of plated through-hole vias. The die is not electrically bonded to the EP, and the EP must not be used as current-carrying electrical connection.

Note 1: 5V_A, 5V_B, 5V_C,5V_D, 5V_E, 5V_F. These pins must be connected together at all times.

Note 2: LDO2P5V is intended only as an internal device supply and must not be loaded.

TYPICAL PERFORMANCE CHARACTERISTICS

$\overline{EN}$ = 0, 5V_A = 5V_B = 5V_C = 5V_D = 5V_E = 5V_F = 5V, TA = 25°C. Unless otherwise noted.
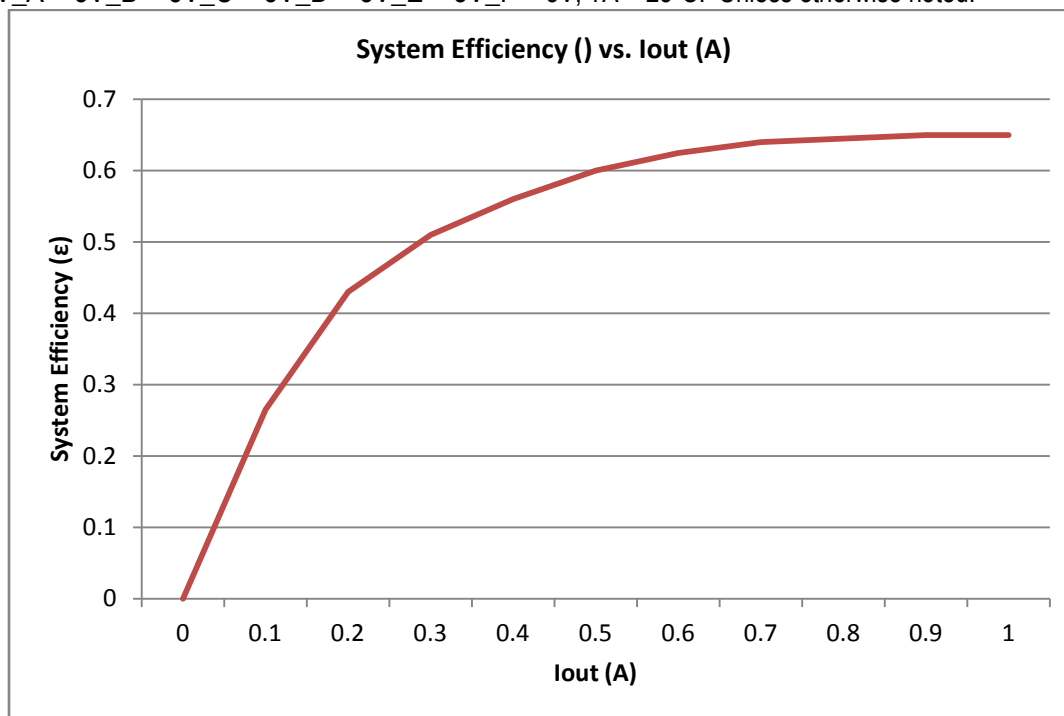
Figure 4. Efficiency vs. RX Output Power with IDTP9020 Receiver
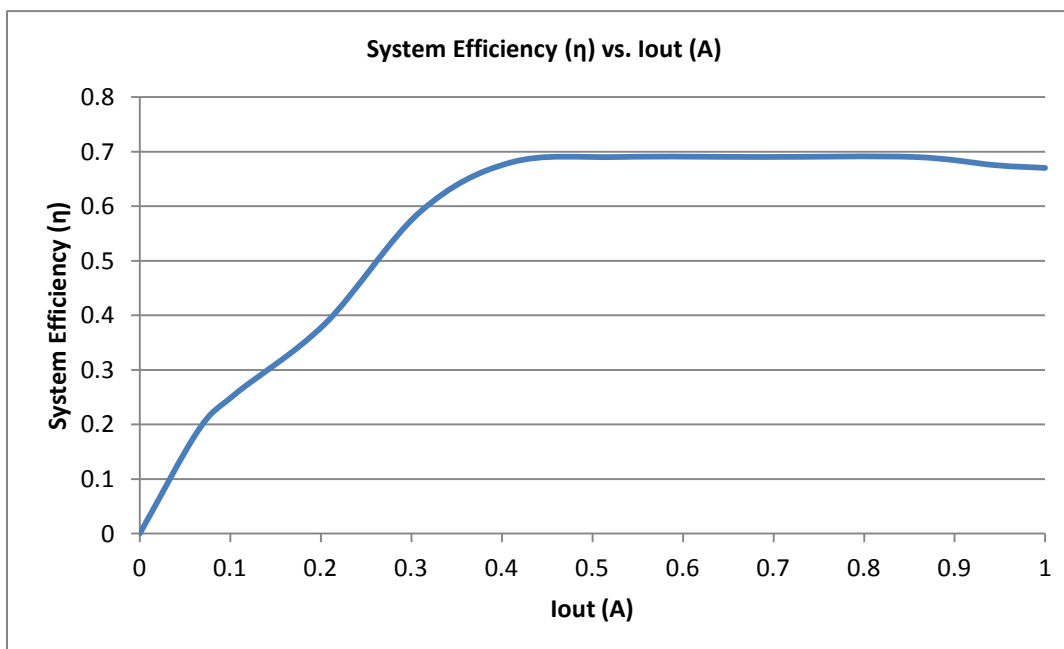
Figure 5. Spacing between TX and RX coils is 2 mm
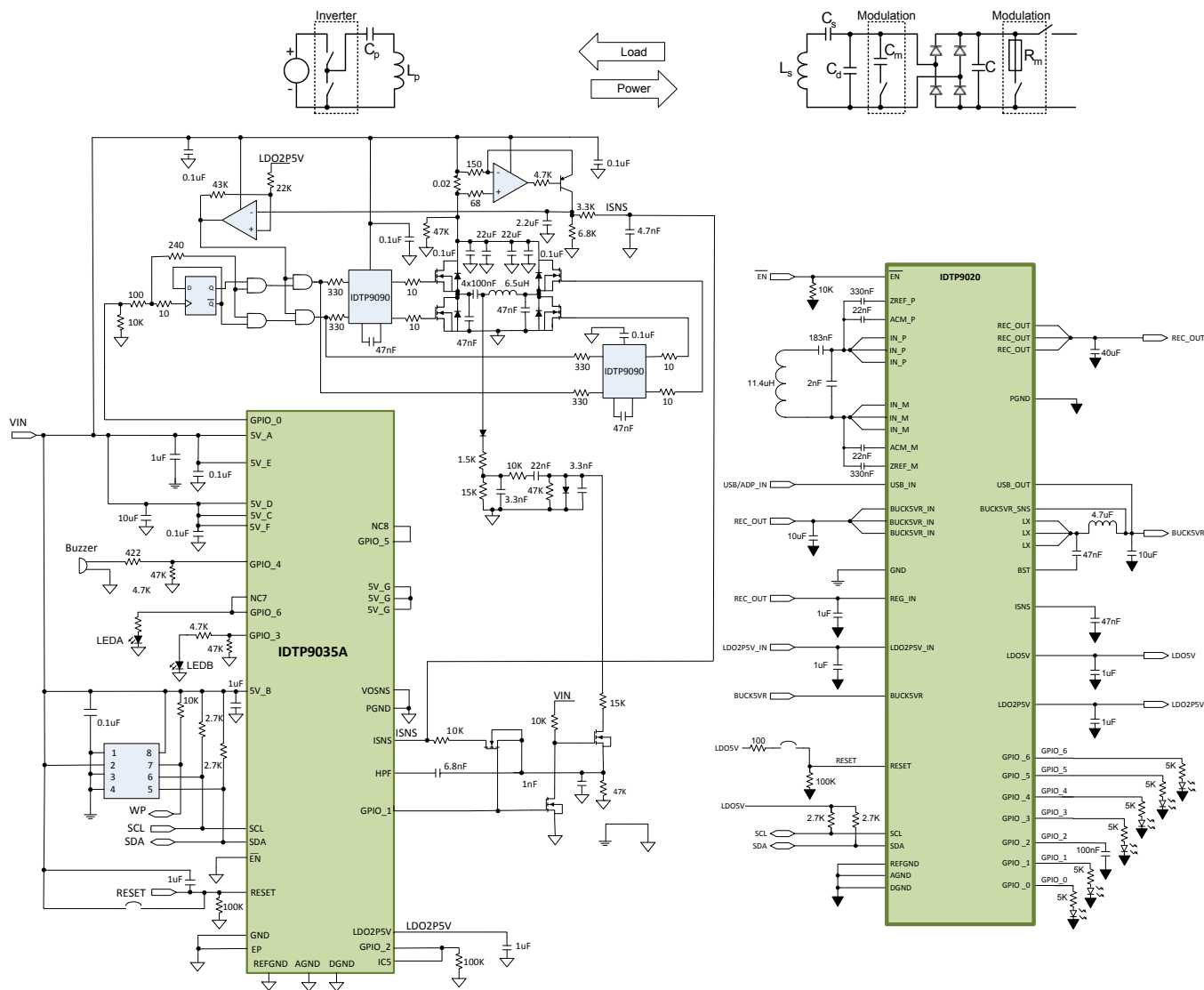
SYSTEMS APPLICATIONS DIAGRAM

Figure 6. IDTP9035A/IDTP9020 Simplified Systems Application Diagram

THEORY OF OPERATION

The IDTP9035A is a highly-integrated WPC[1] (Wireless Power Consortium)-compliant wireless power charging IC solution for transmitter base stations designed to drive a WPC-compliant Type-A5/A11 transmitter coil. It can deliver more than 5W of power to the receiver when used with the IDTP9020 or 5W in WPC "Qi" mode using near-field magnetic induction as a means to transfer energy.

OVERVIEW

Figure 2 shows the block diagram of the IDTP9035A. When 5V is applied at the 5V_A-F pins with $\overline{\text{EN}}$ at a logic LOW, the Enable Sequence circuitry activates the voltage reference, the 2.5V LDO, and the Micro-Controller Unit (MCU).

The voltage at the output of the LDO is monitored to ensure that it remains in regulation, and the adaptor voltage, coil current, and internal temperature are monitored for proper operation.

The Driver Control block converts a PWM signal (generated by the digital block and MCU) to the gate drive signals required by the external full-bridge inverter to drive the field-generating coil.

Communication packets from the receiver in the mobile device are recovered by the Demodulator and converted to digital signals that can be read by the MCU.

Several internal voltages are converted to their digital representations by the ADC and supplied to the MCU. Three GPIO ports are available to the system designer for driving LEDs and a buzzer. The clock for the MCU and other circuitry is generated an internal RC oscillator. I[2]C SDA and SCL pins permit communication with an external device or host.

OVER-CURRENT/TEMPERATURE PROTECTION

The current in the off-chip inverter is monitored by external circuitry. If the instantaneous coil current exceeds the OCP level, the on-time of the switching cycle is terminated early. The internal temperature is also monitored, and the part is temporarily deactivated if the temperature exceeds 140°C and reactivated when the temperature falls below 110°C.

DRIVER CONTROL BLOCK and INVERTER

The Driver Control block contains some of the logic for the off-chip power FETs. The external FETs are configured as a full-bridge power inverter, effectively doubling the peak-to-peak voltage applied to the coil. The frequency of the full-bridge output waveform is set by the MCU. (For details, please refer to the simplified application diagram (Figure 1) and the reference design schematic (Figure 9)).

DEMODULATOR

Power is transferred from the transmitter to the receiver through the coupling of their respective coils: a loosely-coupled transformer. The amount of power transferred is determined by the transmitter's switching frequency (110kHz-205kHz, by WPC[1]), and is controlled by the receiver through instructions it sends back through the same coils to the transmitter to change its frequency, end power transfer, or do something else. The instructions take the form of data packets, which are coupled through a series of filters connected to the IDTP9035A's Demodulator through the HPF pin. Recovering the data packets is the function of the Demodulator. Decoding and executing the packets is one of the functions of the MCU.

MICRO-CONTROLLER UNIT (MCU)

The IDTP9035A's MCU processes the algorithm, commands, and data that control the power transferred to the reciever. The MCU is provided with RAM and ROM, and parametric trim and operational modes are set at the factory through the One-Time Programming (OTP) block, read by the MCU at power-up Communication with external memory is perforned through I[2]C via the SCL and SDA pins.

.APPLICATIONS INFORMATION

The recommended applications schematic diagram is shown in Figure 9. The IDTP9035A operates with a $5V_{DC}$ (±0.25V) input. The switching frequency varies from 110kHz to 205kHz. At the 205kHz limit the duty cycle is also changed to adjust the power transfer level. The power transfer is controlled via changes in the switching frequency and duty cycle. The base or TX-side has a series resonance circuit made of a WPC Type-A5 or A11 coil (~6.5μH) and a series resonant capacitor (~400nF) driven by a full-bridge inverter, as shown in Figure 7.
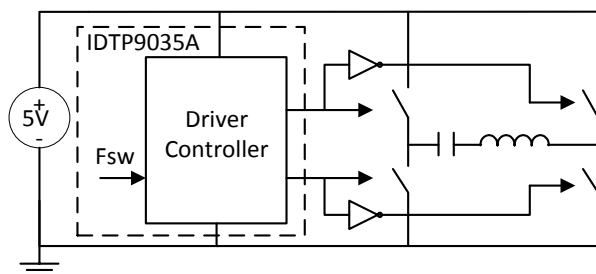
Figure 7. Full-Bridge inverter TX Coil Driver.

EXTERNAL CHIP RESET and $\overline{EN}$

The IDTP9035A can be externally reset by pulling the RESET pin to a logic high (above the V_{IH} level).

The RESET pin is a dedicated high-impedance active-high digital input, and the effect is similar to the power-up reset function. Because of the internal low voltage monitoring scheme, the use of the external RESET pin is not mandatory. If desired, a manual external reset scheme can be added by connecting 5V to the RESET pin through a simple switch. When RESET is HIGH, the microcontroller's registers are set to the default configuration. When the RESET pin is released to a LOW, the microcontroller starts executing the code from the external EEPROM.

If the particular application requires the IDTP9035A to be disabled, this can be accomplished with the $\overline{EN}$ pin. When the $\overline{EN}$ pin is pulled high, the device is suspended and placed in low current (sleep) mode. If pulled low, the device is active.

The current into $\overline{EN}$ is approximately equal to:

$$I\left(\mathrm{EN}\right) = \frac{V\left(\mathrm{EN}-2V\right)}{300k},$$

or close to zero if V($\overline{EN}$) is less than 2V.

SYSTEM FEEDBACK CONTROL (WPC)

The IDTP9035A contains logic to demodulate and decode error packets sent by the mobile device (Rx-side), and adjusts power transfer accordingly. The IDTP9035A varies the switching frequency of the full-bridge inverter between 110kHz to 205 kHz to adjust power transfer. The mobile device controls the amount of power transferred via a communication link that exists from the mobile device to the base station. The mobile device (IDTP9020-based or another WPC-compliant receiver) communicates with the IDTP9035A via Communication Packets. Each packet has the following format:

Table 6 – Data Packet Format.

Preamble	Header	Message	Checksum

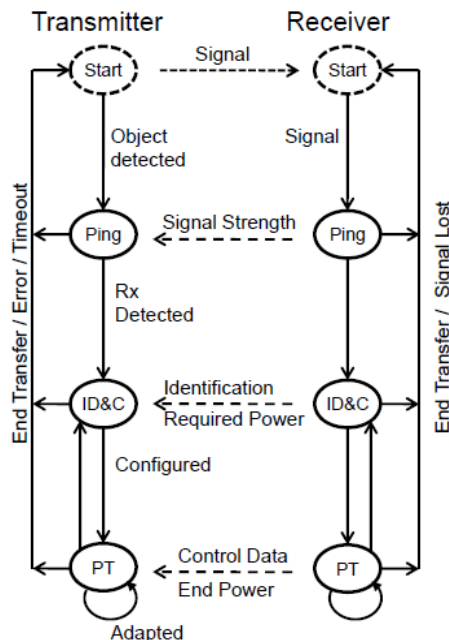The overall system behavior between the transmitter and receiver follows the state machine diagram below:

Figure 8. System state machine diagram

The IDTP9035A performs four phases: Selection, Ping, Identification & Configuration, and Power Transfer.

START (SELECTION) PHASE

In this phase, the IDTP9035A operates in a low power mode to determine if a potential receiver has been placed on the coil surface prior to the PING state. Twice a second, the IDTP9035A applies a brief AC signal to its coil and listens for a response.

PING PHASE

In this phase, the IDTP9035A applies a power signal at 175 kHz with a fixed 50% duty cycle and attempts to establish a communication link with a mobile device.

Required packet(s) in PING:

1. Signal strength packet (0x01)

The mobile device must send a Signal Strength Packet within a time period specified by the WPC, otherwise the power signal is terminated and the process repeats.

The mobile device calculates the Signal Strength Packet value, which is an unsigned integer value between 0-255, based on this formula:

$$Signal\ Strength\ Value = \left(\frac{U}{U_{max}}\right).256$$

where U is a monitored variable (i.e. rectified voltage/current/power) and U_{max} is a maximum value of that monitored variable expected during the digital ping phase at 175 kHz.

If the IDTP9035A does not detect the start bit of the header byte of the Signal Strength Packet during the Ping Phase, it removes the power signal after a delay. If a signal strength packet is received, the IDTP9035A goes to the Identification and Configuration Phase. If the IDTP9035A does not move to the Identification and Configuration Phase after receiving the signal strength packet, or if a packet other than a signal strength packet is received, then power is terminated.

IDENTIFICATION AND CONFIGURATION (ID & Config)

In this phase, the IDTP9035A tries to identify the mobile device and collects configuration information.

Required packet(s) in ID & Config:

1. Identification packet (0x71)
2. Extended Identification packet (0x81)*
3. Configuration packet (0x51)

* If Ext bit of 0x71 packet is set to 1.

Also, the IDTP9035A must correctly receive the following sequence of packets without changing the operating point (175 kHz @ 50% duty cycle):

1. Identification Packet (0x71)

2. Extented Identification (0x81)
   a. Up to 7 optional Configuration Packets from the following set:
   b. Power Control Hold-Off Packet (0x06)
   c. Proprietary Packet (0x18 – 0xF2)
   d. Reserved Packet
3. Configuration Packet (0x51)

If the IDTP9035A does not detect the start bit of the header byte of the next packet in the sequence within a WPC-specified time after receiving the stop bit of the checksum byte of the preceding Signal Strength Packet, then the Power Signal is removed after a delay. If a correct control packet in the above sequence is received late, or if control packets that are not in the sequence are received, the IDTP9035A removes the Power Signal after a delay.

POWER TRANSFER PHASE

In this phase, the IDTP9035A adapts the power transfer to the receiver based on control data it receives in control error packets.

Required packet(s) in Power Transfer:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)

For this purpose, the IDTP9035A may receive zero or more of the following Packets:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)
3. Charge Status Packet (0x05)
4. End Power Transfer Packet (0x02)
5. Any Proprietary Packet
6. Any Reserved Packets

If the IDTP9035A does not correctly receive the first Control Error Packet in time, it removes the Power Signal after a delay. Because Control Error Packets come at a regular interval, the IDTP9035A expects a new Control Error Packet after receiving the stop bit of the checksum byte of the preceding Control Error Packet. If that does not happen, then the IDTP9035A removes the Power Signal. Similary, the IDTP9035A must receive a Rectified Power Packet within a WPC-specified time after receiving the stop bit of the checksum byte of the Configuration Packet (which was received earlier in the *identification and*

configuration phase). Otherwise, it removes the Power Signal.

Upon receiving a Control Error value, the IDTP9035A makes adjustments to its operating point after a delay to enable the Primary Coil current to stabilize again after communication.

If the IDTP9035A correctly receives a Packet that does not comply with the sequence, then it removes the Power Signal.

FOREIGN OBJECT DETECTION (FOD)

In addition to over-temperature protection, the IDTP9035A employs a proprietary FOD technique which detects foreign objects placed on the base station. The FOD algorithm is multi-layered and may issue warnings and/or change device operation depending on the severity of the warning.

FOD is an optional feature that is not included in the standard firmware. Please contact IDT to incorporate this feature into a specific product, indicating volume and business case.
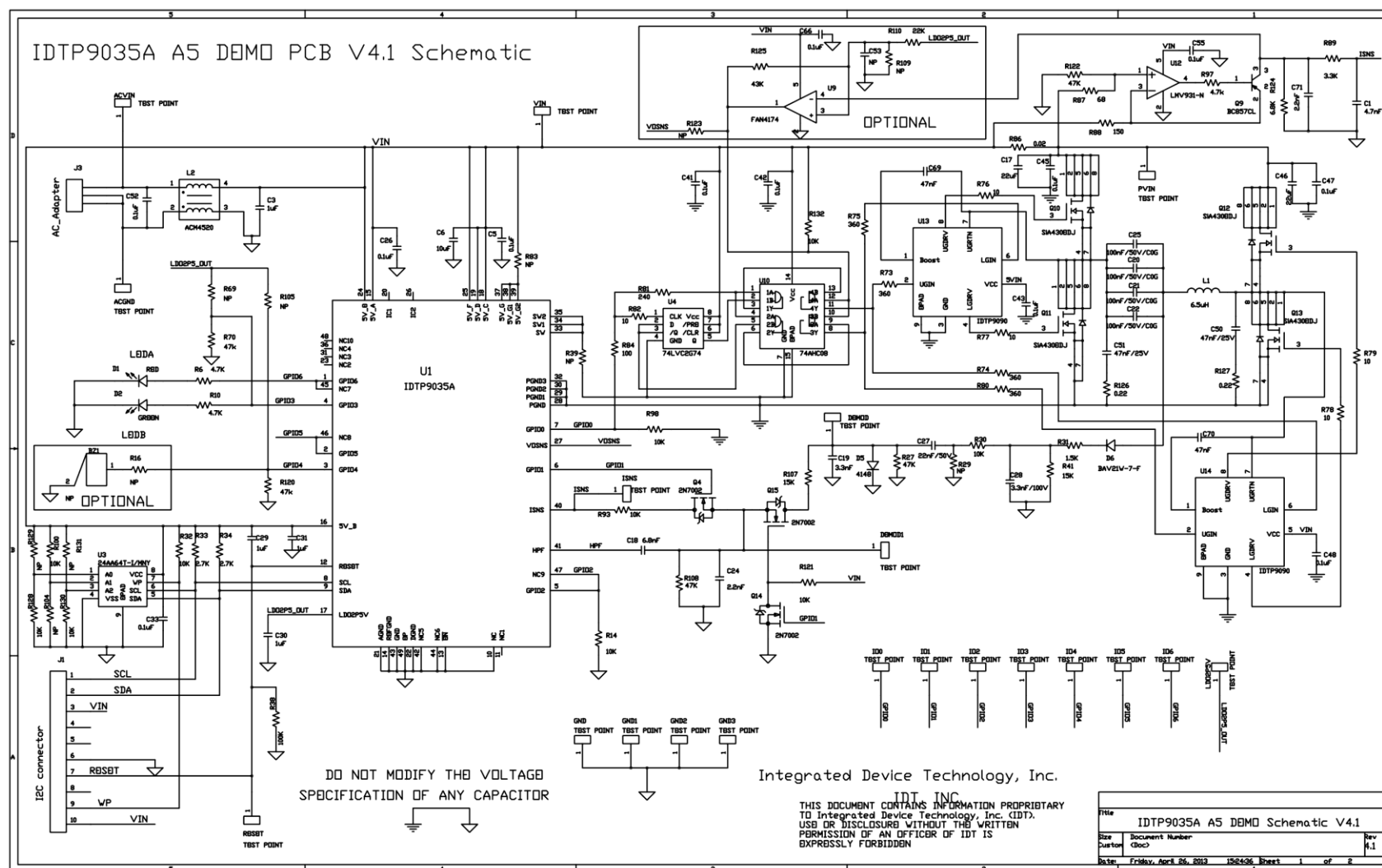
APPLICATIONS INFORMATION

Figure 9. IDTP9035A WPC "Qi" Compliance Schematic (See IDTP9035A Evaluation Kit User Manual for complete details)
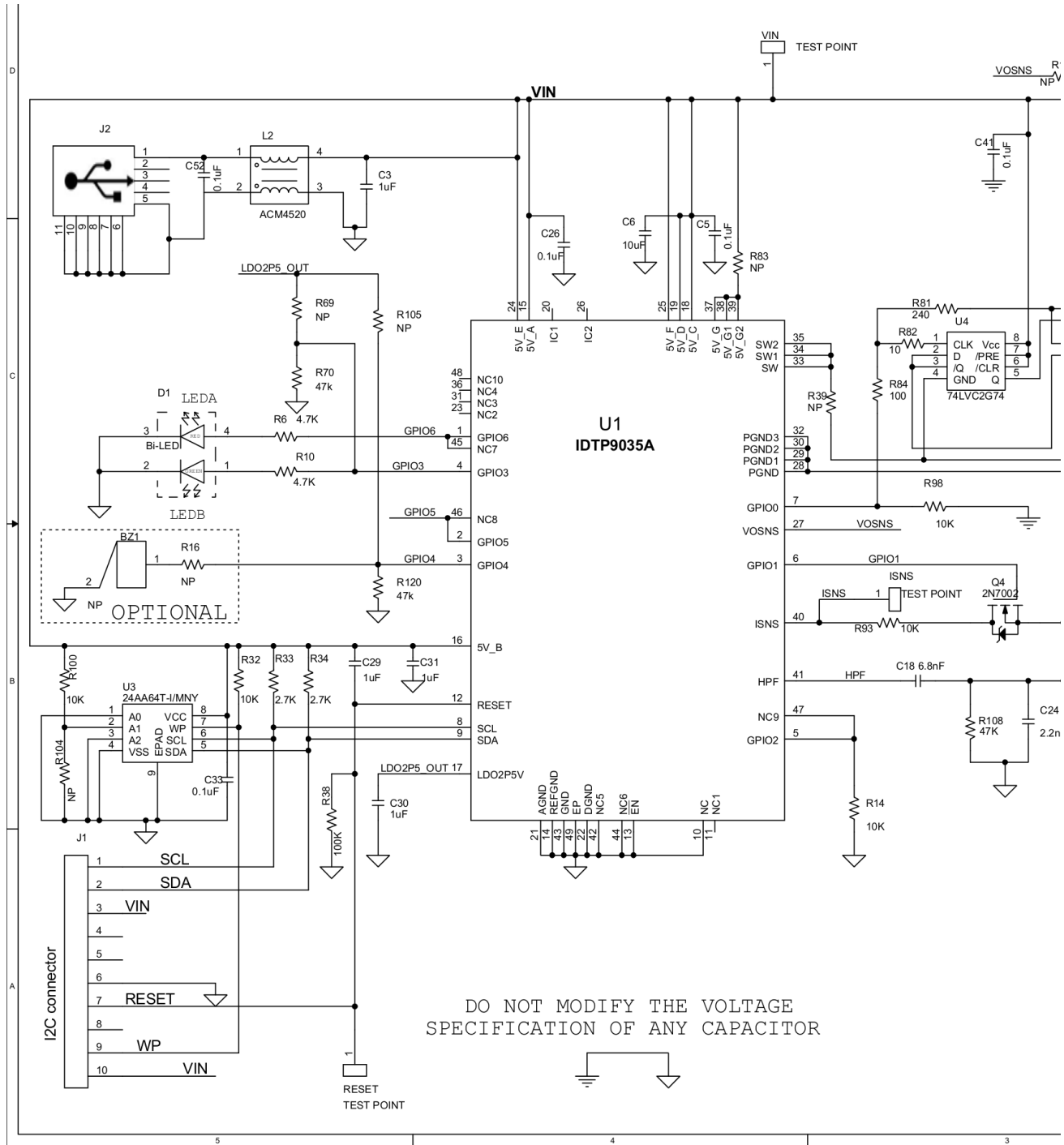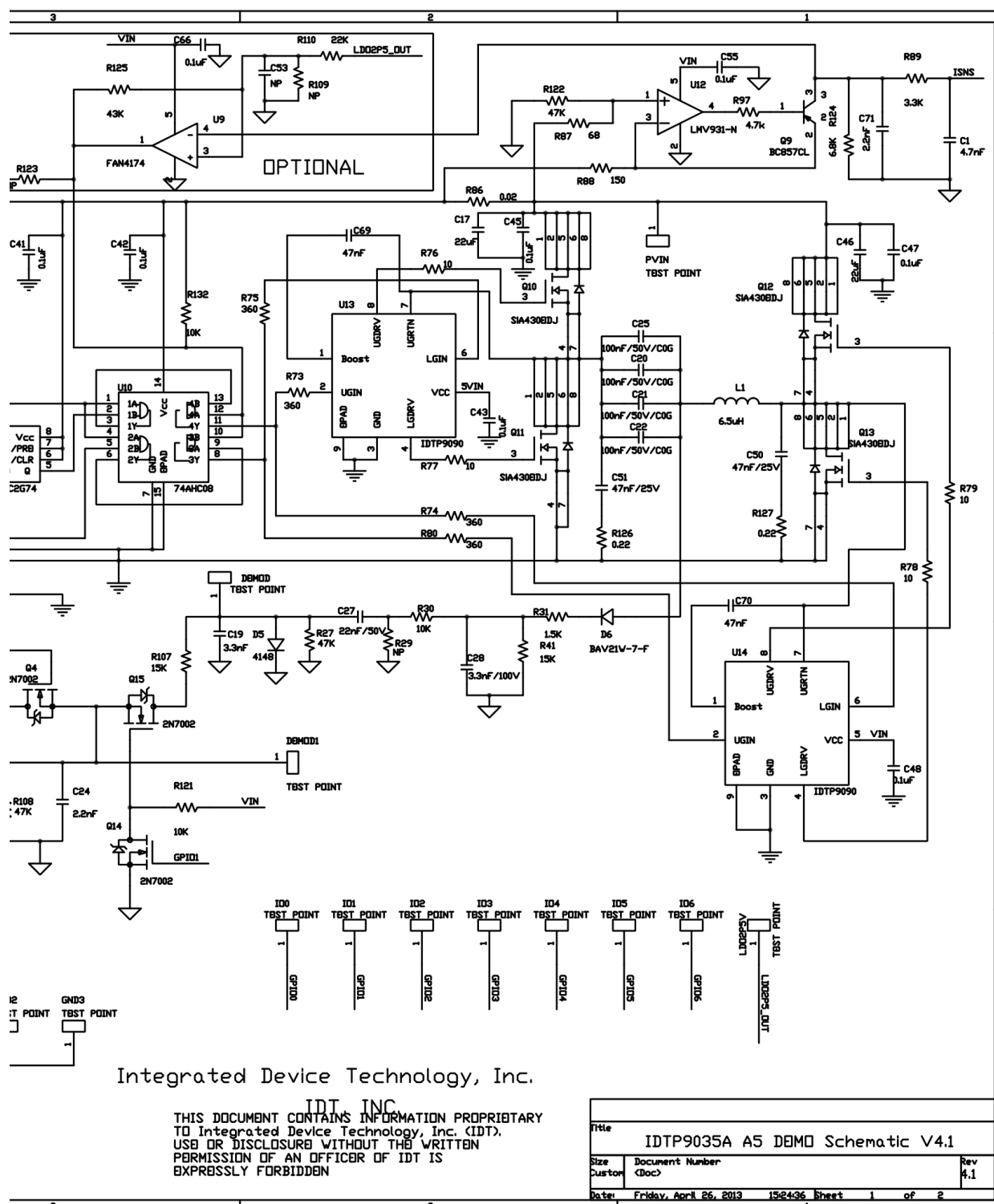
Figure 9a. Connections to the IDTP9035A

Figure 9b. External Drivers, Full-bridge, and Demodulator/Filter

Table 7. IDTP9035A WPC "Qi" Compliance Bill of Materials

Item	Quantity	Reference	Part	Part_Number	PCB Footprint
1	14	IO1,GND1,IO2,GND2,IO3, GND3,IO4,IO5,IO6,VIN, PVIN,GND,ACVIN,ACGND	TEST POINT	5015	TEST_PT_SM_135X70
2	1	BZ1	NP	PS1240P02CT3 (Optional)	buzz_ps1240
3	1	C1	4.7nF	C1005X7R1H472K050BA	402
4	4	C3,C29,C30,C31	1uF	C1608X7R1E105K	603
5	3	C5,C26,C33	0.1uF	GRM188R71H104KA93D	603
6	1	C6	10uF	C2012X5R1E106M	805
7	2	C17,C46	22uF	GRM31CR61E226KE15L	1206
8	1	C18	6.8nF	C1005X7R1H682K	402
9	1	C19	3.3nF	C1005X7R1H332K	402
10	4	C20,C21,C22,C25	100nF/50V/C0G	C3216C0G1H104J160AA	1206
11	2	C24,C71	2.2nF	C1005X7R1E222K	402
12	1	C27	22nF/50V	C1608X7R1H223K	603
13	1	C28	3.3nF/100V	C1608X7R2A332K	603
14	9	C41,C42,C43,C45,C47,C48, C52,C55,C66	0.1uF	C1005X7R1H104K	402
15	2	C50,C51	47nF/25V	C0805C473J3GACTU	805
16	2	C53,R69	NP	NP	402
17	2	C69,C70	47nF	GRM188R71C473KA01D	603
18	6	DEMOD1,LDO2P5V,RESET, ISNS,IO0,DEMOD	TEST POINT	NP	test_pt30dpad
19	1	D1	RED	L29K-G1J2-1-0-2-R18-Z	0603_DIODE
20	1	D2	GREEN	LG L29K-G2J1-24-Z	0603_DIODE
21	1	D5	4148	1N4148W-TP	sod123
22	1	D6	BAV21W-7-F	BAV21W-7-F	SOD123
23	1	J1	I2C connector	5103308-1	LOPRO8PIN01INREVB
24	1	J3	AC_Adapter	PJ-002BH	CONN_POWER_JACK5_5MM
25	1	L1	6.5uH	WT-505060-10K2-A11-G	ind_a11_Tx_Coil_smd
26	1	L2	ACM4520	ACM4520-901-2P-T000	TDK_ACM4520
27	3	Q4,Q14,Q15	2N7002	2N7002	SOT23_3
28	1	Q9	BC857CL	BC857CLT1G	SOT23_3
29	4	Q10,Q11,Q12,Q13	SiA430EDJ	SIA430EDJ-T1-GE3	sc70_6ld_fet
30	3	R6,R10,R97	4.7k	ERJ-2GEJ472X	402
31	7	R14,R32,R98,R100,R128, R130,R132	10K	ERJ-2GEJ103X	402
32	1	R16	NP	TBD	603
33	5	R27,R70,R108,R120,R122	47K	ERJ-2GEJ473X	402
34	1	R29	NP	NP	603
35	1	R30	10K	ERJ-3EKF1002V	603
36	1	R31	1.5K	ERJ-3EKF1501V	603
37	2	R33,R34	2.7K	ERJ-2GEJ272X	402
38	1	R38	100K	ERJ-2GEJ104X	402
39	4	R39,R105,R109,R123	NP	TBD	402
40	1	R41	15K	ERJ-3GEYJ153V	603
41	4	R73,R74,R75,R80	360	ERJ-3GEYJ361V	603
42	4	R76,R77,R78,R79	10	ERJ-3GEYJ100V	603
43	1	R81	240	ERJ-2GEJ241X	402
44	1	R82	10	ERJ-1GEJ100C	201
45	1	R83	NP	OPEN	603
46	1	R84	100	ERJ-3GEYJ101V	603
47	1	R86	0.02	WSL0805R0200FEA	805
48	1	R87	68	ERJ-2GEJ680X	402
49	1	R88	150	ERJ-2RKF1200X	402
50	1	R89	3.3K	ERJ-2GEJ332X	402
51	2	R93,R121	10K	RC0402FR-0710KL	402
52	3	R104,R129,R131	NP	OPEN	402
53	1	R107	15K	ERJ-2RKF1502X	402
54	1	R110	22K	ERJ-2RKF2202X	402
55	1	R124	6.8K	CRCW02016K80FKED	201
56	1	R125	43K	CRCW040243K0JNED	402
57	2	R126,R127	0.22	RL0816S-R22-F	603
58	1	U1	IDTP9035A	IDTP9035A	NTG_48LD_6X6MM_0P4PITCH
59	1	U3	24AA64T-I/MNY	24AA64T-I/MNY	DFN8
60	1	U4	74LVC2G74	74LVC2G74DP,125	TSSOP_8LD
61	1	U9	FAN4174	FAN4174IS5XCT	SOT_23_5
62	1	U10	74AHC08	74AHC08BQ,115	DHVQFN_14LD_2p5x3mm
63	1	U12	LMV931-N	LMV931-N	SC70_5LD
64	2	U13,U14	IDTP9090	IDTP9090	nlg8LD_3x3_0p65mm

Note 1: Recommended capacitor temperature/dielectric and voltage ratings: 100V capacitors are recommended because >50Vp-p voltage levels may appear on the resonance capacitors as stated in the WPC specification. C0G/NPO-type capacitor values stay relatively constant with voltage while X7R and X5R ceramic capacitor values change from -40% to over -80%, with the applied voltage. The decision to use lower voltage 50V capacitors or other type temperature/dielectric capacitors is left to the end user.

External Components

The IDTP9035A requires a minimum number of external components for proper operation (see the BOM in Table 7). A complete design schematic compliant to the WPC "Qi" standard is given in Figure 9. It includes WPC "Qi" LED and buzzer signaling, and an EEPROM for loading IDTP9035A firmware.

I²C Communication

The IDTP9035A includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the IDTP9035A will initially become I²C Master for the purpose of uploading firmware from an external memory device, such as an EEPROM. The I²C Master mode on the IDTP9035A does not support multi-master mode, and it is important for system designers to avoid any bus master conflict until the IDTP9035A has finished any firmware uploading and has released control of the bus as I²C Master. After any firmware uploading from external memory is complete, and when the IDTP9035A begins normal operation, the IDTP9035A is normally configured by the firmware to be exclusively in I²C Slave mode.

For maximum flexibility, the IDTP9035A tries to communicate with the first address on the EEPROM at 100kHz. If no ACK is received, communication is attempted at the other addresses at 300kHz.

EEPROM

The IDTP9035A requires an external EEPROM memory chip, pre-programmed with a standard start-up program that is automatically loaded when 5V power is applied. The IDTP9035A uses I²C slave address 0x52 to access the EEPROM. The IDTP9035A slave address is 0x39. The EEPROM can be reprogrammed to update the start-up program using the IDT Windows GUI (see the IDTP9035A-Qi Demo Board User Manual for complete details). A serial 8Kbyte (8Kx8 64Kbits) external EEPROM is sufficient.

If the standard firmware is not suitable for the application, custom ROM options are possible. Please contact IDT sales for more information. IDT will provide the appropriate image in the format best suited to the application.

Overview of Standard GPIO Usage

There are 7 GPIO's on the IDTP9035A transmitter IC, of which three are available for use as follows:

- GPIO3: Green LED_B to indicate standby, power transfer, and power complete; see Table 8.

- GPIO4: AC or DC buzzer (optional) with resistor options for different buzzer configurations (Not Yet Available).

- GPIO6: Red LED_A to indicate standby, fault conditions, and FOD warnings. Table 8 lists how the red and green LEDs can be used to display information about the IDTP9035A's operating modes. The table also includes information about external resistors or internal pull up/down options to select LED modes. Eight of the ten LED modes (those associated with advanced charging modes) are currently designated as "Future" modes.

All GPIOs are configured as inputs during the boot process, and then reconfigured according to Table 5.

LED FUNCTIONS

Two GPIOs are used to drive LEDs which indicate, through various on/off and illumination options, the state of charging and some possible fault conditions.

A red LED indicates various Fault and FOD ("Foreign Object Detection") states. The green LED indicates Power Transfer and Charge Complete state information. Upon power up, the two LEDs together may optionally indicate the Standby State and remain in this state until another of the defined Operational States occurs

As shown in Figure 10, one or two resistors configure the defined LED option combinations. The DC voltage set in this way is read one time during power-on to determine the LED configuration. To avoid interfering with the LED operation, the useful DC voltage range must be limited to not greater than 1Vdc.
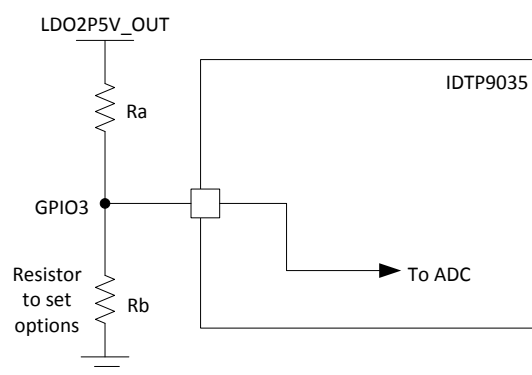
LED Mode Resistor Configuration

Figure 10. IDTP9035A LED Resistor Options.

LED Pattern Operational Status Definitions:

Blink Slow, Fast, repeat.

Table 8 – IDTP9035A LED Resistor Optioning (Not all options supported, shaded rows are for future development).

LED Control Option	LED Select Resistor Value	Description	LED #/ Color	Operational Status				FOD
				Standby	Transfer	Complete	Condition	Warning
1	Pull Down	Standby LEDs ON	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
2	R1	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
3	R2	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
4	R3	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
5	R4	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
6	Pull Up	Standby LEDs OFF	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
7	R5	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
8	R6	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
9	R7	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
10	R8	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST

R1-R8 are created using combination of two 1% resistors.

Designates Future Option

Buzzer Function

An optional buzzer feature is supported on GPIO4. The default configuration is an "AC" buzzer. The signal is created by toggling GPIO4 active-high/active-low at a 2kHz frequency.

Buzzer Action: Power Transfer Indication

The IDTP9035A supports audible notification when the device operation successfully reaches the Power Transfer state. The duration of the power transfer indication sound is 400ms.

The latency between reaching the Power Transfer state and sounding the buzzer does not exceed 500ms.

Additionally, the buzzer sound is concurrent within ±250ms of any change to the LED configuration indicating the start of power transfer.

Buzzer Action: No Power Transfer due to Foreign Object Detected (FOD)
When a major FOD situation is detected such that, for safety reasons, power transfer is not initiated, or that power transfer is terminated, the buzzer is sounded in a repeating sequence:

For 30 seconds: 400ms ON, 800ms OFF, repeat
Next 30 seconds: Off/silence (but no change to LED on/off patterns)
The pattern is repeated while the error condition exists

The buzzer is synchronized with the FOD LED such that the 400ms on tone corresponds with the red LED illumination and 800ms off (no sound) corresponds with the red LED being off.

Decoupling/Bulk Capacitors

As with any high-performance mixed-signal IC, the IDTP9035A must be isolated from the system power supply noise to perform optimally. A decoupling capacitor of 0.1µF must be connected between each power supply and the PCB ground plane as close to these pins as possible. For optimum device performance, the decoupling capacitor must be mounted on the component side of the PCB. Additionally, a medium value capacitor in the 10µF range must be used at the 5V_D input. To minimize ripple voltage and voltage droop due to the large current requirements of the Full-Bridge driver, a 22µF capacitor must be connected as close as possible to the drain of each top MOSFET of the external half-bridge. The value of the capacitors will decrease due to capacitance-to-applied voltage characteristics of the commonly-used ceramic dielectrics. For example, a 22µF X7R 6.3V capacitor's value is actually 6µF when operating at 5V, depending on the manufacturer.

ADC Considerations

The GPIO pins can be configured to connect internally to the successive approximation ADC through the ADC's input multiplexer. The ADC has a limited input range, so attention must be paid to the maximum VIN (2.4V). 0.01µF decoupling capacitors can be added to the GPIO inputs to minimize noise.

WPC TX-A5 or A11 Coil

The SW pin connects to a series-resonance circuit comprising a WPC Type-A5 or A11 coil (~6.5µH) and a series resonant capacitor (~400nF), as shown in Figure 9. The inductor serves as the primary coil in a loosely-coupled transformer, the secondary of which is the inductor connected to the power receiver (IDTP9020 or another).

The TX-A5 or A11 power transmitter coil is mounted on a ferrite shield to reduce EMI. The coil assembly can be mounted next to the IDTP9035A. Either ground plane or grounded copper shielding can be added beneath the ferrite shield for added reduction in radiated electrical field emissions. The coil ground plane/shield must be connected to the IDTP9035A ground plane by a single trace.

Resonance Capacitors

The resonance capacitors must be C0G type dielectric and have a DC rating to 100V. The highest-efficiency combination is four 100nF in parallel to get the lowest ESR. The part numbers are shown in Table 7.

LDO

Input Capacitor

The input capacitors must be located as physically close as possible to the power pin (5V_C) and power ground (GND). Ceramic capacitors are recommended for their low ESR and small profile. Also, ceramic capacitors are inherently more capable than are tantalum capacitors to withstand input current surges from low impedance sources such as batteries used in portable devices. Typically, 10V- or 16V-rated capacitors are required. The recommended external components are shown in Table 7.

Output Capacitor
For proper voltage regulation and stability, a capacitor is required on the output of the LDO. The output capacitor must be placed as close to the device and power (PGND) pins as possible. Since the LDO has been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

PCB Layout Considerations

- For optimum device performance and lowest output phase noise, the following guidelines must be observed. Please contact IDT for Gerber files that contain the recommended board layout.

- As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths.

- The 0.1μF decoupling capacitors must be mounted on the component side of the board as close as possible to the pins intended to be decoupled. Keep PCB traces to each VDD pin and to ground vias as short as possible.

- To optimize board layout, place all components on the same side of the board. Route signal traces away from the IDTP9035A

- The NQG48 6.0 mm x 6x0 mm x 75mm 48L package has an inner thermal pad which requires blind assembly. It is recommended that a more active flux solder paste be used such as Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT for Gerber files that contain recommended solder stencil design.

- The package center exposed pad (EP) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EP) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of plated-through-hole (PTH) vias embedded in the PCB center land pad for the NTG48. The PTH vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board.

- On the solder side of the board, these thermal vias embed in a copper fill having the same dimensions as the center land pad on the component side. Recommendations for the via finished hole-size and array pitch are 0.3mm to 0.33mm and 1.3mm, respectively.

- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques must then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:

1. PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces.
2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
3. Thermal vias are needed to provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.
4. Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).

Power Dissipation/Thermal Requirements

The IDTP9035A is offered in a TQFN-48L package. The maximum power dissipation capability is 1.3W, limited by the die's specified maximum operating junction temperature, T_J, of 125℃. The junction temperature rises with the device power dissipation based on the package thermal resistance. The package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 31°C/W when the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB Layout section need to be followed when designing the printed circuit board layout, as well as the placement of the IDTP9035A IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size, and internal package construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB itself upon which the TQFN is mounted. Changing the design or configuration of the

PCB changes impacts the overall thermal resistivity and, thus, the board's heat sinking efficiency.

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:
1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation must be calculated:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation (W)

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the IDTP9035A device is 150°C. The thermal resistance of the 48-pin NQG package (NGQ48) is optimally θ_{JA}=30°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is:

$P_{D(Max)}$ = (125°C - 85°C) / 30°C/W $\cong$ 1.3 Watt

Thermal Overload Protection

The IDTP9035A integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 140°C. To allow the maximum load current on each regulator and resonant transmitter, and to prevent thermal overload, it is important to ensure that the heat generated by the IDTP9035A is dissipated into the PCB. The package exposed paddle must be soldered to the PCB, with multiple vias evenly distributed under the exposed paddle and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

Special Notes

NQG TQFN-48 Package Assembly
Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for minimum of 8 hours at 125°C within 24 hours of the assembly reflow process.
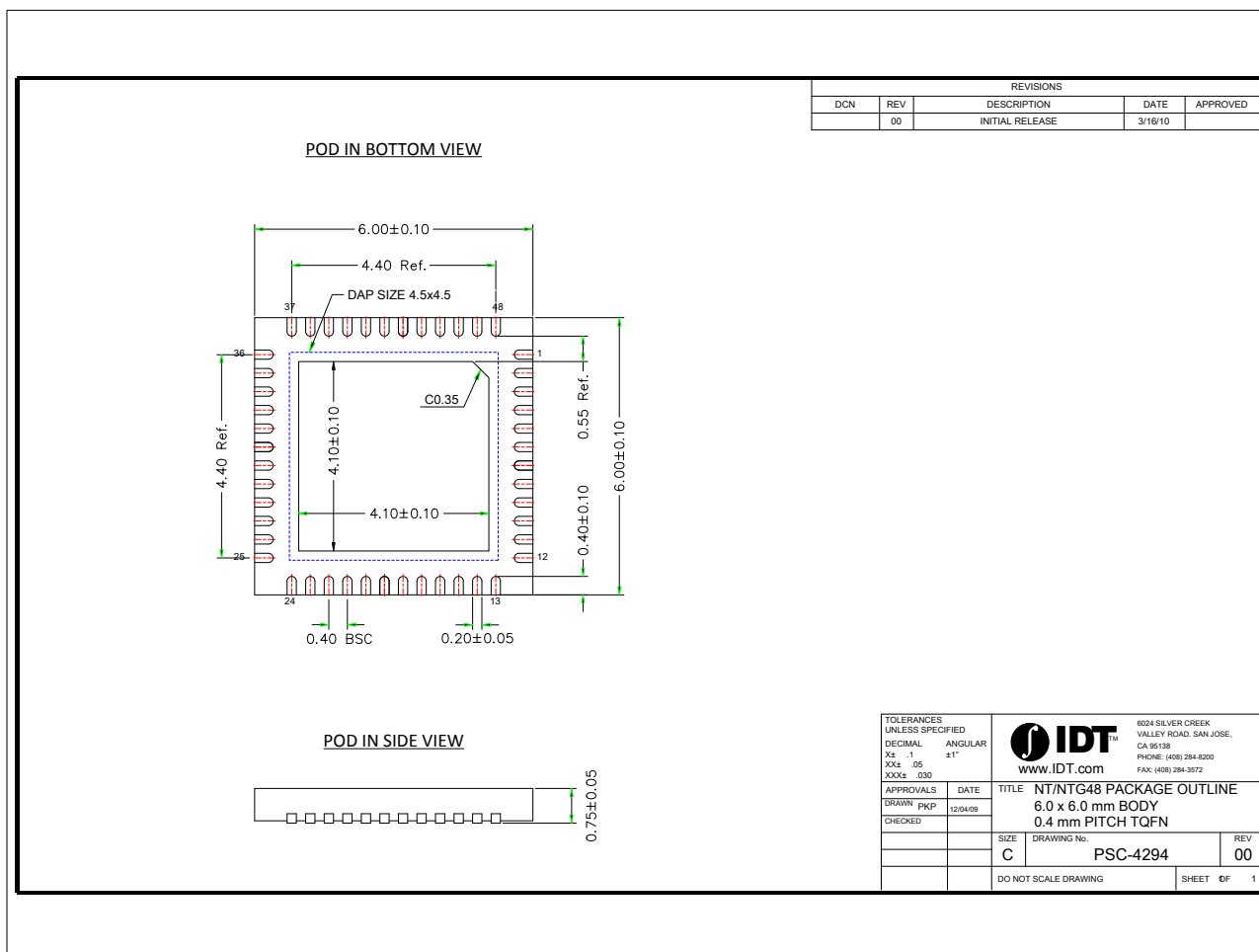
PACKAGE OUTLINE DRAWING

Figure 11. IDTP9035A Package Outline Drawing (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm48L, 0.4mm pitch)

ORDERING GUIDE

Table 9. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9035A-0NTGI	P9035ANTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tray	25
P9035A-0NTGI8	P9035ANTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tape and Reel	2,500

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