# ES_LPC11Axx

## Errata sheet LPC11Axx

**Rev. 2 — 15 January 2013** **Errata sheet**

### Document information

| Info | Content |
|---|---|
| **Keywords** | LPC11A02UK; LPC11A04UK; LPC11A11FHN33; LPC11A12FHN33; LPC11A12FBD48; LPC11A13FHI33; LPC11A14FHN33; LPC11A14FBD48 LPC11Axx errata |
| **Abstract** | This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.<br>Each deviation is assigned a number and its history is tracked in a table. |

### Revision history

| Rev | Date | Description |
|---|---|---|
| 2 | 20130115 | Added I2C.1. |
| 1.2 | 20120719 | Added UVLO.1. |
| 1.1 | 20120601 | Added Rev. ‘B’. |
| 1 | 20120401 | Initial version. |

## Contact information

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# 1. Product identification

The LPC11Axx devices typically have the following top-side marking:

LPC11Axx

/xxx

xxxxxxx

xxYYWWxR[x]

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC11Axx:

**Table 1. Device revision table**

| Revision identifier (R) | Revision description |
|---|---|
| 'A' | Initial device revision |
| 'B' | Second device revision |

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

# 2. Errata overview

**Table 2. Errata summary table**

| Functional problems | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| I2C.1 | In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. | 'A', 'B' | Section 3.1 |
| UVLO.1 | Double reset occurs during initial cold start-up when temperature is −20 °C and $V_{DD}$ ramp rate is >40 ms | 'A', 'B' | Section 3.2 |

**Table 3. AC/DC deviations table**

| AC/DC deviations | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| n/a | n/a | n/a | n/a |

**Table 4. Errata notes table**

| Errata notes | Short description | Revision identifier | Detailed description |
|---|---|---|---|
| Note.1 | During power-up, an unexpected glitch (low pulse) could occur on the port pins as the $V_{DD}$ supply ramps up. | 'A', 'B' | Section 5.1 |
| Note.2 | Rev A version does not support boot ROM power profiles. | 'A' | Section 5.2 |

# 3. Functional problems detail

## 3.1 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

### Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I2C bus in a non-intrusive way.

### Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I2C bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

### Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

## 3.2 UVLO.1: Double reset occurs during initial cold start-up when temperature is –20 °C and $V_{DD}$ ramp rate is >40 ms

### Introduction:

The UnderVoltage LockOut (UVLO) provides protection against power supply droop below 2.4 V. When the $V_{DD}$ ramps up to 2.4 V (UVLO threshold voltage level), the device comes out of reset and starts executing the boot ROM and application code.

### Problem:

For cold start-ups only, as $V_{DD}$ initially ramps up from ground, the device comes briefly out of reset and starts execution of the program code before the device returns to reset. Under the conditions where the temperature is below –20 °C and the a $V_{DD}$ ramp rate is 40 ms or greater, a double reset of the LPC11Axx occurs during the initial cold power-up.

### Work-around:

For a hardware fix, a decoupling capacitor can be placed on the $\overline{\text{RESET}}$ pin with a minimum value of 5 μF.

If a software fix is desired, the BOD reset flag can be monitored. The software should loop until the BOD reset flag is set. The software fix is restricted to a $V_{DD}$ ramp time of 0.9 ms or greater at all operating temperatures.

Software fix loop code example:

```
while (!(LPC_SYSCON->SYSRSTSTAT & (0x1<<3)))        //while no reset is detected...

{LPC_SYSCON->SYSRSTSTAT |= (1<<3);  }    //clear BOD status bit and repeat loop
```

# 4. AC/DC deviations detail

## 4.1 n/a

# 5. Errata notes detail

## 5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the $V_{DD}$ level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the $V_{DD}$ supply ramps up.

## 5.2 Note.2

Rev A version does not support boot ROM power profiles.

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