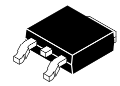
DATA SHEET
www.onsemi.com

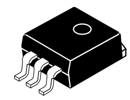
Voltage Regulator – 2% and 4%

400 mA

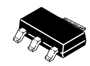
NCV4274, NCV4274A



DPAK
DT SUFFIX
CASE 369C



D2PAK
DS SUFFIX
CASE 418AF



SOT−223
ST SUFFIX
CASE 318E

Description

The NCV4274 and NCV4274A is a precision micro−power voltage regulator with an output current capability of 400 mA available in the DPAK, D2PAK and SOT−223 packages.

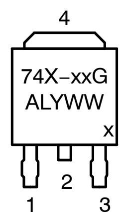
The output voltage is accurate within ±2.0% or ±4.0% depending on the version with a maximum dropout voltage of 0.5 V with an input up to 40 V. Low quiescent current is a feature drawing only 150 μA with a 1 mA load. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

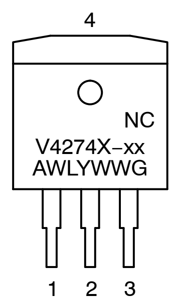
Features

- 2.5, 3.3 V, 5.0 V, 8.5 V, ±2.0% Output Options
- 2.5, 3.3 V, 5.0 V, ±4.0% Output Options
- Low 150 μA Quiescent Current at 1 mA load current
- 400 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage with Respect to GND
    - −42 V Reverse Voltage
    - Short Circuit
    - Thermal Overload
- Very Low Dropout Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

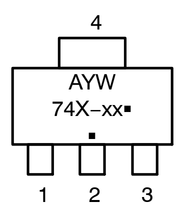
MARKING DIAGRAMS



1 Input
2, 4 Ground
3 Output



1 Input
2, 4 Ground
3 Output



1 Input
2, 4 Ground
3 Output

X	= A or blank
xx	= Voltage Ratings
A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
WW, W	= Work Week
G, ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 15.

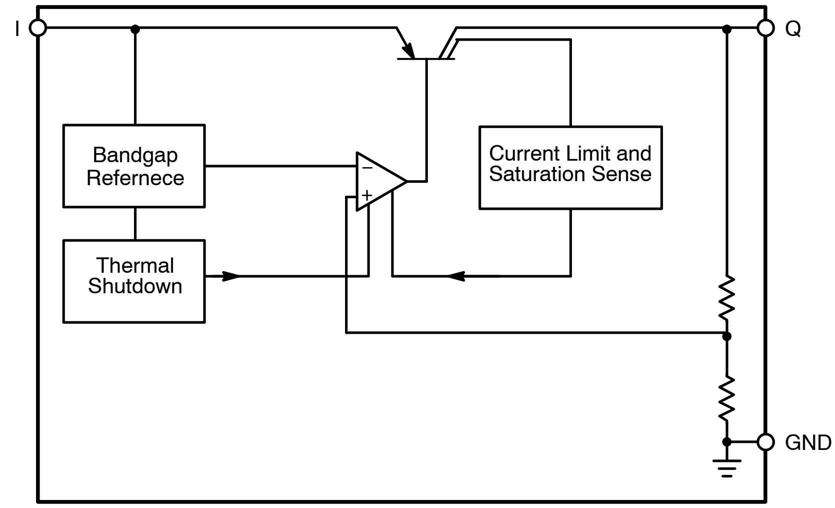


Figure 1. Block Diagram

Pin Definitions and Functions

Symbol	Pin No.	Function
I	1	Input; Bypass directly at the IC a ceramic capacitor to GND.
GND	2,4	Ground
Q	3	Output; Bypass with a capacitor to GND.

1. DPAK 3LD package code 6025
2. D2PAK 3LD package code 6083

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin Symbol, Parameter		Condition	Min	Max	Unit
V_I	**I**, Input−to−Regulator	Voltage		−42	45	V
I_I		Current		Internally Limited	Internally Limited	
V_I	**I**, Input peak Transient Voltage to Regulator with Respect to GND				60	V
V_Q	**Q,** Regulated Output	Voltage	$V_Q = V_I$	−1.0	40	V
I_Q		Current		Internally Limited	Internally Limited	
I_{GND}	**GND,** Ground Current			–	100	mA
T_J T_{Stg}	Junction Temperature Storage Temperature			– −50	150 150	°C °C
ESD_{HB}	ESD Capability, Human Body Model			4		kV
ESD_{MM}	ESD Capability, Machine Model			200		V
ESD_{CDM}	ESD Capability, Charged Device Model			1		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD CDM tested per EIA/JES D22/C101, Field Induced Charge Model

OPERATING RANGE

Symbol	Parameter	Condition	Min	Max	Unit
V_I	Input Voltage (8.5 V Version)		9.0	40	V
V_I	Input Voltage (5.0 V Version)		5.5	40	V
V_I	Input Voltage (3.3 V, and 2.5 V Version)		4.5	40	V
T_J	Junction Temperature		−40	150	°C

THERMAL RESISTANCE

Symbol	Parameter		Condition	Min	Max	Unit
R_{thja}	Junction−to−Ambient	DPAK		−	70 (Note 4)	°C/W
R_{thja}	Junction−to−Ambient	D2PAK		−	60 (Note 4)	°C/W
R_{thjc}	Junction−to−Case	DPAK		−	4	°C/W
R_{thjc}	Junction−to−Case	D2PAK		−	3	°C/W
Ψ−JLX, Ψ_{LX}	Junction−to−Tab	SOT−223		−	14.5 (Note 5)	°C/W
$R_{\theta JA}$, θ_{JA}	Junction−to−Ambient	SOT−223		−	169.7 (Note 5)	°C/W

4. Soldered in, minimal footprint, FR4
5. 1 oz copper, 5 mm^2 copper area, FR4

LEAD FREE SOLDERING TEMPERATURE AND MSL

Symbol	Parameter	Condition	Min	Max	Unit
T_{sld}	Lead Free Soldering, (Note 6) Reflow (SMD styles only), Pb−Free	60s − 150s Above 217s 40s Max at Peak	−	265 pk	°C
MSL	Moisture Sensitivity Level	DPAK and D2PAK SOT−223	1 3	− −	

6. Per IPC/JEDEC J−STD−020C

ELECTRICAL CHARACTERISTICS
−40°C < T_J < 150°C; V_I = 13.5 V unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
			NCV4274A			NCV4274			
REGULATOR									
V_Q	Output Voltage (8.5 V Version)	5 mA < I_Q < 200 mA 9.5 V < V_I < 40 V	8.33	8.5	8.67	–	–	–	V
V_Q	Output Voltage (8.5 V Version)	5 mA < I_Q < 400 mA 9.5 V < V_I < 28 V	8.33	8.5	8.67	–	–	–	V
V_Q	Output Voltage (5.0 V Version)	5 mA < I_Q < 400 mA 6 V < V_I < 28 V	4.9	5.0	5.1	4.8	5.0	5.2	V
V_Q	Output Voltage (5.0 V Version)	5 mA < I_Q < 200 mA 6 V < V_I < 40 V	4.9	5.0	5.1	4.8	5.0	5.2	V
V_Q	Output Voltage (3.3 V Version)	5 mA < I_Q < 400 mA 4.5 V < V_I < 28 V	3.23	3.3	3.37	3.17	3.3	3.43	V
V_Q	Output Voltage (3.3 V Version)	5 mA < I_Q < 200 mA 4.5 V < V_I < 40 V	3.23	3.3	3.37	3.17	3.3	3.43	V
V_Q	Output Voltage (2.5 V Version)	5 mA < I_Q < 400 mA 4.5 V < V_I < 28 V	2.45	2.5	2.55	2.4	2.5	2.6	V
V_Q	Output Voltage (2.5 V Version)	5 mA < I_Q < 200 mA 4.5 V < V_I < 40 V	2.45	2.5	2.55	2.4	2.5	2.6	V
I_Q	Current Limit	–	400	600	–	400	600	–	mA
I_q	Quiescent Current	I_Q = 1 mA V_Q = 8.5 V V_Q = 5.0 V V_Q = 3.3 V V_Q = 2.5 V I_Q = 250 mA V_Q = 8.5 V V_Q = 5.0 V V_Q = 3.3 V V_Q = 2.5 V I_Q = 400 mA V_Q = 8.5 V V_Q = 5.0 V V_Q = 3.3 V V_Q = 2.5 V	 – – – – – – – – – – – –	 195 190 145 140 10 10 13 12 20 20 30 28	 250 250 250 250 15 15 20 20 35 35 45 45	 – – – – – – – – – – – –	 – 190 145 140 – 10 13 12 – 20 30 28	 – 250 250 250 – 15 20 20 – 35 45 45	 μA μA μA μA mA mA mA mA mA mA mA mA
V_{DR}	Dropout Voltage 8.5 V Version 5.0 V Version 3.3 V Version 2.5 V Version	I_Q = 250 mA, $V_{DR} = V_I - V_Q$ V_I = 8.5 V V_I = 5.0 V V_I = 4.5 V V_I = 4.5 V	 – – – –	 250 250 – –	 500 500 1.27 2.05	 – – – –	 – 250 – –	 – 500 1.33 2.1	 mV mV V V
ΔV_Q	Load Regulation	I_Q = 5 mA to 400 mA	–	7	20	–	7	30	mV
ΔV_Q	Line Regulation	ΔV_I = 12 V to 32 V I_Q = 5 mA	–	10	25	–	10	25	mV
P_{SRR}	Power Supply Ripple Rejection	fr = 100 Hz, V_r = 0.5 V_{PP}	–	60	–	–	60	–	dB
$\Delta V_Q/\Delta T$	Temperature output voltage drift		–	0.5	–	–	0.5	–	mV/K
T_{SD}	Thermal Shutdown Temperature*	I_Q = 5 mA	165	–	210	165	–	210	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Guaranteed by design, not tested in production

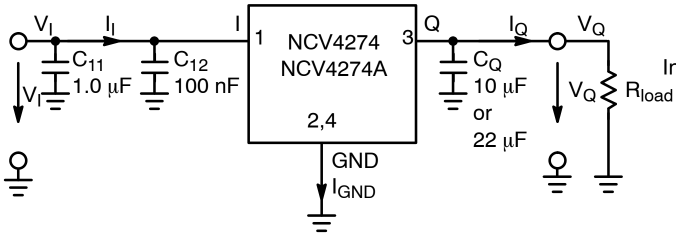


Figure 2. Measuring Circuit

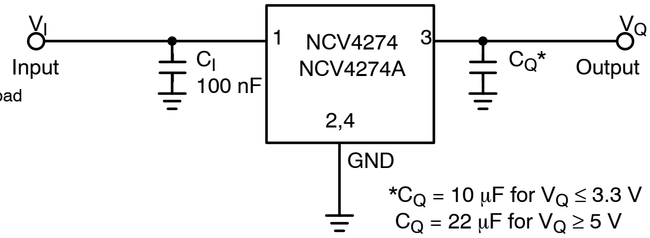


Figure 3. Application Circuit

TYPICAL CHARACTERISTIC CURVES

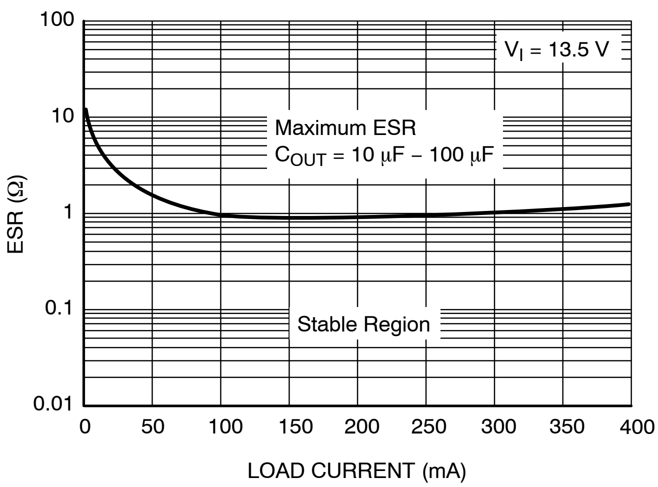


Figure 4. ESR Characterization − 3.3 V, 5 V and 8.5 V Versions

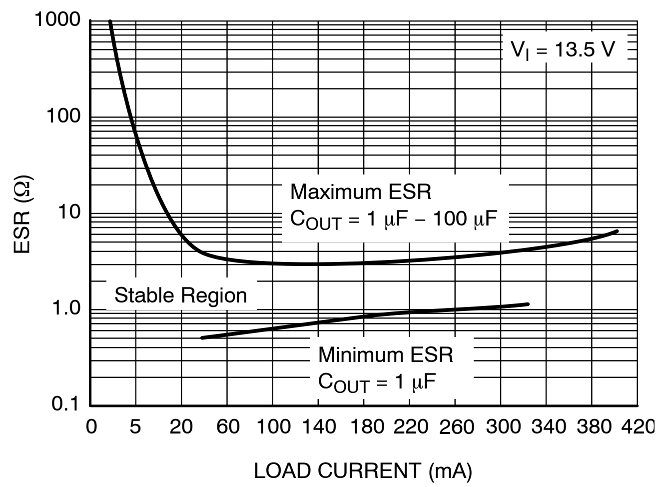


Figure 5. ESR Characterization − 2.5 V Version

TYPICAL CHARACTERISTIC CURVES – 8.5 V VERSION

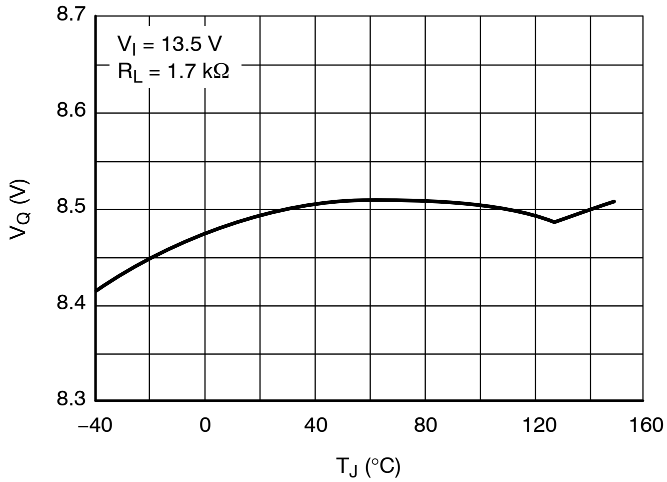


Figure 6. Output Voltage vs. Junction Temperature

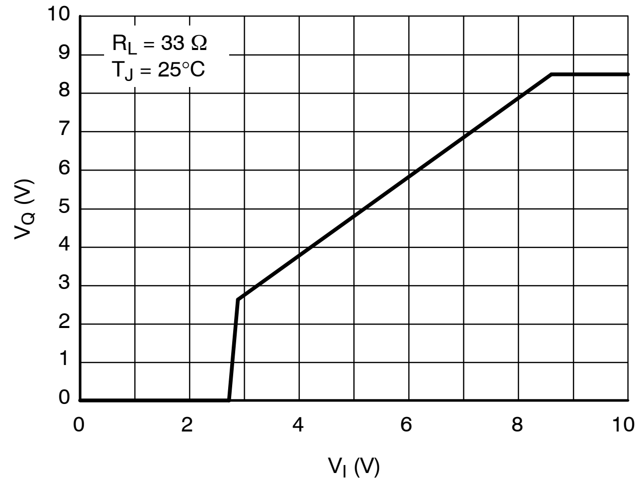


Figure 7. Output Voltage vs. Input Voltage

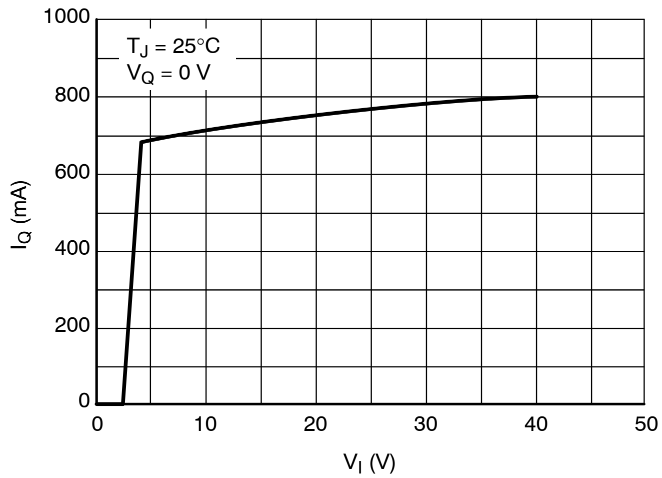


Figure 8. Output Current vs. Input Voltage

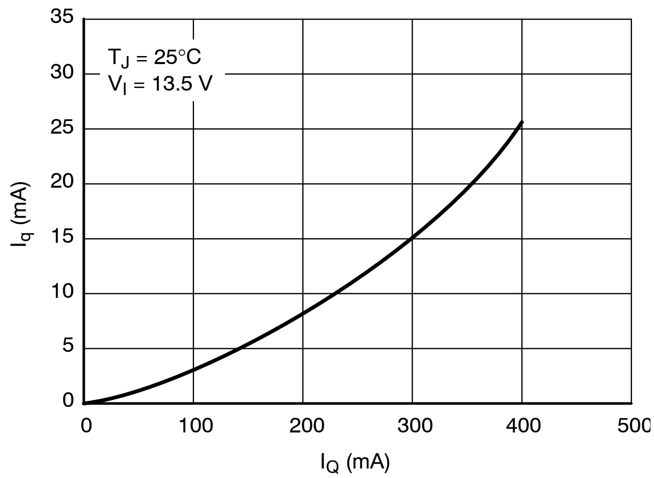


Figure 9. Current Consumption vs. Output Current (High Load)

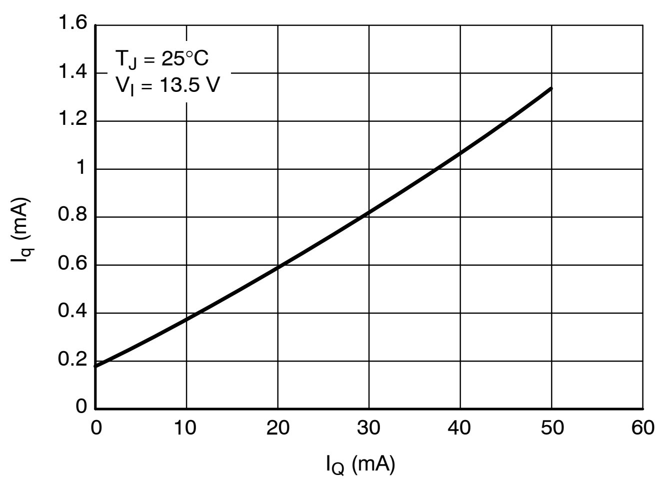


Figure 10. Current Consumption vs. Output Current (Low Load)

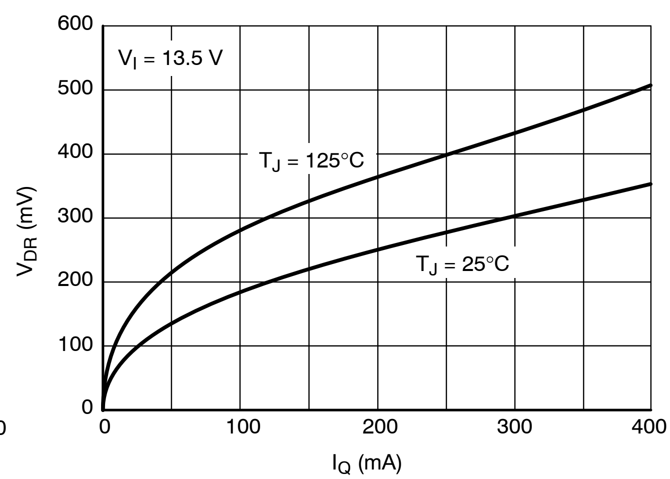


Figure 11. Drop Voltage vs. Output Current

TYPICAL CHARACTERISTIC CURVES – 8.5 V VERSION (continued)

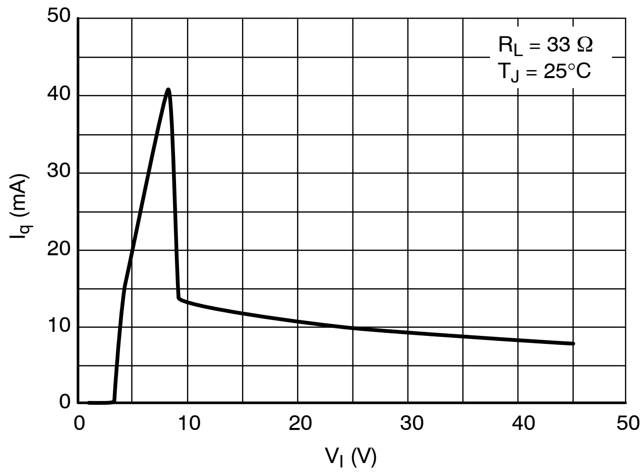


Figure 12. Current Consumption vs. Input Voltage

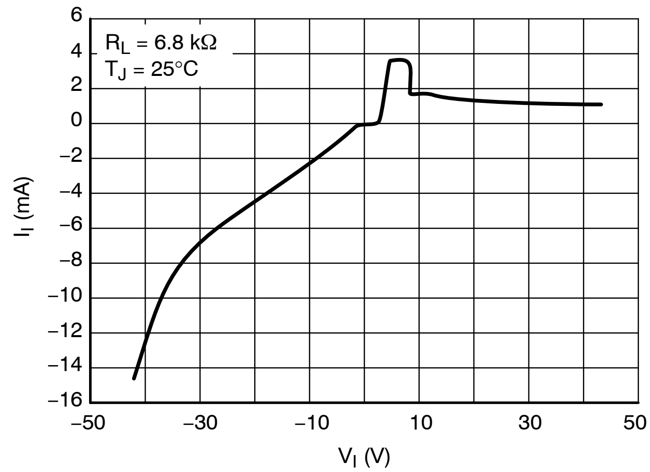


Figure 13. Input Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 5.0 V VERSION

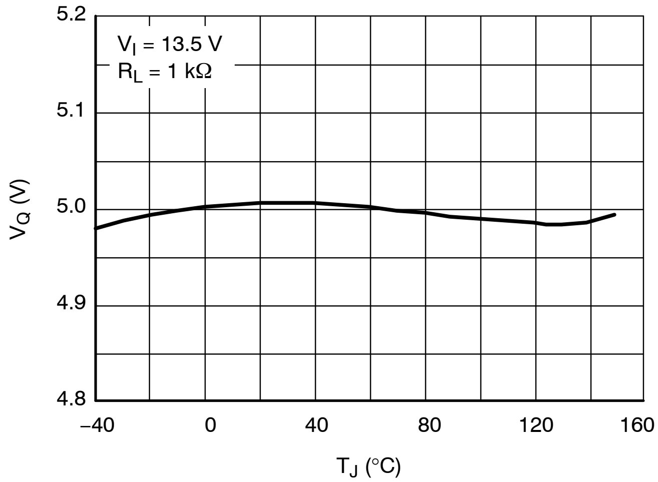


Figure 14. Output Voltage vs. Junction Temperature

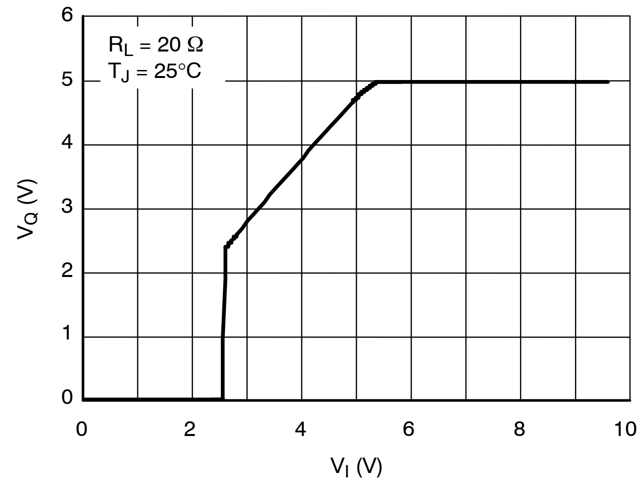


Figure 15. Output Voltage vs. Input Voltage

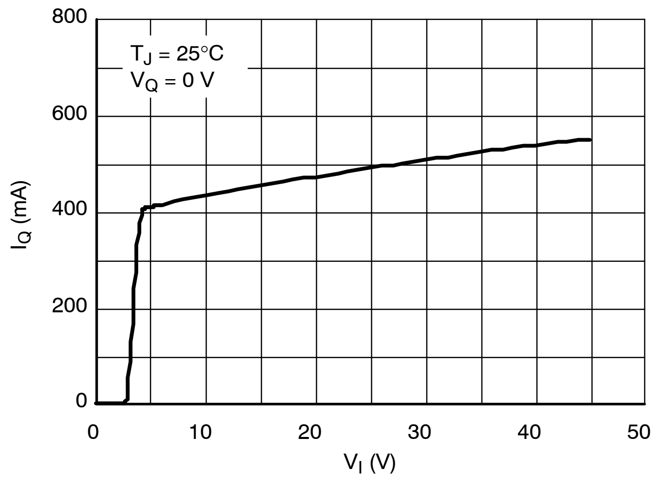


Figure 16. Output Current vs. Input Voltage

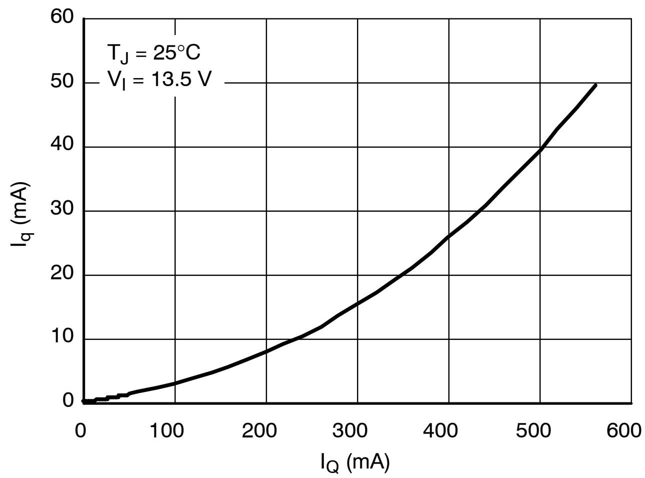


Figure 17. Current Consumption vs. Output Current (High Load)

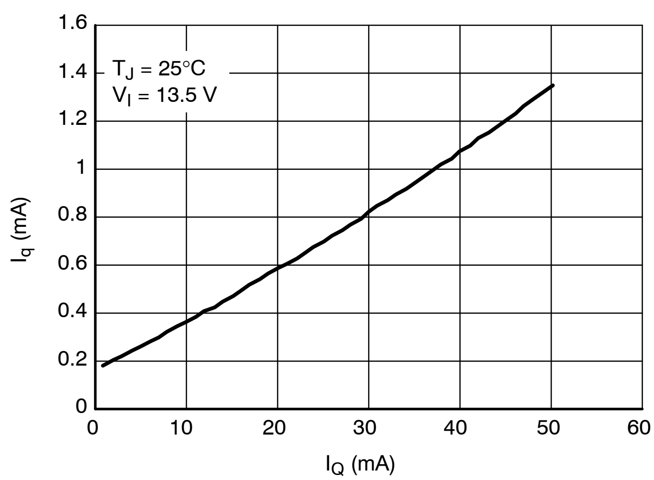


Figure 18. Current Consumption vs. Output Current (Low Load)

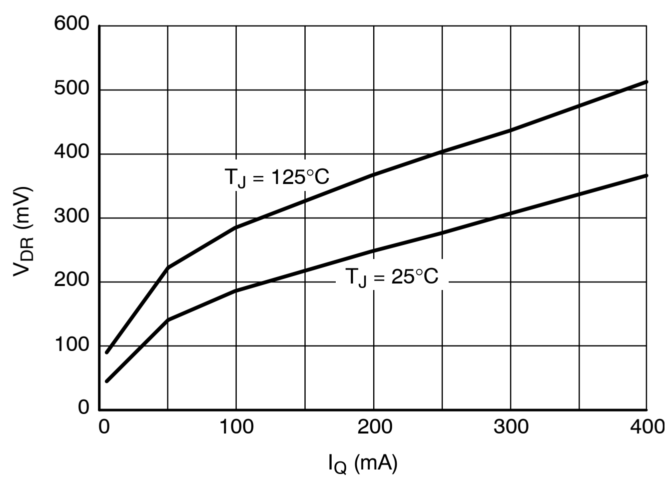


Figure 19. Drop Voltage vs. Output Current

TYPICAL CHARACTERISTIC CURVES – 5.0 V VERSION (continued)

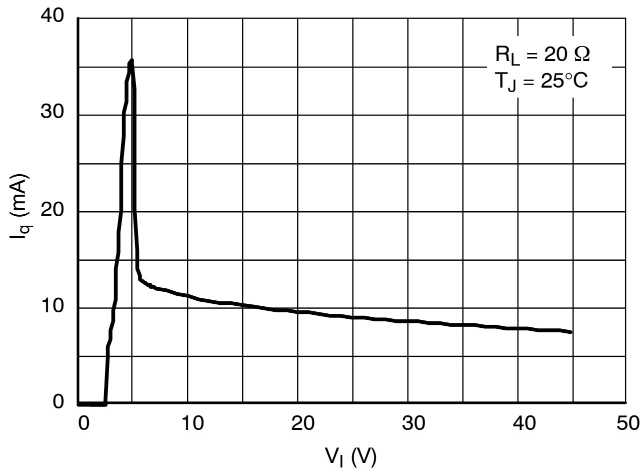


Figure 20. Current Consumption vs. Input Voltage

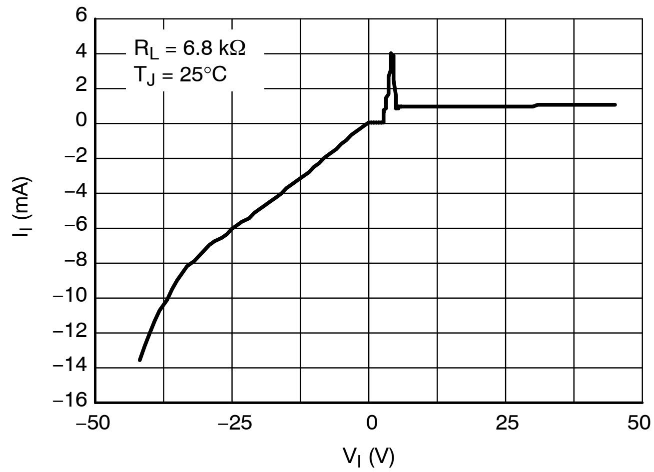


Figure 21. Input Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION

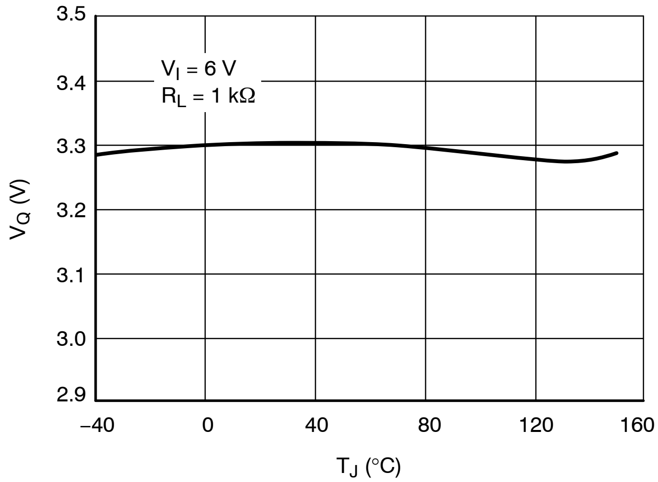


Figure 22. Output Voltage vs. Junction Temperature

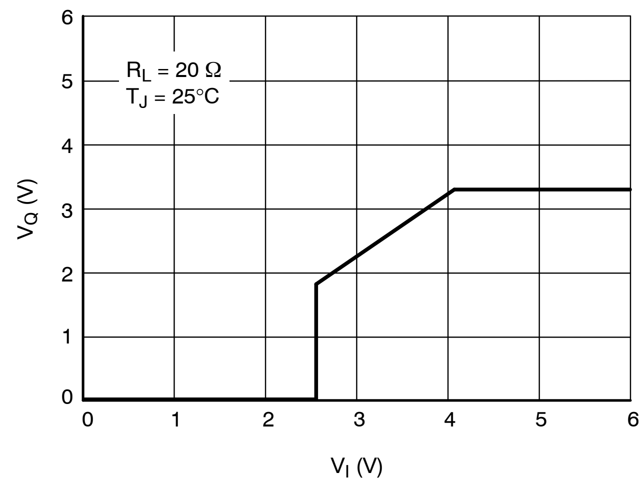


Figure 23. Output Voltage vs. Input Voltage

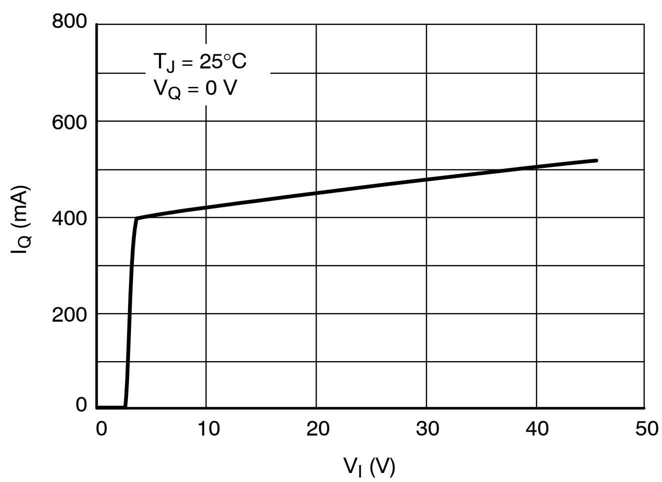


Figure 24. Output Current vs. Input Voltage

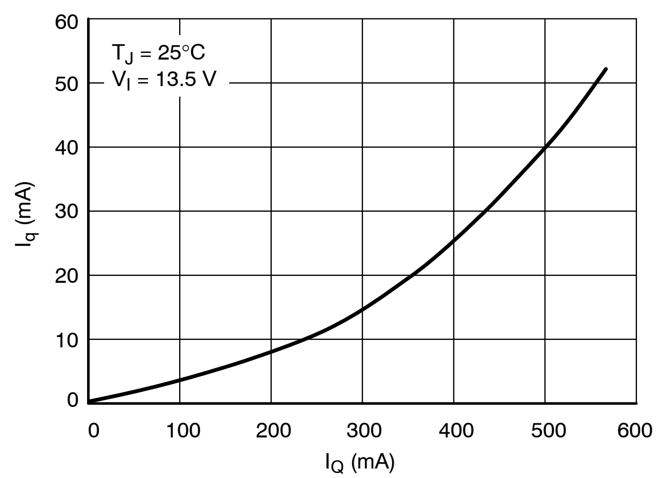


Figure 25. Current Consumption vs. Output Current (High Load)

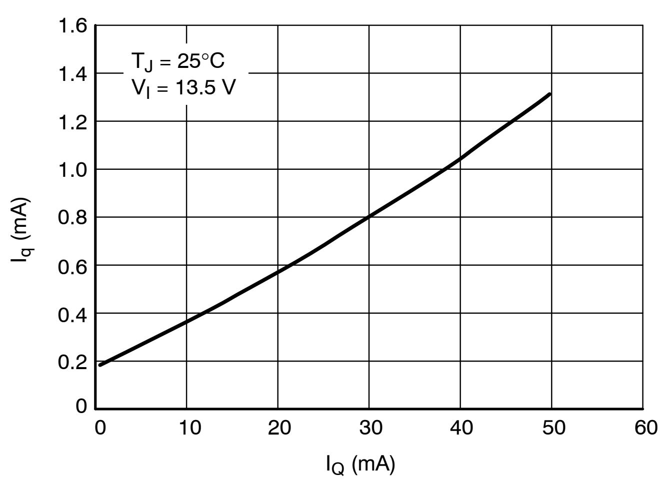


Figure 26. Current Consumption vs. Output Current (Low Load)

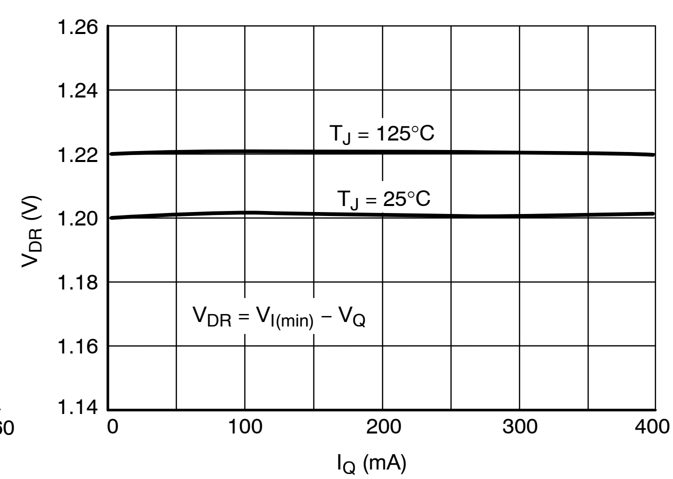


Figure 27. Voltage Drop vs. Output Current

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION (continued)

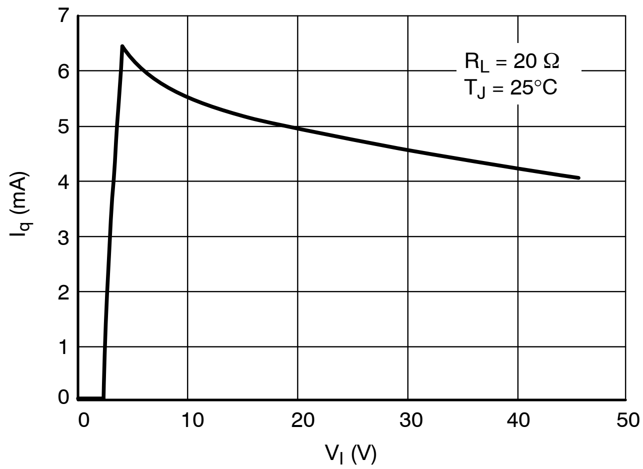


Figure 28. Current Consumption vs. Input Voltage

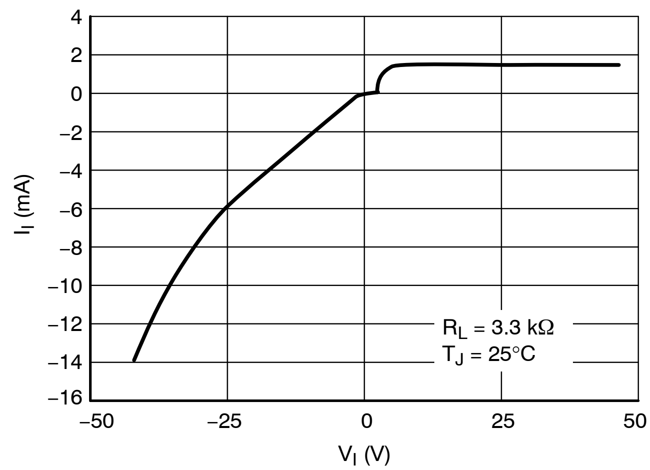


Figure 29. Input Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 2.5 V VERSION

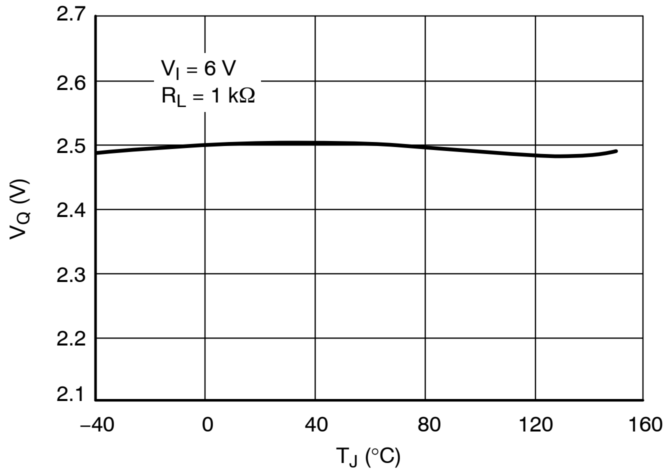


Figure 30. Output Voltage vs. Junction Temperature

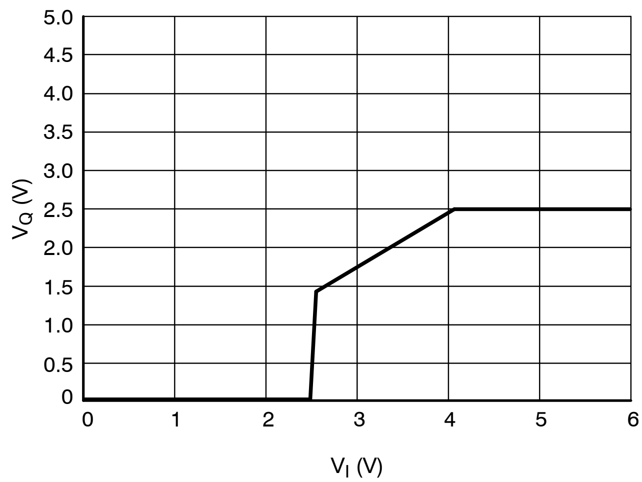


Figure 31. Output Voltage vs. Input Voltage

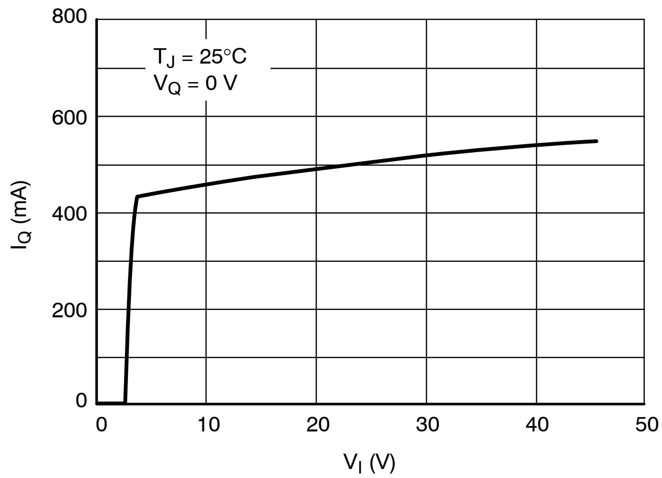


Figure 32. Output Current vs. Input Voltage

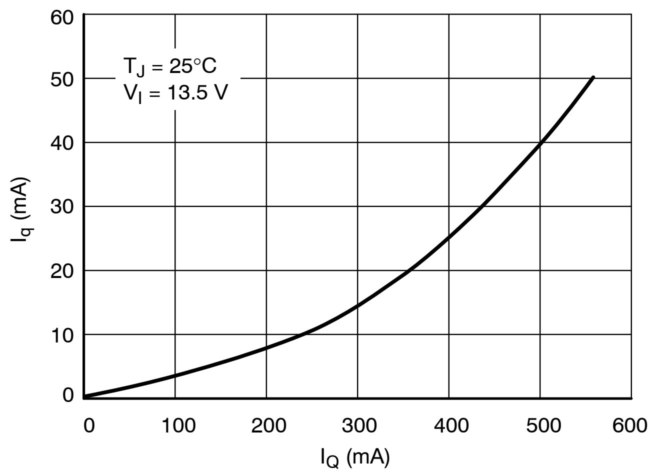


Figure 33. Current Consumption vs. Output Current (High Load)

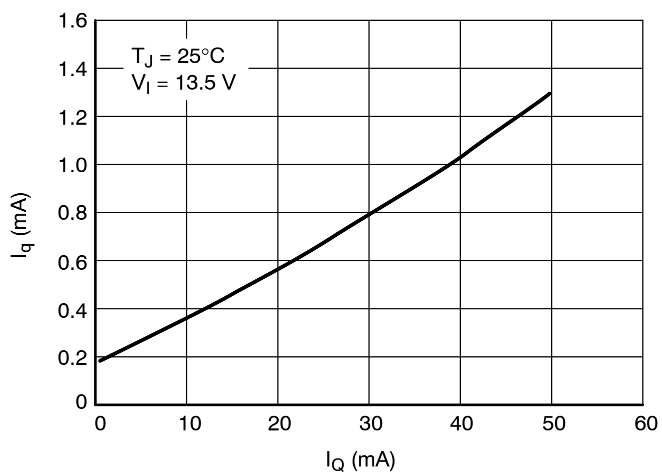


Figure 34. Current Consumption vs. Output Current (Low Load)

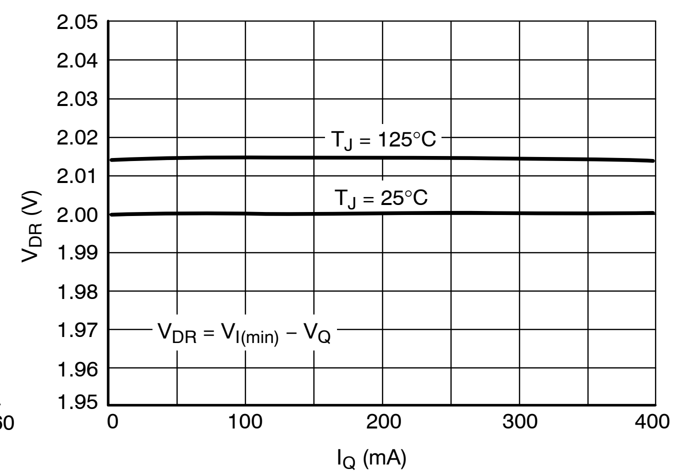


Figure 35. Voltage Drop vs. Output Current

TYPICAL CHARACTERISTIC CURVES – 2.5 V VERSION (continued)

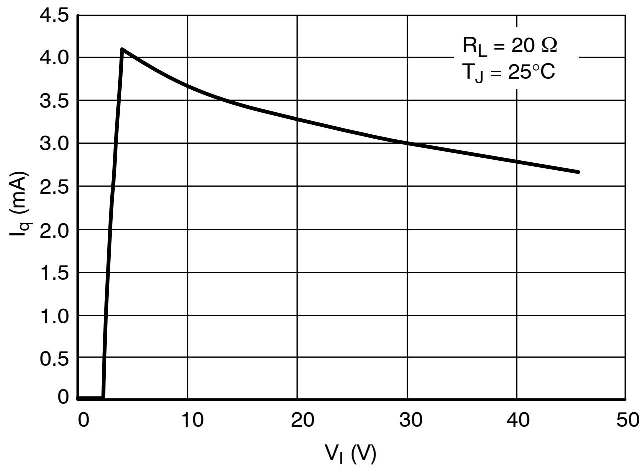


Figure 36. Current Consumption vs. Input Voltage

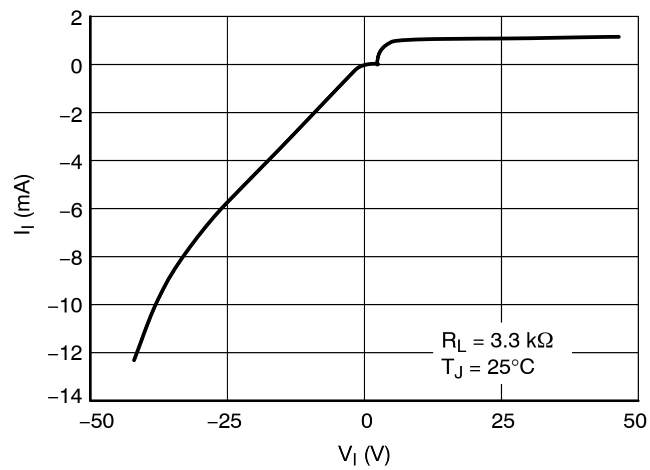


Figure 37. Input Current vs. Input Voltage

APPLICATION DESCRIPTION

Output Regulator

The output is controlled by a precision trimmed reference and error amplifier. The PNP output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Stability Considerations

The input capacitor C_{I1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{I2}.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_Q \geq 2.2\ \mu F$ and an $ESR \leq 2.5\ \Omega$ within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad \text{(eq. 1)}$$

Where:

$V_{I(max)}$ is the maximum input voltage,

$V_{Q(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application, and

I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta_{JA}} = \frac{(150\ C - T_A)}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

Where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet.

Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the **onsemi** application note AN1040/D, available on the **onsemi** Website.

ORDERING INFORMATION

Device*	Output Voltage Accuracy	Output Voltage	Package	Shipping†
NCV4274ADT50RKG	2%	5.0 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274AST33T3G	2%	3.3 V	SOT−223 (Pb−Free)	4000 / Tape & Reel

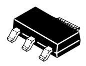
DISCONTINUED (Note 7)

NCV4274ADS33R4G	2%	3.3 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4274ADS50G	2%	5.0 V	D2PAK (Pb−Free)	50 Units / Rail
NCV4274ADS50R4G	2%	5.0 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4274DS50R4G	4%	5.0 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4274ADS85R4G	2%	8.5 V	D2PAK (Pb−Free)	800 / Tape & Reel
NCV4274DT33RKG	4%	3.3 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274DT50RKG	4%	5.0 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274AST25T3G	2%	2.5 V	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4274ADT33RKG	2%	3.3 V	DPAK (Pb−Free)	2500 / Tape & Reel
NCV4274DS50G	4%	5.0 V	D2PAK (Pb−Free)	50 Units / Rail
NCV4274ST25T3G	4%	2.5 V	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4274ST33T3G	4%	3.3 V	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

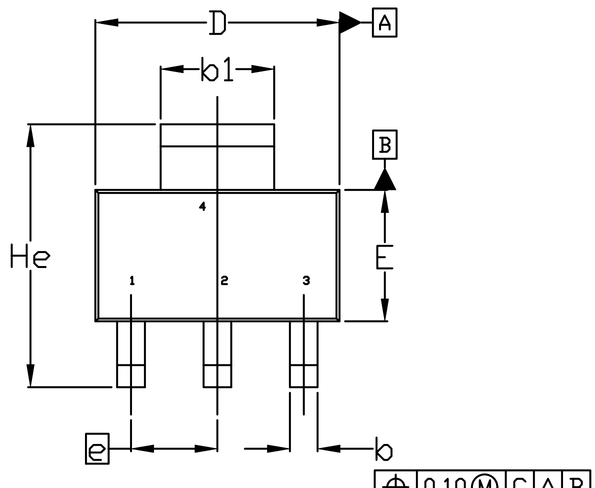
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



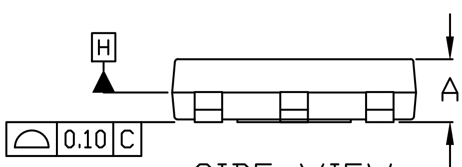
SCALE 1:1

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

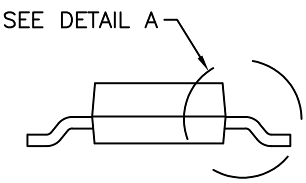
DATE 02 OCT 2018



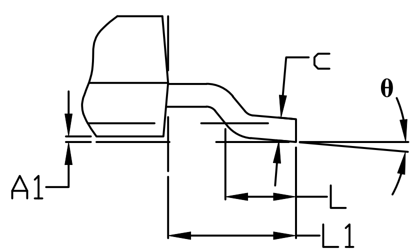
TOP VIEW



SIDE VIEW



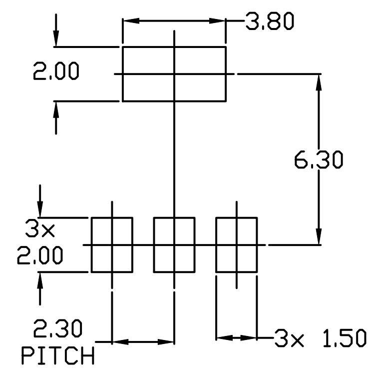
FRONT VIEW



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

DOCUMENT NUMBER:	**98ASB42680B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−223 (TO−261)**		**PAGE 1 OF 2**

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

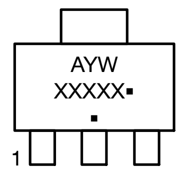
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

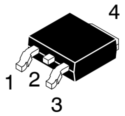
GENERIC MARKING DIAGRAM*



A	= Assembly Location
Y	= Year
W	= Work Week
XXXXX	= Specific Device Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

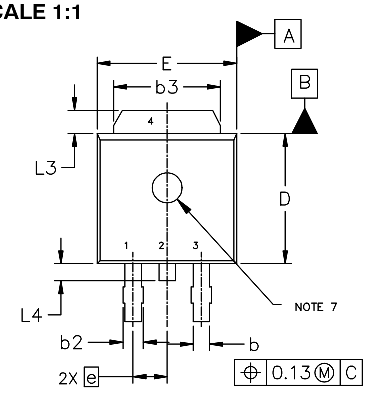
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



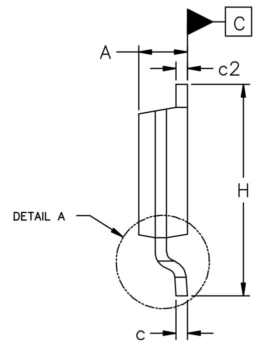
SCALE 1:1

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE H

DATE 15 JUL 2025

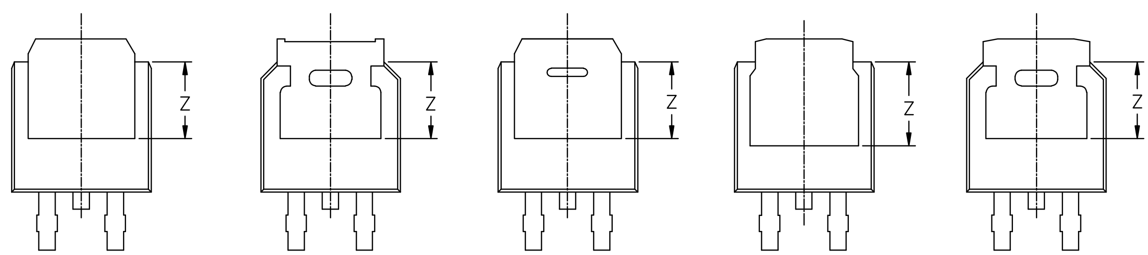


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	10.10	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

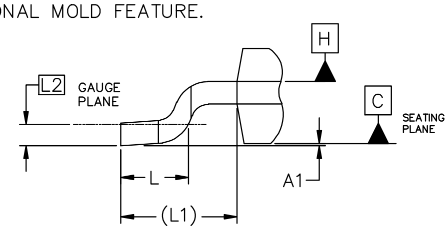


BOTTOM VIEW

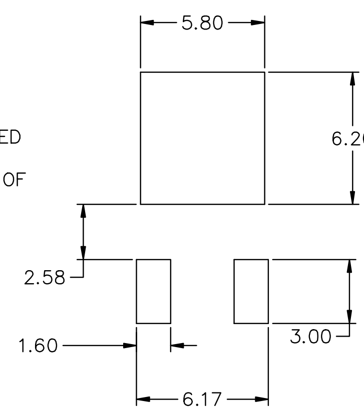
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW

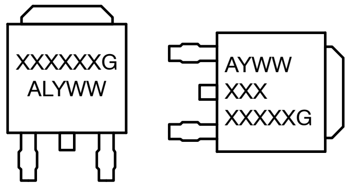


RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

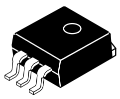
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

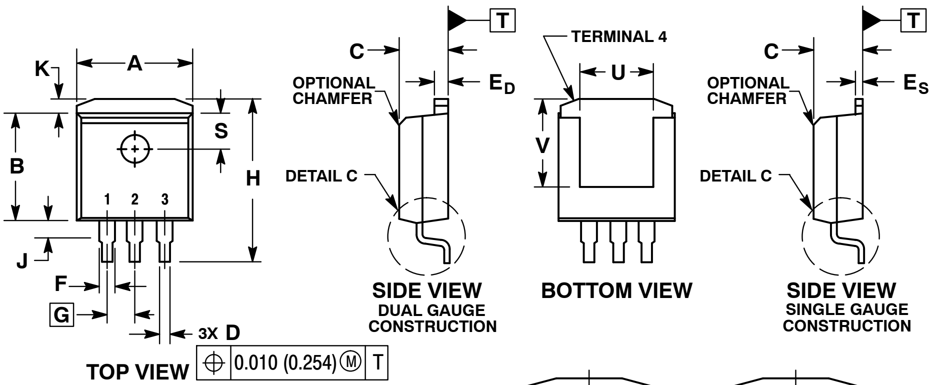
DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 2 OF 2



SCALE 1:1

D2PAK
CASE 418AF
ISSUE E

DATE 15 SEP 2015

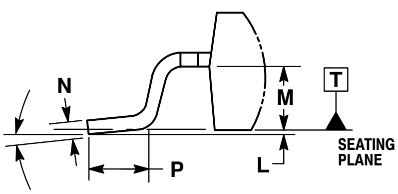


TOP VIEW

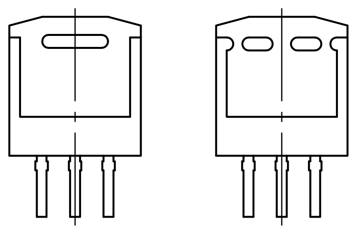
SIDE VIEW
DUAL GAUGE CONSTRUCTION

BOTTOM VIEW

SIDE VIEW
SINGLE GAUGE CONSTRUCTION



DETAIL C

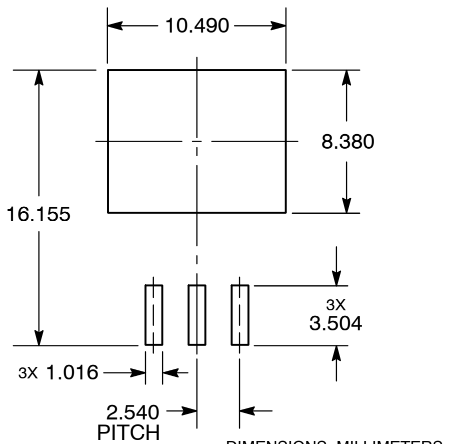


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E_D	0.045	0.055	1.143	1.397
E_S	0.018	0.026	0.457	0.660
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

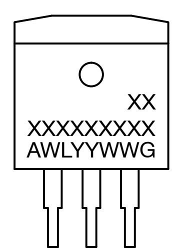
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

DOCUMENT NUMBER:	**98AON21981D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**D2PAK**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊