



SLOS340B - DECEMBER 2000 - REVISED AUGUST 2001

FAMILY OF NANOPOWER OPERATIONAL AMPLIFIERS AND PUSH-PULL COMPARATORS

FEATURES

- Micro-Power Operation . . . 1.4 μA
- Input Common-Mode Range Exceeds the Rails . . . -0.1 V to V_{CC} + 5 V
- Supply Voltage Range . . . 2.5 V to 16 V
- Rail-to-Rail Input/Output (Amplifier)
- Reverse Battery Protection Up to 18 V
- Gain Bandwidth Product . . . 5.5 kHz (Amplifier)
- Push-Pull CMOS Output Stage (Comparator)
- Specified Temperature Range
 - $-T_A = -40^{\circ}C$ to $125^{\circ}C$. . . Industrial Grade
- Ultrasmall Packaging
 - 8-Pin MSOP (TLV2702)
- Universal Op-Amp EVM (See the SLOU060 For More Information)

APPLICATIONS

- Portable Battery Monitoring
- Consumer Medical Electronics
- Security Detection Systems

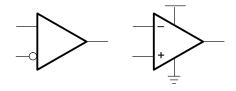
DESCRIPTION

The TLV270x combines sub-micropower operational amplifier and comparator into a single package that produces excellent micropower signal conditioning with only 1.4 μ A of supply current. This combination gives the designer more board space and reduces part counts in systems that require an operational amplifier and comparator. The low supply current makes it an ideal choice for battery powered portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an over-current condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The TLV270x's low supply current is coupled with extremely low input bias currents enabling them to be used with mega-ohm resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as $390\mu V$, CMRR of 90 dB, and minimum open loop gain of $130\ V/mV$ at $2.7\ V$.

The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V, and 15 V. The 2.5-V operation makes it compatible with Li-lon battery-powered systems and many micro-power microcontrollers available today including TI's MSP430.

All members are available in PDIP and SOIC with the duals, one op-amp and one comparator, in the small MSOP package and quads, two operational amplifiers and two comparators, in the TSSOP package.



SUPPLY CURRENT SUPPLY VOLTAGE 2.25 CC − Supply Current − µ A 1.75 1.5 1.25 QmA qO 0.75 i = V_{CC}/2 Comparator 0.5 VID = 0.25 T_A = 25°C 6 8 10 12 14 16 V_{CC} - Supply Voltage - V



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

A SELECTION OF OUTPUT COMPARATORS†

DEVICE	V _{CC} (V)	V _{IO} (μV)	ICC/Ch (μA)	GBW (kHz)	SR (V/μs)	tPLH (μs)	tpHL (μs)	t f (μ s)	RAIL-TO- RAIL	OUTPUT STAGE
TLV270x	2.5 – 16	390	1.4 [‡]	5.5	0.0025	56	83	8	I/O	PP
TLV230x	2.5 – 16	390	1.4‡	5.5	0.0025	55	30	5	I/O	OD
TLV240x	2.5 – 16	390	880	5.5	0.0025	_	_	_	I/O	_
TLV224x	2.5 – 12	600	1	5.5	0.002	_	_	_	I/O	_
TLV340x	2.5 – 16	250	0.47	_	_	55	30	5	- 1	OD
TLV370x	2.5 – 16	250	0.56	_	_	56	83	8	I	PP

[†] All specifications are typical values measured at 5 V.

TLV2702 AVAILABLE OPTIONS

		PACKAGED DEVICES						
	V _{IO} max	OMALL QUELINET	MSO	DI ACTIO DID				
ТА	AT 25°C	SMALL OUTLINE [†] (D)	MSOP [†] (DGK)	SYMBOLS	PLASTIC DIP (P)			
-40°C to 125°C	4000 μV	TLV2702ID	TLV2702IDGK	xxTIAQF	TLV2702IP			

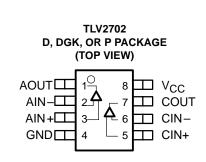
[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2702IDR).

TLV2704 AVAILABLE OPTIONS

	.,	PA	CKAGED DEVICES	
TA	V _{IO} max AT 25°C	SMALL OUTLINE [†] (D)	TSSOP (PW)	PLASTIC DIP (N)
-40°C to 125°C	4000 μV	TLV2704ID	TLV2704IPW	TLV2704IN

[†] This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2704IDR).

TLV270x PACKAGE PINOUTS



TLV2704



[‡]ICC is specified as one op-amp and one comparator.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	17 V
Differential input voltage, V _{ID}	
Input voltage range, V _I (see Notes 1 and 2)	
Input current range, I _I (any input)	±10 mA
Output current range, IO	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A : I suffix	–40°C to 125°C
Maximum junction temperature, T _J	150°C
Storage temperature range, T _{sta}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	⊝JC	[⊝] JA (°C/W)	T _A ≤ 25°C POWER RATING	T _A = 125°C POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.3	1022 mW	204.4 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

recommended operating conditions

				UNIT
Complex of the real V	Single supply	2.5	16	V
Supply voltage, V _{CC}	Split supply	±1.25	±8	V
Common-mode input voltage range, VICR	Amplifier and comparator	-0.1	V _{CC} +5	V
Operating free-air temperature, T _A		-40	125	°C



NOTES: 1. All voltage values, except differential voltages, are with respect to GND

^{2.} Input voltage range is limited to 20 V max or V_{CC} + 5 V, whichever is smaller.

electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted)

amplifier dc performance

	PARAMETER	TEST CONDIT	IONS	T _A †	MIN	TYP	MAX	UNIT
V	lanut affa at valta na			25°C		390	4000	\/
VIO	Input offset voltage	$V_O = V_{CC}/2 V$, $V_{IC} = V_{CC}/2 V$	2 V, Rs = 50Ω	Full range			6000	μV
ανιο	Offset voltage draft			25°C		3		μV/°C
			V 27V	25°C	55	73		
			V _{CC} = 2.7 V	Full range	52			
CMDD	Common mode mainsting patin	-	V _{CC} = 5 V	25°C	60	80		40
CMRR	Common-mode rejection ratio			Full range	55			dB
			V 45.V	25°C	66	90		
			V _{CC} = 15 V	Full range	60			
		$V_{CC} = 2.7 \text{ V}, V_{O(pp)} = 1.5 \text{ V}, R_L = 500 \text{ k}\Omega$		25°C	130	400		
				Full range	30			
_	Large-signal differential voltage	V 5V V 2V	D F00 L O	25°C	300	1000		l l
AVD	amplification	$V_{CC} = 5 \text{ V}, V_{O(pp)} = 3 \text{ V},$	KL = 200 K22	Full range	100			V/mV
		V 45V V 0V	D F00. 1-0	25°C	400	1800		
		$V_{CC} = 15 \text{ V}, V_{O(pp)} = 8 \text{ V},$	KL = 500 KΩ	Full range	120			
			V 071.5V	25°C	90	120		
DODE	Power supply rejection ratio		$V_{CC} = 2.7 \text{ to 5 V}$	Full range	85			40
PSRR	(ΔVCC/ΔVIO)	$V_{IC} = V_{CC}/2 V$, No load	V 545.45.V	25°C	94	120		dB
			$V_{CC} = 5 \text{ to } 15 \text{ V}$	Full range	90			

[†] Full range is -40°C to 125°C.

amplifier and comparator input characteristics

	PARAMETER	TEST CONDITIONS	T _A †	MIN	TYP	MAX	UNIT
			25°C		25	250	
liO	Input offset current		0 to 70°C			300	pА
		$V_O = V_{CC}/2 \text{ V}, V_{IC} = V_{CC}/2 \text{ V}$	Full range			700	
		$R_S = 50 \Omega$	25°C		100	500	
I _{IB}	Input bias current		0 to 70°C			550	pА
"			Full range			1700	
r _{i(d)}	Differential input resistance		25°C		300		MΩ
C _{i(c)}	Common-mode input capacitance	f = 100 kHz	25°C		3		pF

[†]Full range is -40°C to 125°C.



electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted) (continued)

amplifier output characteristics

	PARAMETER	TEST CONDITIONS		T _A †	MIN	TYP	MAX	UNIT
			\/ 07\/	25°C	2.55	2.65		
			$V_{CC} = 2.7 \text{ V}$	Full range	2.5			
V _{OH} F	Liberta and and and and and	$V_{IC} = V_{CC}/2$,	_{O/2} , _{O μA} V _{CC} = 5 V	25°C	4.85	4.95		l
	High-level output voltage	$V_{IC} = V_{CC}/2$, $I_{OH} = -50 \mu A$		Full range	4.8			V
			V _{CC} = 15 V	25°C	14.8	14.95		
				Full range	14.8			
	Landard advisors	V V (0 I	50 A	25°C		180	260	
VOL	Low-level output voltage	$V_{IC} = V_{CC}/2$, $I_{OL} = 50 \mu A$		Full range			300	mV
IO	Output current	V _O = 0.5 V from rail		25°C		±200		μΑ
ZO	Closed-loop output impedance	f = 100 Hz,	A _V = 10	25°C		1.2		kΩ

[†] Full range is -40°C to 125°C.

amplifier dynamic performance

	PARAMETER	TE	ST CONDITION	IS	TA	MIN TY	P MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 500 \text{ k}\Omega$		C _L = 100 pF	25°C	5	5	kHz
SR	Slew rate at unity gain	$V_{O(pp)} = 0.8 \text{ V},$	$R_L = 500 \text{ k}\Omega$,	C _L = 100 pF	25°C	2	5	V/ms
φМ	Phase margin	D 50010	0 400 - 5		0500	60)°	
	Gain margin	$R_L = 500 \text{ k}\Omega,$	CL = 100 pF		25°C	1	5	dB
	Settling time	V _{CC} = 2.7 or 5 V, V(STEP)PP = 1 V, A _V = -1,	$C_L = 100 \text{ pF},$ $R_L = 100 \text{ k}\Omega$	0.1%	0500	1.8	4	
t _S		V _{CC} = 15 V,		0.1%	25°C	6	1	ms
		V(STEP)PP = 1 V, $A_V = -1,$	$C_L = 100 \text{ pF},$ $R_L = 100 \text{ k}\Omega$	0.01%		3	2	
.,	Equivalent input noise	f = 0.1 to 10 Hz	f = 0.1 to 10 Hz			5	3	μV_{pp}
Vn	voltage	f = 100 Hz			25°C	50	0	nV/√ Hz
In	Equivalent input noise current	f = 100 Hz			25°C		8	fA/√Hz

supply current

PARAMETER		TEST CO	T _A †	MIN	TYP	MAX	UNIT	
			V _{CC} = 2.7 V or 5 V	25°C		1.4		
ICC	Supply current (one op-amp and one comparator)	$V_O = V_{CC}/2$	V _{CC} = 15 V	25°C		1.4	1.9	μΑ
	oomparator)			Full range			3.7	
	Reverse supply current	V _{CC} = -18 V, V _I = 0 V, V _O = open		25°C		50		nA

[†] Full range is -40°C to 125°C.



electrical characteristics at recommended operating conditions, V_{CC} = 2.7, 5 V, and 15 V (unless otherwise noted) (continued)

comparator dc performance

	PARAMETER	TEST COND	DITIONS [†]	T _A †	MIN	TYP	MAX	UNIT
.,	land Markarlana			25°C		250	5000	
VIO	Input offset voltage	$V_{IC} = V_{CC}/2$, $R_S = 50$	Ω	Full range			7000	μV
ανιο	Offset voltage drift	1		25°C		3		μV/°C
		V_{IC} = 0 to V_{CC} , R_S = 50 Ω	V _{CC} = 2.7 V	25°C	55	72		
	Common-mode rejection ratio			Full range	50			dB
OMBB			V _{CC} = 5 V	25°C	60	76		
CMRR				Full range	55			
			V 45 V	25°C	65	88		
			V _{CC} = 15 V	Full range	60			
AVD	Large-signal differential voltage amplification			25°C		1000		V/mV
			V 071-5V	25°C	75	100		
PSRR	Power supply rejection ratio	$V_{IC} = V_{CC}/2 V$	$V_{CC} = 2.7 \text{ to } 5 \text{ V}$	Full range	70			dB
FORK	(ΔV _{CC} /ΔV _{IO})	No load	V _{CC} = 5 to 15 V	25°C	85	105		ub
				Full range	80			

[†]Full range is -40°C to 125°C.

comparator output characteristics

PARAMETER		TEST CONDITIONS†	T _A †	MIN	TYP	MAX	UNIT	
r _{i(d)}	Differential input resistance		25°C		300		MΩ	
.,	LPak laval autout valta va	$V_{IC} = V_{CC}/2$, $I_{OL} = -50 \mu\text{A}$,	25°C	V _{CC} -320			.,	
VOH	High-level output voltage	V _{ID} = 1 V	Full range	V _{CC} -450			mV	
Vai	Low lovel output voltage	$V_{IC} = V_{CC}/2$, $I_{OL} = 50 \mu\text{A}$,	25°C		80	200	mV	
VOL	Low-level output voltage	$V_{ID} = -1 V$	Full range			300	IIIV	

[†]Full range is -40°C to 125°C.

switching characteristics at recommended operating conditions, V_{CC} = 2.7 V, 5 V, 15 V (unless otherwise noted)

	PARAMETER	TEST CO	TA	MIN	TYP	MAX	UNIT			
^t (PLH)			Overdrive = 2 mV			240				
	Propagation response time, low-to- high-level output	f = 10 kHz.	Overdrive = 10 mV	25°C		64				
	riigir iever output	VSTEP = 100 mV,	Overdrive = 50 mV			36				
		C _L = 10 pF,	Overdrive = 2 mV			167		μs		
t(PHL)	Propagation response time, high-to- low-level output	$V_{CC} = 2.7 \text{ V}$	Overdrive = 10 mV	25°C		67				
(low-level output		Overdrive = 50 mV			37				
t _r	Rise time	C _L = 10 pF,	V _{CC} = 2.7 V	25°C		7		μs		
tf	Fall time	C _L = 10 pF,	V _{CC} = 2.7 V	25°C		9		μs		

NOTE: The propagation response time specified is the interval between the input step function and the instant when the output crosses 1.4 V. Propagation responses are longer at higher supply voltages, refer to Figure 18 through Figure 36 for further details.



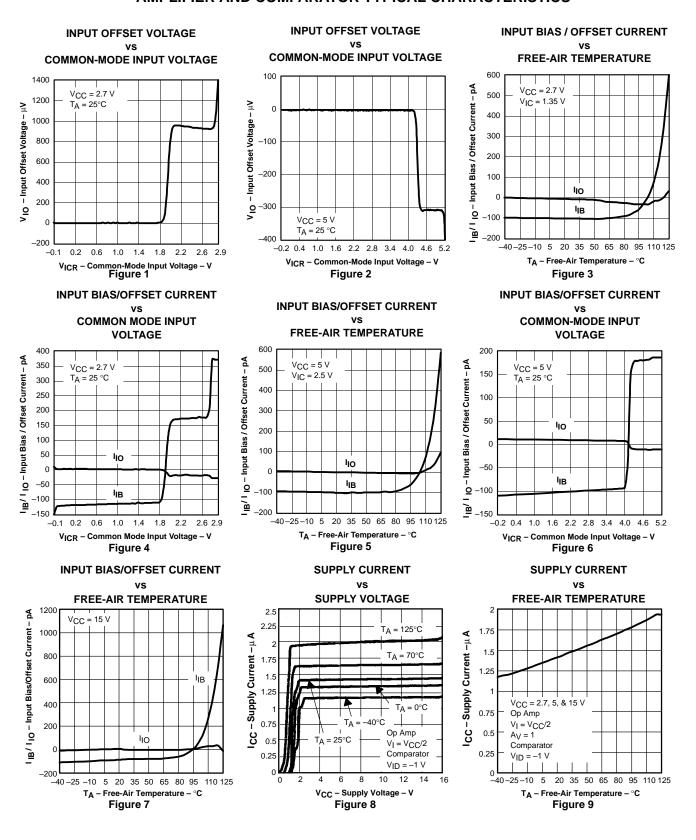
TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
VIO	Input offset voltage	vs Common-mode input voltage	1, 2
	land bin amount	vs Free-air temperature	3, 5, 7
lв	Input bias current	vs Common-mode input voltage	4, 6
	land effect comment	vs Free-air temperature	3, 5, 7
lio	Input offset current	vs Common-mode input voltage	4, 6
		vs Supply voltage	8
ICC	Supply current	vs Free-air temperature	9
Amplifier			
CMRR	Common-mode rejection ratio	vs Frequency	10
Voн	High-level output voltage	vs High-level output current	11, 13
VOL	Low-level output voltage	vs Low-level output current	12, 14
VO(PP)	Output voltage, peak-to-peak	vs Frequency	15
PSRR	Power supply rejection ratio	vs Frequency	16
	Voltage noise over a 10 Second Period		17
фm	Phase margin	vs Capacitive load	18
A_{VD}	Differential voltage gain	vs Frequency	19
	Phase	vs Frequency	19
	Gain-bandwidth product	vs Supply voltage	20
SR	Slew rate	vs Free-air temperature	21
	Large-signal follower pulse response		22
	Small-signal follower pulse response		23
	Large-signal inverting pulse response		24
	Small-signal inverting pulse response		25
Comparator		•	
Vон	High-level output voltage	vs High-level output current	26, 28
VOL	Low-level output voltage	vs Low-level output current	27, 29
	Output rise/fall time	vs Supply voltage	30
	Low-to-high level output response for various input overdrives		31, 33, 35
	High-to-low level output response for various input overdrives		32, 34, 36



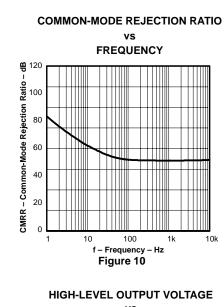
AMPLIFIER AND COMPARATOR TYPICAL CHARACTERISTICS

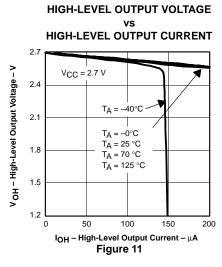


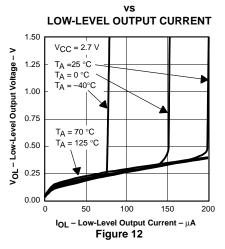


LOW-LEVEL OUTPUT VOLTAGE

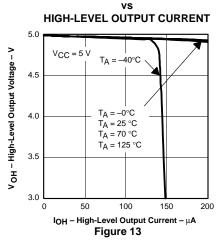
AMPLIFIER TYPICAL CHARACTERISTICS

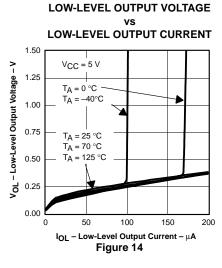


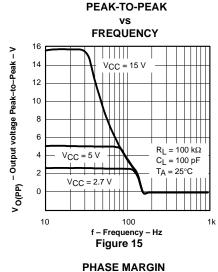


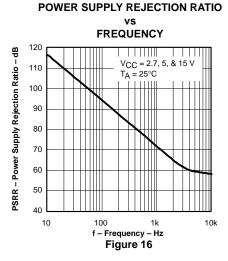


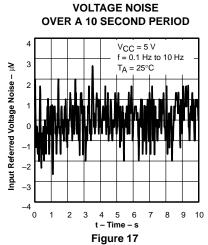
OUTPUT VOLTAGE

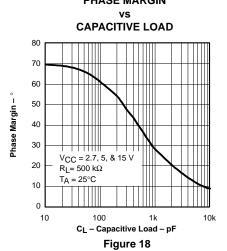






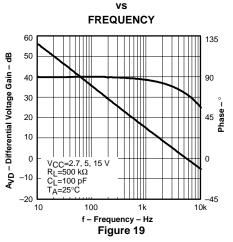


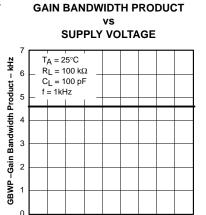




AMPLIFIER TYPICAL CHARACTERISTICS



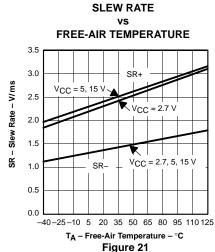




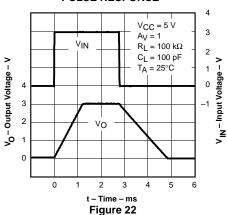
2.5 4.0 5.5 7.0 8.5 10.0 11.5 13.0 14.5 16.0

V_{CC} - Supply Voltage -V

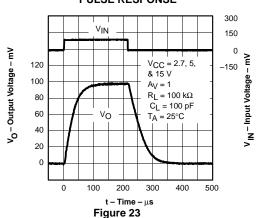
Figure 20



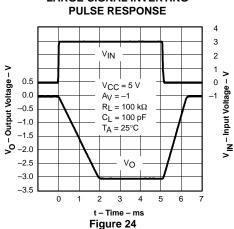
LARGE-SIGNAL FOLLOWER PULSE RESPONSE



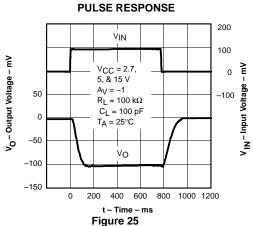
SMALL-SIGNAL FOLLOWER PULSE RESPONSE



LARGE-SIGNAL INVERTING

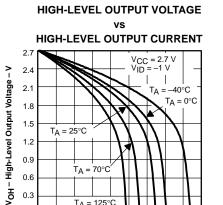


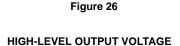
SMALL-SIGNAL INVERTING





COMPARATOR TYPICAL CHARACTERISTICS





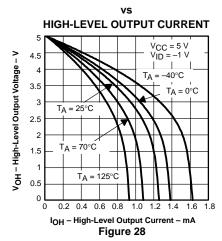
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IOH - High-Level Output Current - mA

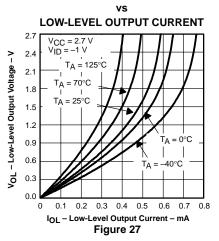
T_A = 125°C

0.3

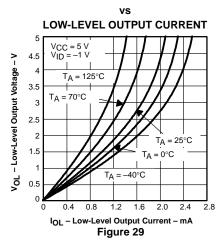
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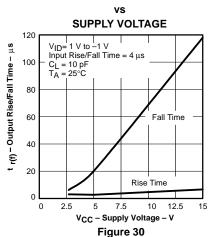
LOW-LEVEL OUTPUT VOLTAGE



LOW-LEVEL OUTPUT VOLTAGE



OUTPUT RISE/FALL TIME



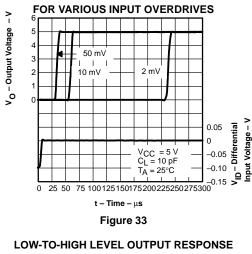


TYPICAL CHARACTERISTICS

LOW-TO-HIGH OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES V_O - Output Voltage - V 3 2.7 2.4 2.1 1.8 1.5 1.2 0.9 0.6 0.3 50 mV 2 mV 10 mV 0.05 V_{ID}- Differential nput Voltage - V 0 -0.05 V_{CC} = 2.7 V C_L = 10 pF -0.10 T_A = 25°C -0.15 25 50 75 100125150175200225250275300 $\textbf{t-Time}-\mu\textbf{s}$

Figure 31

LOW-TO-HIGH LEVEL OUTPUT RESPONSE



LOW-TO-HIGH LEVEL OUTPUT RESPONSE

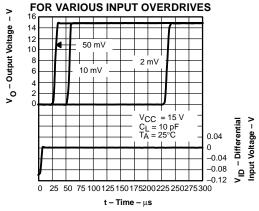


Figure 35

HIGH-TO-LOW LEVEL OUTPUT RESPONSE

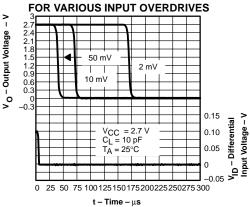


Figure 32

HIGH-TO-LOW LEVEL OUTPUT RESPONSE

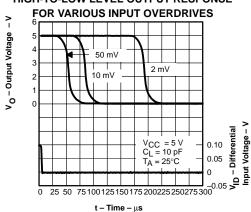


Figure 34

HIGH-TO-LOW LEVEL OUTPUT RESPONSE

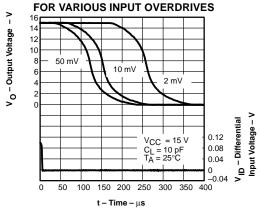


Figure 36



reverse battery protection

The TLV2702/4 are protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of 6 Schottky diodes and will therefore increase as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure will turn on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

common-mode input range

The TLV2702/4 has rail-rail input and outputs. For common-mode inputs from -0.1 V to $\text{V}_{\text{CC}} - 0.8 \text{ V}$ a PNP differential pair will provide the gain.

For inputs between V_{CC} – 0.8 V and V_{CC} , two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails; because as the inputs go above V_{CC} , the NPNs switch from functioning as transistors to functioning as diodes. This will lead to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC} .

The TLV2702/4 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain will be observed with the ultimate possibility of phase inversion.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage.

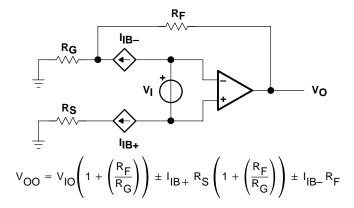


Figure 37. Output Offset Voltage Model



general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 38).

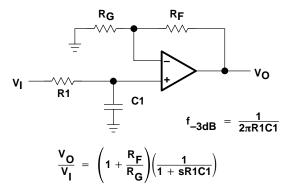


Figure 38. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

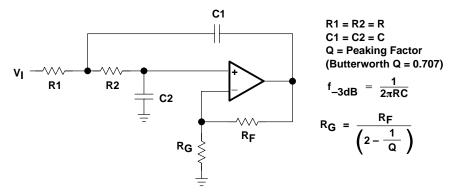


Figure 39. 2-Pole Low-Pass Sallen-Key Filter



circuit layout considerations

To achieve the levels of high performance of the TLV270x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all
 components with a low inductive ground connection. However, in the areas of the amplifier inputs and
 output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins
 will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board
 is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high
 performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of
 surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small
 size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray
 inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be
 kept as short as possible.



general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 40 and is calculated by the following formula:

$$P_{D} = \left(\frac{T_{MAX} - T_{A}}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV270x IC (watts)

 T_{MAX} = Absolute maximum junction temperature (150°C)

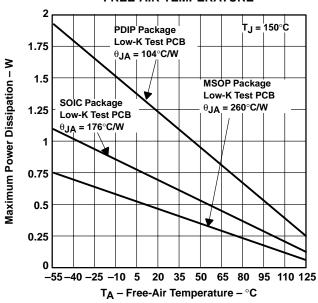
T_A = Free-ambient air temperature (°C)

 $\theta_{JA} = \theta_{JC} + \theta_{CA}$

 θ_{JC} = Thermal coefficient from junction to case

 θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

MAXIMUM POWER DISSIPATION vs FREE-AIR TEMPERATURE



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 40. Maximum Power Dissipation vs Free-Air Temperature



amplifier macromodel information

Macromodel information provided was derived using Microsim $Parts^{TM}$ Release 8, the model generation software used with Microsim $PSpice^{TM}$. The Boyle macromodel (see Note 2) and subcircuit in Figure 41 are generated using the TLV270x typical electrical and operating characteristics at $T_A = 25^{\circ}C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 3: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

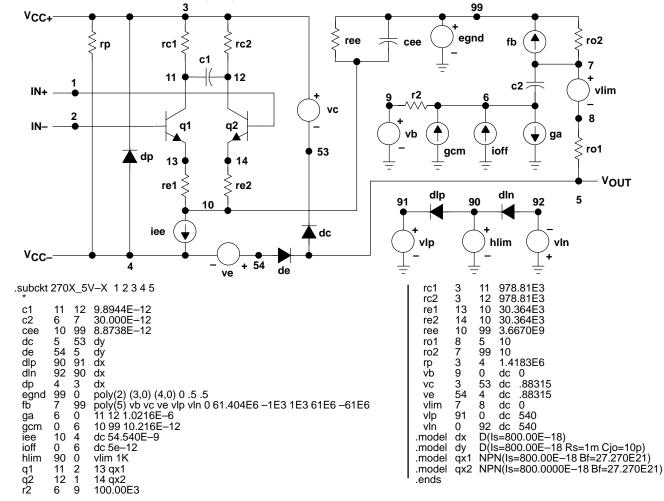


Figure 41. Boyle Macromodels and Subcircuit

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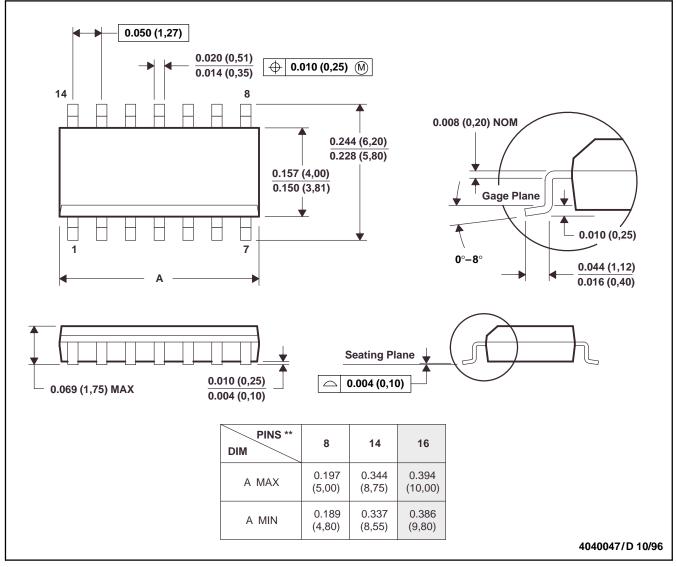


MECHANICAL DATA

D (R-PDSO-G**)

14 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

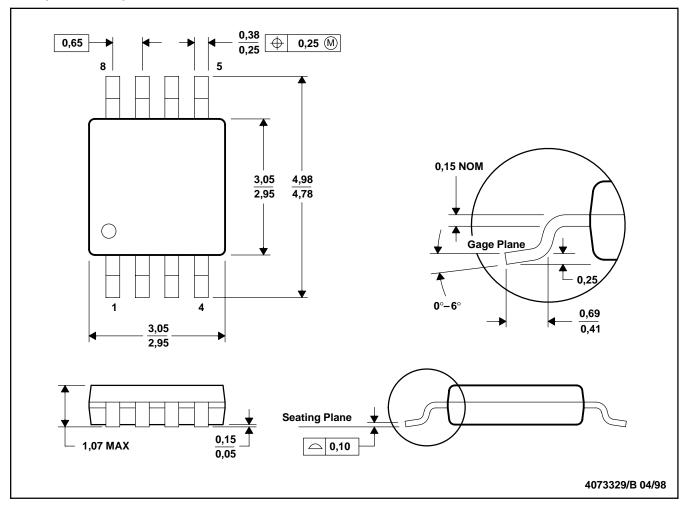
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).



DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

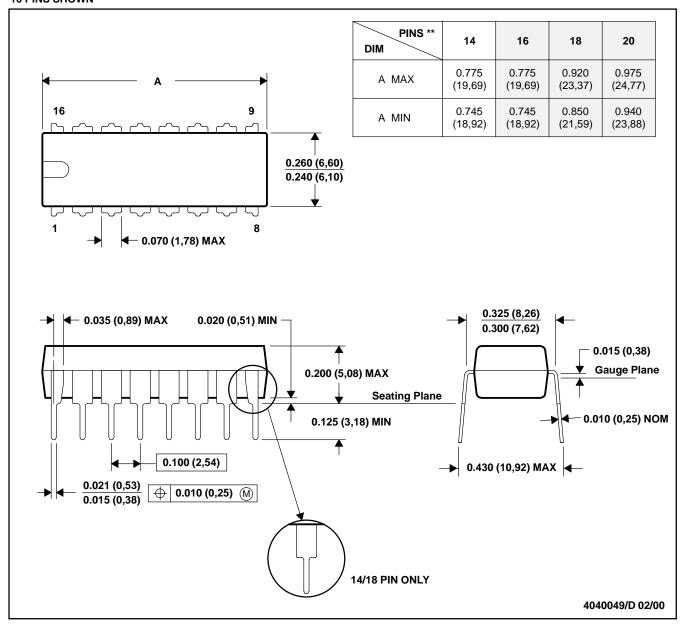
B. This drawing is subject to change without notice.C. Body dimensions do not include mold flash or protrusion.

D. Falls within JEDEC MO-187

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



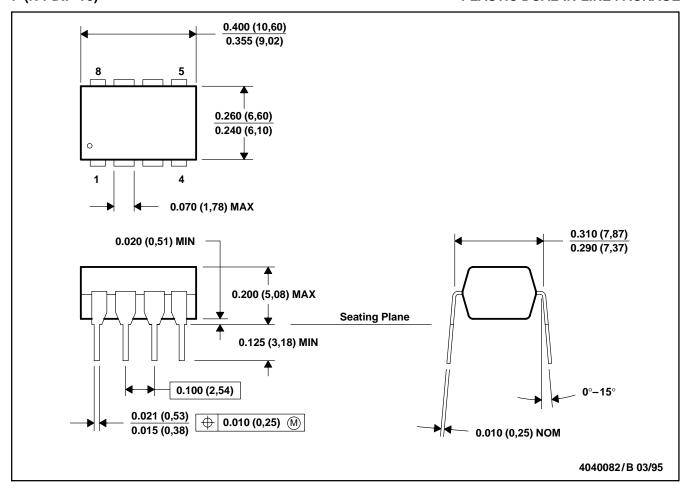
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



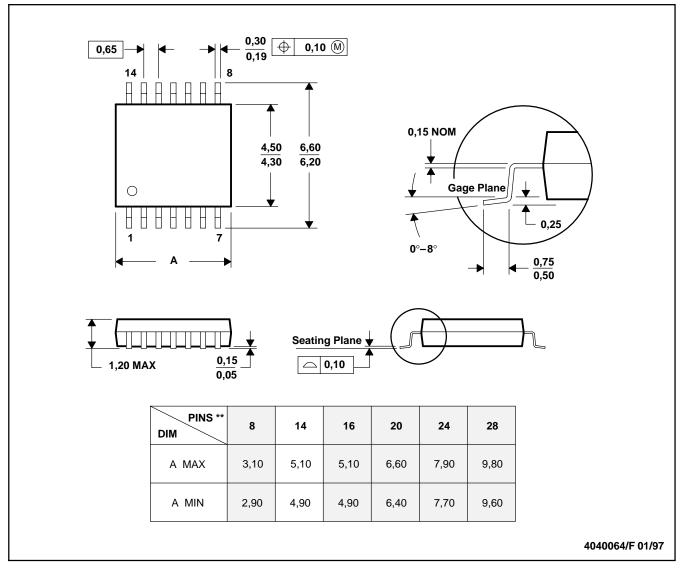
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153







com 17-Jun-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2702ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2702IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2702IDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2702IDGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2702IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2702IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2702IP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2702IPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2704ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2704IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

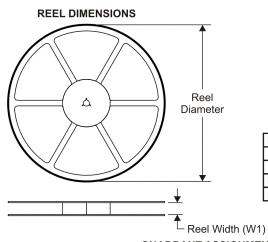
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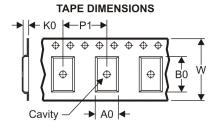
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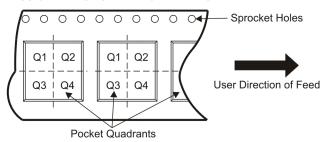
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

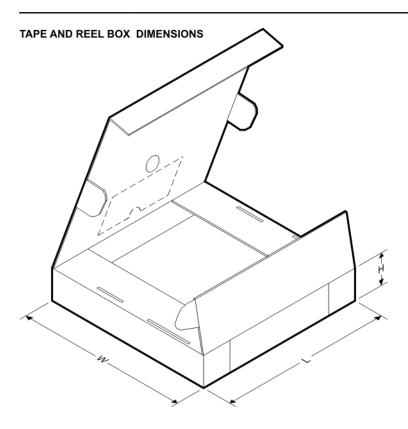
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2702IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2702IDGKR	MSOP	DGK	8	2500	358.0	335.0	35.0

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