19-3498; Rev 0; 11/04

EVALUATION KIT AVAILABLE

Simplified Multichemistry SMBus Battery Charger

MAX8713

General Description

The MAX8713 multichemistry battery charger simplifies construction of smart chargers with a minimum number of external components. It uses the Intel System Management Bus (SMBus™) to control the charge voltage and charge current. High efficiency is achieved through the use of a constant off-time step-down topology with synchronous rectification.

The MAX8713 charges one to four lithium-ion (Li+) cells in series and delivers over 2A charge current—scalable with the sense resistor. The MAX8713 drives n-channel MOSFETs for improved efficiency and reduced cost. A low-offset charge-current-sense amplifier provides high-accuracy charge current with small sense resistors.

The MAX8713 is available in a space-saving 24-pin 4mm x 4mm thin QFN package and operates over the extended (-40°C to +85°C) temperature range. An evaluation kit is available to reduce design time.

Applications

Handset Car Kits

Digital Cameras

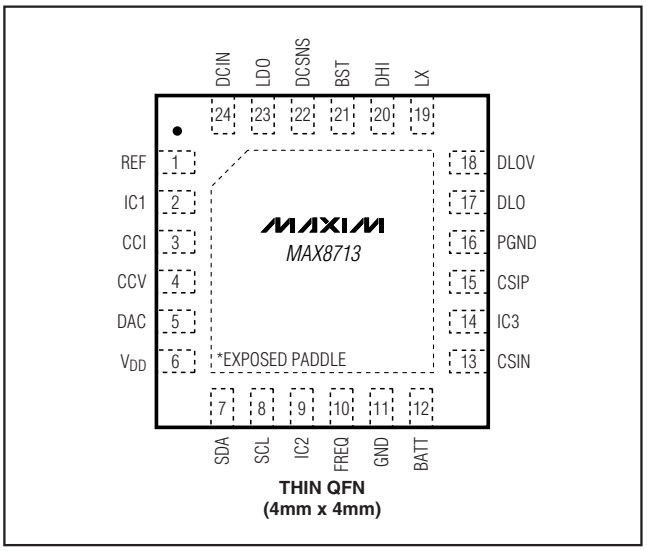
PDAs and Tablet Computers

Notebook Computers

Portable Equipment with Rechargeable Batteries

SMBus is a trademark of Intel Corp.

Pin Configuration



THIN QFN
(4mm x 4mm)

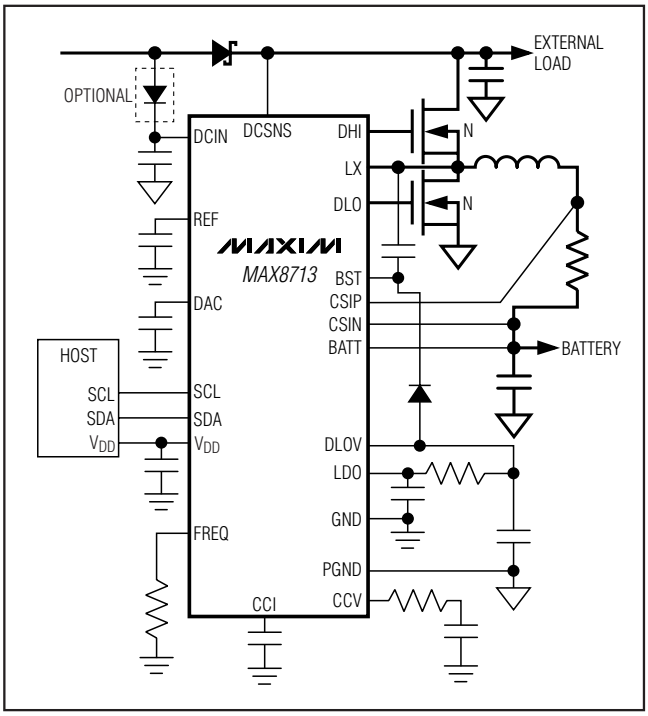
Features

- ♦ Over 2A Charge Current
- ♦ Intel SMBus 2-Wire Serial Interface
- ♦ ±0.6% Charge Voltage Accuracy
- ♦ 11-Bit Charge Voltage Resolution
- ♦ 6-Bit Charge Current Resolution
- ♦ Adjustable Switching Frequency
- ♦ +8V to +28V Input Voltage Range
- ♦ Cycle-By-Cycle Current Limit
- ♦ Charges Any Battery Chemistry (Li+, NiCd, NiMH, Lead Acid, etc.)
- ♦ Small 24-Pin TQFN

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8713ETG	-40°C to +85°C	24 Thin QFN 4mm x 4mm

Typical Operating Circuit



Simplified Multichemistry SMBus Battery Charger

ABSOLUTE MAXIMUM RATINGS

V_{DCSNS}, V_{DCIN} to GND .....-0.3V to +30V
V_{BST} to GND .....-0.3V to +36V
V_{BST} to LX .....-0.3V to +6V
V_{DHI} to LX.....-0.3V to (V_{BST} + 0.3V)
V_{LX} to GND.....-6V to +30V
V_{DHI} to GND .....-6V to +36V
V_{BATT}, V_{CSIN} to GND .....-0.3V to +20V
V_{CSIP} to V_{CSIN} .....-0.3V to +0.3V
PGND to GND .....-0.3V to +0.3V
V_{CCI}, V_{CCV}, V_{DAC}, V_{REF} to GND .....-0.3V to (V_{LDO} + 0.3V)
V_{DLOV}, V_{LDO}, V_{DD}, V_{SCL}, V_{SDA}, V_{FREQ} to GND .....-0.3V to +6V
V_{DLO} to PGND .....-0.3V to (V_{DLOV} + 0.3V)
LDO Short-Circuit Current.....25mA
Continuous Power Dissipation (T_A = +70°C)
24-Pin Thin QFN 4mm x 4mm (derate 20.8mW/°C above +70°C).....1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{DCSNS} = 12V, V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BST} = V_{LX} = 8.4V, GND = PGND = 0, LDO = DLOV, C_{REF} = C_{LDO} = C_{DLOV} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V. Pins CCI and CCV are compensated per Figure 1. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE VOLTAGE REGULATION					
Battery Regulation Voltage Accuracy	ChargingVoltage() = 0x20D0	-0.6		+0.6	%
	ChargingVoltage() = 0x1060	-1.0		+1.0	
	ChargingVoltage() = 0x41A0 and 0x3130	-0.8		+0.8	
Battery Full Charge Voltage	ChargingVoltage() = 0x41A0, V_{DCIN} = 19V	16.668	16.8	16.934	V
	ChargingVoltage() = 0x3130, V_{DCIN} = 19V	12.491	12.592	12.693	
	ChargingVoltage() = 0x20D0, V_{DCIN} = 12V	8.439	8.4	8.442	
	ChargingVoltage() = 0x1060, V_{DCIN} = 12V	4.150	4.192	4.234	
CHARGE CURRENT REGULATION					
CSIP to CSIN Full-Scale Current-Sense Voltage	V_{BATT} = 8.4V, V_{DCIN} = 12V	78.22	80.64	88.05	mV
Compliance Current Accuracy	ChargingCurrent() = 0x07e0	-3		+3	%
	ChargingCurrent() = 0x03e0	-5		+5	
Battery Charge Current-Sense Voltage	ChargingCurrent() = 0x07e0	78.22	80.64	83.05	mV
	ChargingCurrent() = 0x03e0	37.68	39.68	41.68	
	ChargingCurrent() = 0x0180	13.82	15.36	16.88	
	ChargingCurrent() = 0x0020		1.28		
BATT/CSIP/CSIN Input Voltage Range		0		19	V
CSIP/CSIN Input Current	V_{DCIN} = 0 or charger not switching		0.1	1	µA
	V_{CSIP} = V_{CSIN} = 19V			700	µA
SUPPLY AND LINEAR REGULATOR					
DCIN Input Voltage Range		7.5		28.0	V
DCSNS Input Voltage Range		7.5		28.0	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{DCSNS} = 12V, V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BST} = V_{LX} = 8.4V, GND = PGND = 0, LDO = DLOV, C_{REF} = C_{LDO} = C_{DLOV} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V. Pins CCI and CCV are compensated per Figure 1. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
DCIN Undervoltage-Lockout Trip Point	DCIN falling			6.5	7		V
	DCIN rising				7	7.5	
DCIN Quiescent Current	7.5V < V_{DCIN} < 28V				2.7	6	mA
DCSNS Quiescent Current	7.5V < V_{DCSNS} < 28V				200	300	µA
BATT Input Current	V_{BATT} = 19V, V_{DCIN} = 0 or charger not switching				0.1	1	µA
	V_{BATT} = 2V to 19V, V_{DCIN} > V_{BATT} + 0.3V				200	500	
LDO Output Voltage	7.5V < V_{DCIN} < 28V, no load			5.25	5.4	5.55	V
LDO Load Regulation	0 < I_{LDO} < 5mA				34	100	mV
LDO Undervoltage-Lockout Trip Point	V_{DCIN} = 7.5V			3.20	4	5.15	V
VDD Range				2.7		5.5	V
VDD UVLO Rising					2.5	2.7	V
VDD UVLO Hysteresis					100		mV
VDD Quiescent Current	V_{DCIN} < 6V, V_{DD} = 5.5V, V_{SCL} = V_{SDA} = 5.5V					27	µA
REFERENCE							
REF Output Voltage	0 < I_{REF} < 500µA			4.067	4.096	4.125	V
REF Undervoltage-Lockout Trip Point	REF falling				3.1	3.9	V
TRIP POINTS							
BATT POWER_FAIL Threshold	V_{DCSNS} falling			50	100	150	mV
BATT POWER_FAIL Threshold Hysteresis				50	200	400	mV
SWITCHING REGULATOR							
Off-Time	V_{BST} - V_{LX} = 4.5V	V_{BATT} = 8.4V	R_{FREQ} = 100kΩ	675	750	825	ns
			R_{FREQ} = 400kΩ	2700	3000	3300	
		V_{BATT} = 11V	R_{FREQ} = 100kΩ	370	410	450	
			R_{FREQ} = 400kΩ	1476	1640	1804	
DLOV Supply Current	Charger not switching				5	10	µA
BST Supply Current	DHI high				6	15	µA
BST Input Quiescent Current	V_{DCIN} = 0V, V_{BST} = 23.5V, V_{BATT} = V_{LX} = 19V				0.3	1	µA
LX Input Bias Current	V_{DCIN} = 28V, V_{BATT} = V_{LX} = 19V				150	500	µA
Maximum Discontinuous-Mode Peak Current					0.125		A
DHI On-Resistance High	V_{BST} =12.9V, V_{BATT} = 8.4V, V_{DCSNS} = 12, DHI = V_{LX}; I_{DHI} = -10mA				7	14	Ω
DHI On-Resistance Low	V_{BST} =12.9V, V_{BATT} = 8.4V, V_{CSNS} = 12, DHI = V_{BST}; I_{DHI} = +100mA				2	4	Ω
DLO On-Resistance High	V_{DLOV} = 4.5V, I_{DLO} = -10mA				7	14	Ω
DLO On-Resistance Low	V_{DLOV} = 4.5V, I_{DLO} = +100mA				2	4	Ω
ERROR AMPLIFIERS							
GMV Amplifier Transconductance	ChargingVoltage() = 0x20d0, V_{BATT} = 8.400V			0.0625	0.125	0.2500	mA/V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{DCSNS} = 12V, V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BST} = V_{LX} = 8.4V, GND = PGND = 0, LDO = DLOV, C_{REF} = C_{LDO} = C_{DLOV} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V. Pins CCI and CCV are compensated per Figure 1. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GMI Amplifier Transconductance	ChargingCurrent() = 0x03e0, V_{CSIP} - V_{CSIN} = 39.68mV	0.5	1	2.0	mA/V
CCI/CCV Clamp Voltage	0.25V < $V_{CCV/I}$ < 2.0V	150	300	600	mV
SMBus INTERFACE LEVEL SPECIFICATIONS					
SDA/SCL Input Low Voltage	V_{DD} = 2.7V to 5.5V			0.8	V
SDA/SCL Input High Voltage	V_{DD} = 2.7V to 5.5V	2.1			V
SDA/SCL Input Bias Current	V_{DD} = 2.7V to 5.5V	-1		+1	µA
SDA, Output Sink Current	$V_{(SDA)}$ = 0.4V	6			mA

TIMING CHARACTERISTICS

(V_{DCIN} = V_{DCSNS} = 12V, V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BST} = V_{LX} = 8.4V, GND = PGND = 0, LDO = DLOV, C_{REF} = C_{LDO} = C_{DLOV} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V. Pins CCI and CCV are compensated per Figure 1. **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus TIMING SPECIFICATION (V_{DD} = 2.7V TO 5.5V) (Figures 6 and 7)						
SMBus Frequency	f_{SMB}		10		100	kHz
Bus Free Time	t_{BUF}		4.7			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
Stop Condition Setup Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Timeout	$t_{TIMEOUT}$	(Note 1)	25		35	ms
SCL Low Period	t_{LOW}		4.7			µs
SCL High Period	t_{HIGH}		4			µs
Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$	(Note 2)			25	ms

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = V_{DCSNS} = 12V, V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BST} = V_{LX} = 8.4V, GND = PGND = 0, LDO = DLOV, C_{REF} = C_{LDO} = C_{DLOV} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V. Pins CCI and CCV are compensated per Figure 1. **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE VOLTAGE REGULATION					
Battery Regulation Voltage Accuracy	ChargingVoltage() = 0x20D0	-1.0		+1.0	%
	ChargingVoltage() = 0x1060	-1.5		+1.5	
	ChargingVoltage() = 0x41A0 and 0x3130	-1.2		+1.2	
Battery Full Charge Voltage	ChargingVoltage() = 0x41A0, V_{DCIN} = 19V	16.598		17.002	V
	ChargingVoltage() = 0x3130, V_{DCIN} = 19V	12.441		12.743	
	ChargingVoltage() = 0x20D0, V_{DCIN} = 12V	8.312		8.484	
	ChargingVoltage() = 0x1060, V_{DCIN} = 12V	4.124		4.253	
CHARGE CURRENT REGULATION					
CSIP to CSIN Full-Scale Current-Sense Voltage	V_{BATT} = 8.4V, V_{DCIN} = 12V	78.22		83.05	mV
Compliance Current Accuracy	ChargingCurrent() = 0x07e0	-3		+3	%
	ChargingCurrent() = 0x03e0	-5		+5	
Battery Charge Current-Sense Voltage	ChargingCurrent() = 0x07e0	78.22		83.05	mV
	ChargingCurrent() = 0x03e0	37.68		41.68	
	ChargingCurrent() = 0x0180	13.056		17.664	
BATT/CSIP/CSIN Input Voltage Range		0		19	V
CSIP/CSIN Input Current	V_{DCIN} = 0 or charger not switching			1	µA
	V_{CSIP} = V_{CSIN} = 19V			700	µA
SUPPLY AND LINEAR REGULATOR					
DCIN Input Voltage Range		7.5		28.0	V
DCSNS Input Voltage Range		7.5		28.0	V
DCIN Undervoltage-Lockout Trip Point	DCIN falling	6.5			V
	DCIN rising			7.5	
DCIN Quiescent Current	7.5V < V_{DCIN} < 28V			6	mA
DCSNS Quiescent Current	7.5V < V_{DCSNS} < 28V			300	µA
BATT Input Current	V_{BATT} = 19V, V_{DCIN} = 0 or charger not switching			1	µA
	V_{BATT} = 2V to 19V, V_{DCIN} > V_{BATT} + 0.3V			500	
LDO Output Voltage	7.5V < V_{DCIN} < 28V, no load	5.25		5.55	V
LDO Load Regulation	0 < I_{LDO} < 5mA			100	mV
LDO Undervoltage-Lockout Trip Point	V_{DCIN} = 7.5V	3.20		5.15	V
VDD Range		2.7		5.5	V
VDD UVLO Rising				2.7	V
VDD Quiescent Current	V_{DCIN} < 6V, V_{DD} = 5.5V, V_{SCL} = V_{SDA} = 5.5V			27	µA
REFERENCE					
REF Output Voltage	0 < I_{REF} < 500µA	4.053		4.133	V
REF Undervoltage-Lockout Trip Point	REF falling			3.9	V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = V_{DCSNS} = 12V, V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BST} = V_{LX} = 8.4V, GND = PGND = 0, LDO = DLOV, C_{REF} = C_{LDO} = C_{DLOV} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V. Pins CCI and CCV are compensated per Figure 1. **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
TRIP POINTS							
BATT POWER_FAIL Threshold	V_{DCSNS} falling			50		150	mV
BATT POWER_FAIL Threshold Hysteresis				50		400	mV
SWITCHING REGULATOR							
Off-Time	V_{BST} - V_{LX} = 4.5V	V_{BATT} = 8.4V	R_{FREQ} = 100kΩ	637		862	ns
			R_{FREQ} = 400kΩ	2550		3450	
		V_{BATT} = 11V	R_{FREQ} = 100kΩ	350		470	
			R_{FREQ} = 400kΩ	1394		1866	
DLOV Supply Current	Charger not switching					10	µA
BST Supply Current	DHI high					15	µA
BST Input Quiescent Current	V_{DCIN} = 0V, V_{BST} = 23.5V, V_{BATT} = V_{LX} = 19V					1	µA
LX Input Bias Current	V_{DCIN} = 28V, V_{BATT} = V_{LX} = 19V					500	µA
DHI On-Resistance High	V_{BST} =12.9V, V_{BATT} = 8.4V, V_{DCSNS} = 12, DHI= V_{LX}; I_{DHI} = -10mA					14	Ω
DHI On-Resistance Low	V_{BST} =12.9V, V_{BATT} = 8.4V, V_{CSNS} = 12, DHI = V_{BST}; I_{DHI} = +100mA					4	Ω
DLO On-Resistance High	V_{DLOV} = 4.5V, I_{DLO} = -10mA					14	Ω
DLO On-Resistance Low	V_{DLOV} = 4.5V, I_{DLO} = +100mA					4	Ω
ERROR AMPLIFIERS							
GMV Amplifier Transconductance	ChargingVoltage() = 0x20d0, V_{BATT} = 8.384V			0.0625		0.2500	mA/V
GMI Amplifier Transconductance	ChargingCurrent() = 0x03e0, V_{CSIP} - V_{CSIN} = 39.68mV			0.5		2.0	mA/V
CCI/CCV Clamp Voltage	0.25V < $V_{CCV/I}$ < 2.0V			130		600	mV
SMBus INTERFACE LEVEL SPECIFICATIONS							
SDA/SCL Input Low Voltage	V_{DD} = 2.7V to 5.5V					0.8	V
SDA/SCL Input High Voltage	V_{DD} = 2.7V to 5.5V			2.2			V
SDA/SCL Input Bias Current	V_{DD} = 2.7V to 5.5V			-1		+1	µA
SDA, Output Sink Current	$V_{(SDA)}$ = 0.4V			6			mA

TIMING CHARACTERISTICS

(V_{DCIN} = V_{DCSNS} = 12V, V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BST} = V_{LX} = 8.4V, GND = PGND = 0, LDO = DLOV, C_{REF} = C_{LDO} = C_{DLOV} = 1µF, C_{DAC} = 0.1µF , V_{DD} = 3.3V. Pins CCI and CCV are compensated per Figure 1. **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus TIMING SPECIFICATION (V_{DD} = 2.7V TO 5.5V) (Figures 6 and 7)						
SMBus Frequency	f_{SMB}		10		100	kHz
Bus Free Time	t_{BUF}		4.7			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
Stop Condition Setup Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Timeout	$t_{TIMEOUT}$	(Note 1)	25		35	ms
SCL Low Period	t_{LOW}		4.7			µs
SCL High Period	t_{HIGH}		4			µs
Cumulative Clock Low Extend Time	$t_{LOW:SEXT}$	(Note 2)			25	ms

Note 1: Devices participating in a transfer timeout when any clock low exceeds the $t_{TIMEOUT:MIN}$ value of 25ms. Devices that have detected a timeout condition must reset the communication no later than $t_{TIMEOUT:MAX}$ of 35ms. The maximum value specified must be adhered to by both a master and a slave as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).

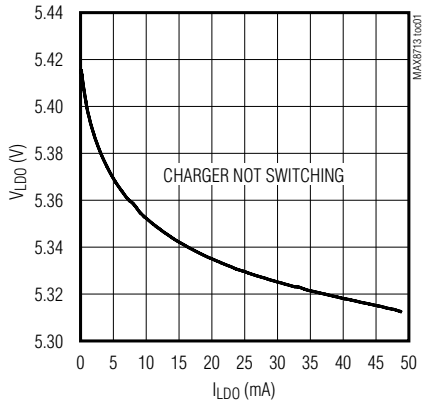
Note 2: $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.

Note 3: Specifications to -40°C are guaranteed by design and not production tested.

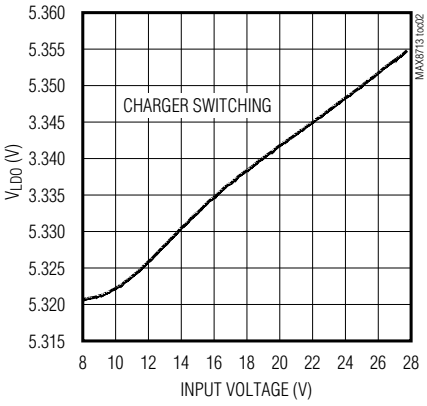
Typical Operating Characteristics

(V_{DCIN} = V_{DCSNS} = 20V, Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

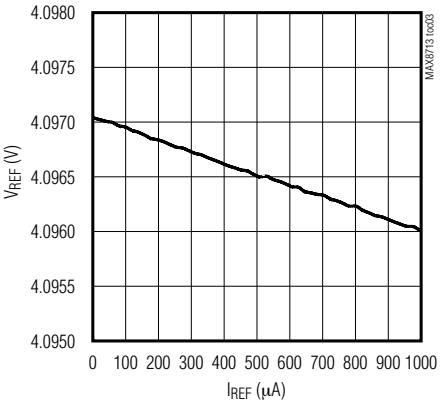
LDO LOAD REGULATION



LDO LINE REGULATION



REFERENCE LOAD REGULATION

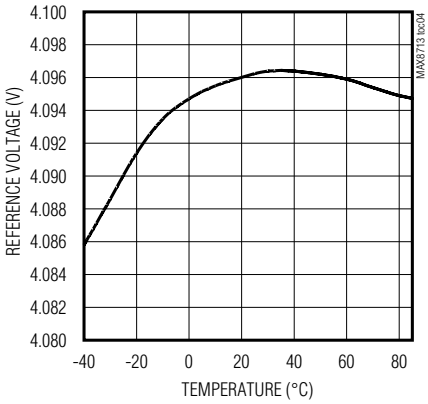


Simplified Multichemistry SMBus Battery Charger

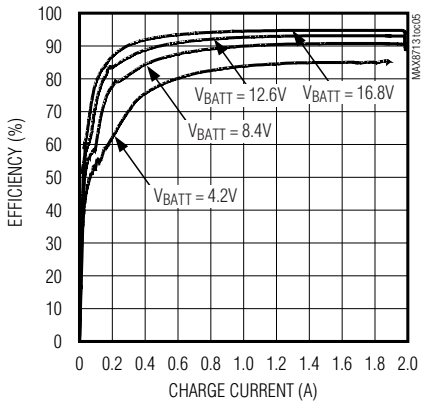
Typical Operating Characteristics (continued)

(V_{DCIN} = V_{DCSNS} = 20V, Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

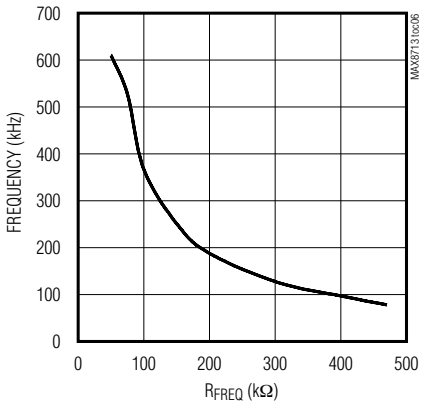
REFERENCE VOLTAGE vs. TEMPERATURE



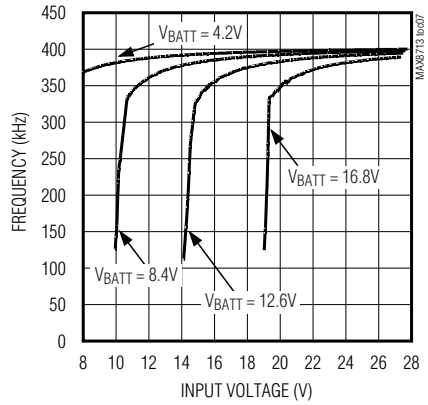
EFFICIENCY vs. CHARGE CURRENT



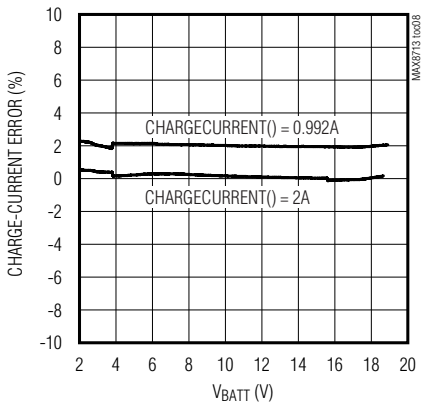
FREQUENCY vs. R_{FREQ}



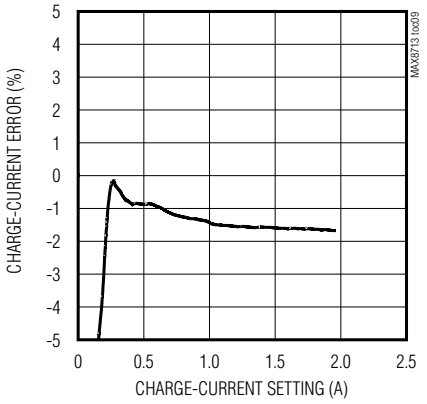
FREQUENCY vs. V_{IN}



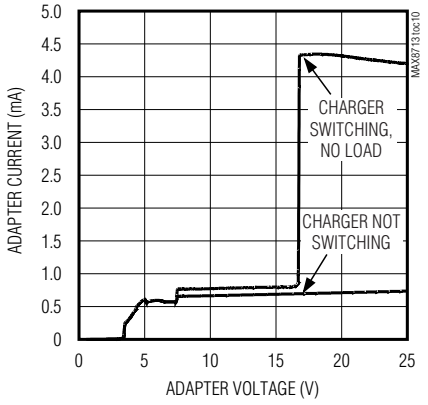
CHARGE-CURRENT ERROR vs. BATTERY VOLTAGE



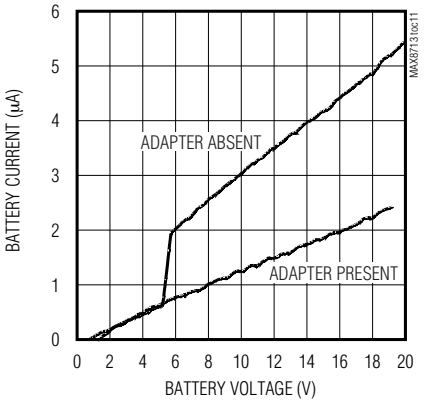
CHARGE-CURRENT ERROR vs. CHARGE-CURRENT SETTING



ADAPTER CURRENT vs. ADAPTER VOLTAGE



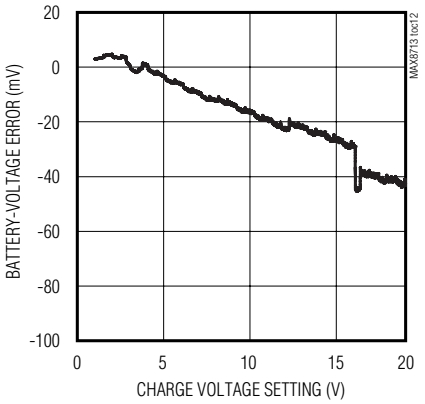
BATTERY CURRENT vs. BATTERY VOLTAGE



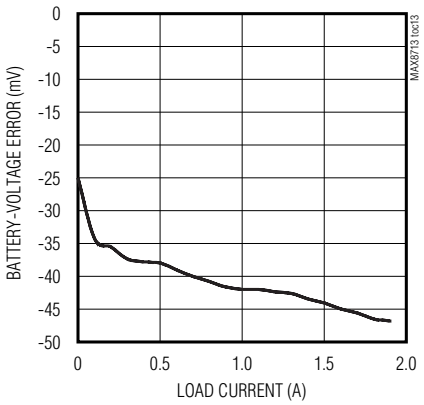
Typical Operating Characteristics (continued)

(V_{DCIN} = V_{DCSNS} = 20V, Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

BATTERY-VOLTAGE ERROR vs. CHARGE VOLTAGE SETTING



BATTERY-VOLTAGE ERROR vs. LOAD



Pin Description

PIN	NAME	FUNCTION
1	REF	4.096V Voltage Reference. Bypass REF with a 1µF capacitor to GND.
2	IC1	Internally Connected. Connect to the exposed paddle for improved layout.
3	CCI	Output Current-Regulation Loop Compensation Point. Connect 0.01µF to GND.
4	CCV	Voltage-Regulation Loop Compensation Point. Connect 10kΩ in series with 0.01µF to GND.
5	DAC	DAC Voltage Output. Bypass with a 0.1µF capacitor to GND.
6	V_{DD}	Logic Circuitry Supply Voltage Input. Bypass with a 0.1µF capacitor to GND.
7	SDA	SMBus Data IO. Open-drain output. Connect the external pullup resistor according to SMBus specifications.
8	SCL	SMBus Clock Input. Connect the external pullup resistor according to SMBus specifications.
9	IC2	Internally Connected. Connect to the exposed paddle for improved layout.
10	FREQ	t_{OFF} Frequency Adjust Input. Connect a 100kΩ to 400kΩ resistor between FREQ and GND to set the PWM frequency.
11	GND	Analog Ground
12	BATT	Battery Voltage Sense Input
13	CSIN	Output Current-Sense Negative Input
14	IC3	Internally Connected. Connect to the exposed paddle for improved layout.
15	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
16	PGND	Power Ground
17	DLO	Low-Side Power MOSFET Driver Output. Connect to the low-side n-channel MOSFET gate.
18	DLOV	Low-Side Driver Supply. Bypass DLOV with a 1µF capacitor to PGND. Connect a 33Ω resistor from LDO to DLOV for filtering.

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Pin Description (continued)

PIN	NAME	FUNCTION
19	LX	High-Side Power MOSFET Driver Power-Supply Connection. Connect a 0.1µF capacitor from BST to LX.
20	DHI	High-Side Power MOSFET Driver Output. Connect to the high-side n-channel MOSFET gate.
21	BST	High-Side Power MOSFET Driver Power-Supply Connection. Connect a 0.1µF capacitor from BST to LX.
22	DCSNS	DC Supply-Voltage Sense Input. Charging is disabled for $V_{DCSNS} < V_{CSIN} + 100mV$. DCSNS is also used to calculate the switching regulator's off-time.
23	LDO	Device Power Supply. LDO is the output of the 5.4V linear regulator supplied from DCIN. Bypass LDO with a 1µF ceramic capacitor from LDO to GND.
24	DCIN	Charger Bias Supply Input. Bypass DCIN with a 0.1µF ceramic capacitor to PGND.

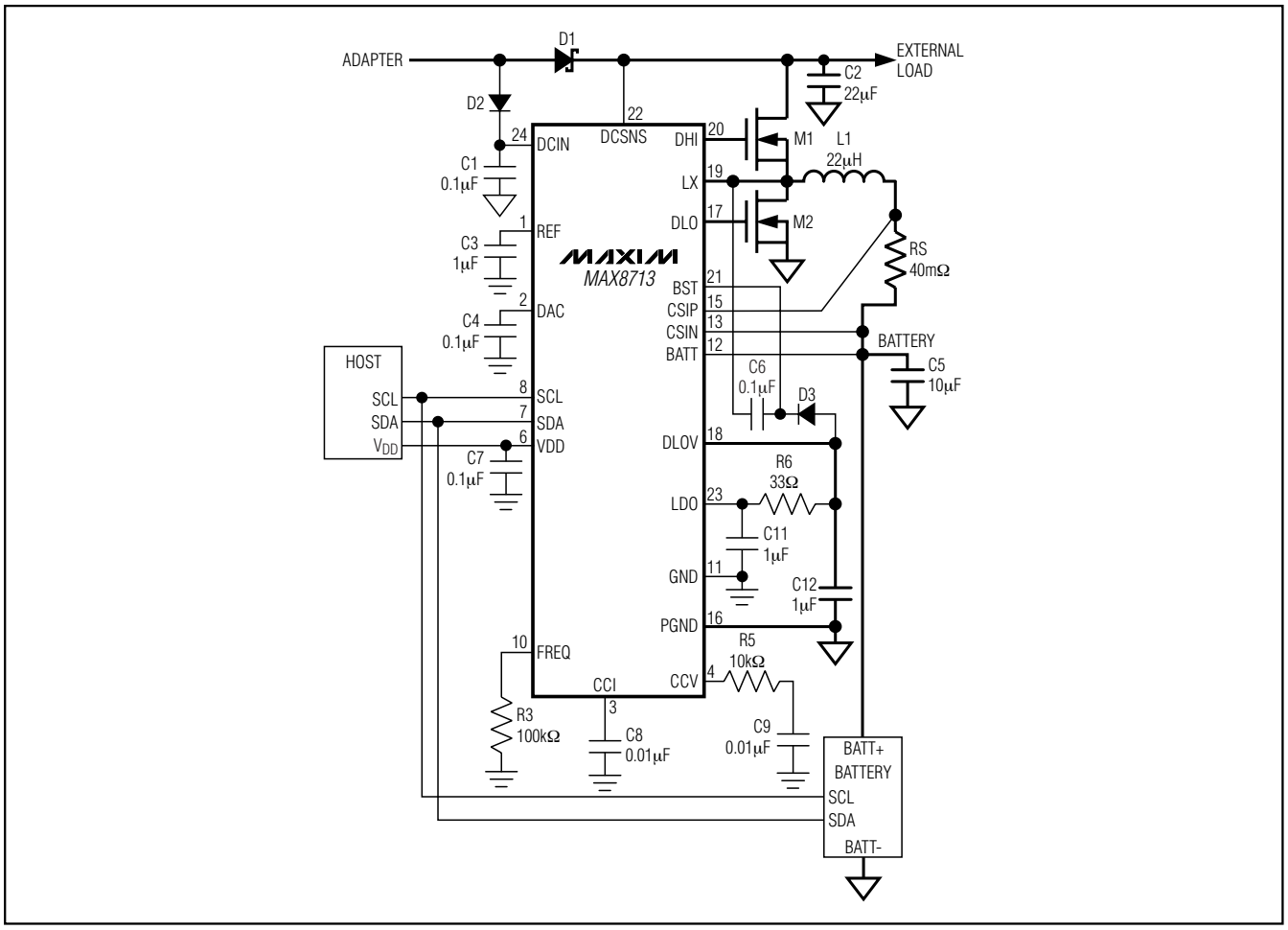

Figure 1. Typical Application Circuit

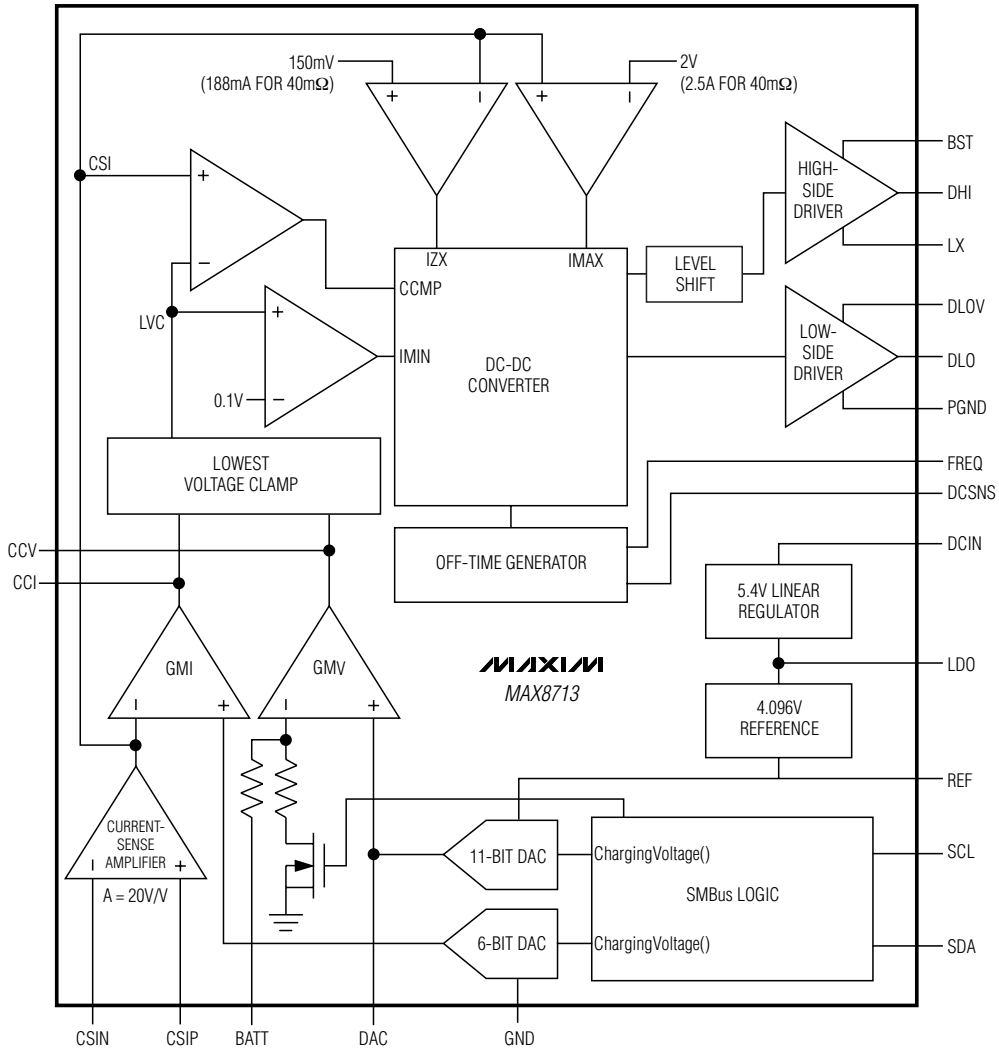

Figure 2. Functional Diagram

Detailed Description

The MAX8713 includes all of the functions necessary to charge Li+, NiMH, and NiCd smart batteries. A high-efficiency, synchronous-rectified, step-down DC-DC converter is used to implement a precision constant-current, constant-voltage charger. The DC-DC converter drives a high-side n-channel MOSFET and provides synchronous rectification with a low-side n-channel MOSFET. The charge current-sense amplifier has a low input offset error, allowing the use of small-valued sense resistors. The MAX8713 features a voltage-regulation loop (CCV) and a current-regulation loop (CCI). CCI and CCV operate independently of each other. The CCV voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set by the ChargeVoltage() command. The CCI battery current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current limit set by the ChargeCurrent() command. The charge current-regulation loop is in control as long as the BATT voltage is below the set point. When the BATT voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point.

Simplified Multichemistry SMBus Battery Charger

The circuit shown in Figure 1 demonstrates a typical application for smart-battery systems. A functional diagram is shown in Figure 2.

Setting Charge Voltage

To set the output voltage of the MAX8713, use the SMBus to write a 16-bit ChargeVoltage() command. This 16-bit command translates to a 1mV LSB and a 65.535V full-scale voltage. The MAX8713 ignores the first 4 LSBs and uses the next 11 bits to set the voltage DAC. The charge voltage range of the MAX8713 is 0 to 19.200V. All codes requesting charge voltage greater than 19.200V result in a voltage setting of 19.200V. All codes requesting charge voltage below 1.024V result in a voltage set point of zero, which terminates charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains shut down until a ChargeVoltage() and ChargeCurrent() command is sent.

The ChargeVoltage() command uses the Write-Word protocol (Figure 5). The command code for ChargeVoltage() is 0x15 (0b00010101). The 16-bit binary number formed by D15–D0 represents the charge-voltage set point in mV. However, the resolution of the MAX8713 is 16mV in setting the charge voltage because the D0–D3 bits are ignored as shown in Table 1. The D15 bit is also ignored because it is not needed to span the 0 to 19.2V range. Figure 3 shows the mapping between the charge-voltage set point and the ChargeVoltage() code. All codes requesting charge voltage greater than 19.200V result in a 19.200V setting. All codes requesting charge voltage below 1024mV result in a voltage set point of zero, which terminates charging.

Upon initial power-up, ChargingVoltage() is reset to zero and a ChargingVoltage() command must be sent to initiate charging.

Setting Charge Current

To set the charge current for the MAX8713, use the SMBus interface to write a 16-bit ChargeCurrent() command. This 16-bit command translates to a 1mA per LSB and a 65.535A full-scale current using a 40mΩ current-sense resistor (RS in Figure 1). Equivalently, the ChargeCurrent() value sets the voltage across the CSIP and CSIN inputs in 40µV increments. The MAX8713 ignores the lowest 5 LSBs and uses the next 6 bits to set the current DAC. The charge current range is 0 to 2.016A using a 40mΩ current-sense resistor. All codes requesting charge current above 2.016A result in a setting of 2.016A. For larger current settings, scale down the sense resistor. All codes requesting charge current between 1mA to 32mA result in a current setting of 32mA. To stop charging, set ChargeCurrent() to 0. Upon initial power-up, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains shut down. To start the charger, send valid ChargeVoltage() and ChargeCurrent() commands.

The ChargeCurrent() command uses the Write-Word protocol (Figure 5). The command code for ChargeCurrent() is 0x14 (0b00010100). Table 2 shows the format of the ChargeCurrent() register. Figure 4 shows the mapping between the charge-current set point and the ChargeCurrent() code. The default charge current setting at power-up is 0mA.

LDO Regulator

An integrated low-dropout (LDO) linear regulator provides a 5.4V supply derived from DCIN, and delivers over 5mA of load current. The LDO powers the gate drivers of the n-channel MOSFETs in the DC-DC converter. See the *MOSFET Drivers* section. The LDO also biases the 4.096V reference and most of the control circuitry. Bypass LDO to GND with a 1µF ceramic capacitor.

V_{DD} Supply

The V_{DD} input provides power to the SMBus interface. Connect V_{DD} to LDO, or apply an external supply to V_{DD} to keep the SMBus interface active while the supply to DCIN is removed. When V_{DD} is biased, the internal registers are maintained. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor.

Operating Conditions

Table 3 is a summary of operating states of the MAX8713.

- **Adapter Present.** When DCIN is greater than 7.5V, the adapter is considered to be present. In this condition, both the LDO and REF function properly and battery charging is allowed.
- **Power Fail.** When DCIN is less than BATT + 0.3V, the MAX8713 is in the power-fail state, since the DC-DC converter is in dropout. The charger will not attempt to charge when in the power-fail state.
- **V_{DD} Undervoltage.** When V_{DD} is less than 2.5V, the V_{DD} supply is considered to be in an undervoltage state. The SMBus interface does not respond to commands. When coming out of the undervoltage condition, the part is in its power-on reset state. No charging occurs when V_{DD} is in the undervoltage state. When V_{DD} is greater than 2.5V, SMBus registers are preserved.

Table 1. ChargeVoltage()

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mV weight.
1	—	Not used. Normally a 2mV weight.
2	—	Not used. Normally a 4mV weight.
3	—	Not used. Normally an 8mV weight.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charge-voltage compliance, 1024mV (min). 1 = Adds 16mV of charge-voltage compliance.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charge-voltage compliance, 1024mV (min). 1 = Adds 32mV of charge-voltage compliance.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charge-voltage compliance, 1024mV (min). 1 = Adds 64mV of charge-voltage compliance.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charge-voltage compliance, 1024mV (min). 1 = Adds 128mV of charge-voltage compliance.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charge-voltage compliance, 1024mV (min). 1 = Adds 256mV of charge-voltage compliance.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charge-voltage compliance, 1024mV (min). 1 = Adds 512mV of charge-voltage compliance.
10	Charge Voltage, DACV 6	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 1024mV of charge-voltage compliance.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 2048mV of charge-voltage compliance.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 4096mV of charge-voltage compliance.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 8192mV of charge-voltage compliance.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charge-voltage compliance. 1 = Adds 16,384mV of charge-voltage compliance, 19,200mV (max).
15	—	Not used. Normally a 32,768mV weight.

Command: 0x15

SMBus Interface

The MAX8713 receives control inputs from the SMBus interface. The serial interface complies with the SMBus protocols as documented in the System Management Bus Specification V1.1, which can be downloaded from www.smbus.org. The MAX8713 uses the SMBus Read-Word and Write-Word protocols (Figure 5) to communicate with the smart battery. The MAX8713 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ (0x12). In addition, the MAX8713 has two identification (ID) registers: a 16-bit device ID register and a 16-bit manufacturer ID register.

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high.

Table 2. ChargeCurrent()

BIT	BIT NAME	DESCRIPTION
0	—	Not used. Normally a 1mA weight.
1	—	Not used. Normally a 2mA weight.
2	—	Not used. Normally a 4mA weight.
3	—	Not used. Normally an 8mA weight.
4	—	Not used. Normally a 16mA weight.
5	Charge Current DAC, bit 0	0 = Adds 0mA of charger current compliance. 1 = Adds 32mA of charger current compliance.
6	Charge Current DAC, bit 1	0 = Adds 0mA of charger current compliance. 1 = Adds 64mA of charger current compliance.
7	Charge Current DAC, bit 2	0 = Adds 0mA of charger current compliance. 1 = Adds 128mA of charger current compliance.
8	Charge Current DAC, bit 3	0 = Adds 0mA of charger current compliance. 1 = Adds 256mA of charger current compliance.
9	Charge Current DAC, bit 4	0 = Adds 0mA of charger current compliance. 1 = Adds 512mA of charger current compliance.
10	Charge Current DAC, bit 5	0 = Adds 0mA of charger current compliance. 1 = Adds 1024mA of charger current compliance. 2016mA (max).
11	—	Not used. Normally a 2048mA weight.
12	—	Not used. Normally a 4096mA weight.
13	—	Not used. Normally a 8192mA weight.
14	—	Not used. Normally a 16,384mA weight.
15	—	Not used. Normally a 32,768mA weight.

Command: 0x14

The bus is then free for another transmission. Figures 6 and 7 show the timing diagram for signals on the SMBus interface. The address-byte, command-byte, and data-bytes are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the MAX8713 because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock. The MAX8713 supports the charger commands as described in Tables 2–4.

Battery Charger Commands

The MAX8713 supports four battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 2. ManufacturerID() and DeviceID() can be used to identify the MAX8713. On the MAX8713, ManufacturerID() always returns 0x004D and DeviceID() always returns 0x0007.

DC-DC Converter

The MAX8713 employs a pseudo-fixed-frequency, current-mode control scheme with cycle-by-cycle current limit. The controller's constant off-time (t_{OFF}) is calculated based on V_{DCIN}, V_{BATT}, and R_{FREQ}, and has a minimum value of 300ns. The operation of the DC-DC controller is determined by the following four comparators as shown in the functional diagram (Figure 2):

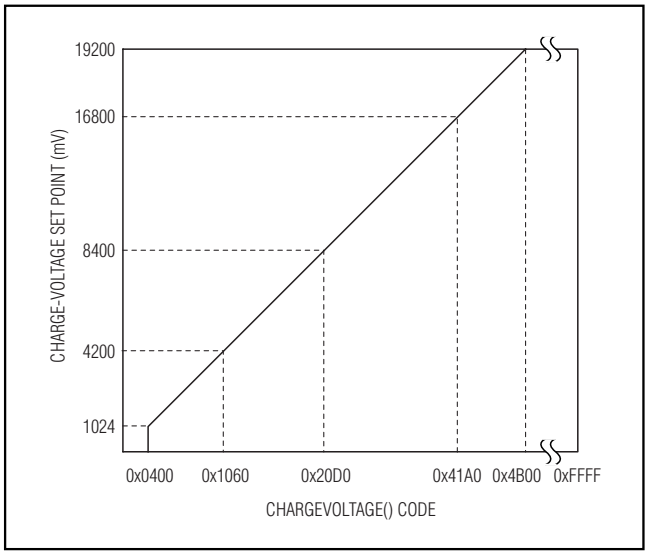

Figure 3. ChargeVoltage() Code to Charge-Voltage Set-Point Mapping

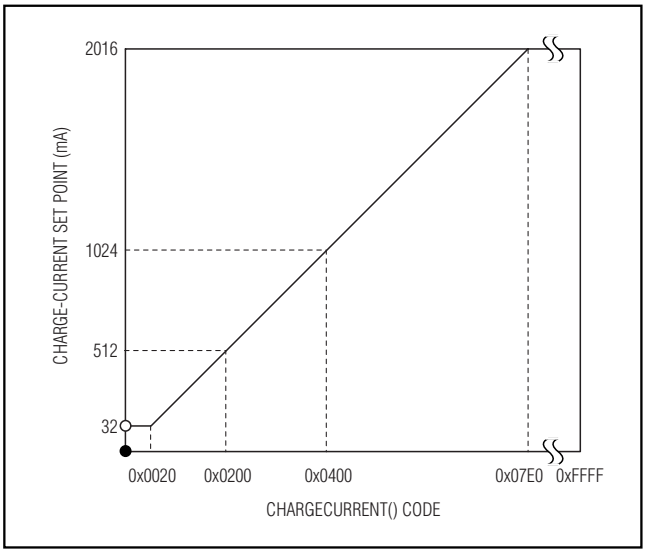

Figure 4. ChargeCurrent() Code to Charge-Current Set Point Mapping (R_2 = 40mΩ)

Table 3. Summary of Operating States

INPUT CONDITIONS	OPERATING STATES		
	ADAPTER PRESENT	POWER FAIL	V_{DD} UNDERVOLTAGE
DCIN	V_{DCIN} > 7.5V	V_{DCIN} < V_{BATT} + 0.1V	X
BATT	X	V_{BATT} > V_{DCIN} - 0.1V	X
V_{DD}	X	X	V_{DD} < 2.5V

X = Don't care.

The **IMIN** comparator sets the peak inductor current in discontinuous mode. IMIN compares the control signal (LVC) against 100mV (typ). When LVC voltage is less than 100mV, DHI and DLO are both low.

The **CCMP** comparator is used for current-mode regulation in continuous-conduction mode. CCMP compares LVC against the charging-current feedback signal (CSI). The comparator output is high and the high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.

The **IMAX** comparator provides a cycle-by-cycle current limit. IMAX compares CSI to 2V (corresponding to 2.5A when RS = 40mΩ). The comparator output is high and the high-side MOSFET on-time is terminated when the current-sense signal exceeds 2.5A. A new cycle cannot start until the IMAX comparator output goes low.

The **ZCMP** comparator provides zero-crossing detection during discontinuous conduction. ZCMP compares the current-sense feedback signal to 188mA (RS = 40mΩ). When the inductor current is lower than the 188mA threshold, the comparator output is high and DLO is turned off.

Setting the Switching Frequency

The MAX8713 features an adjustable switching frequency. To set the switching frequency, choose R_{FREQ} according to the following equation:

$$R_{FREQ} = \frac{100kHz \times 400k\Omega}{f_{SWITCH}}$$

Higher switching frequencies are typically preferred to minimize inductor and capacitor requirements. See the *Typical Operating Characteristics*. The switching frequency has a minor dependence on V_{DCIN} and V_{BATT} because of voltage losses along the high current path and other 2nd-order effects not accounted in the MAX8713's off-time calculation. These can be accounted for by observing the curves in the *Typical Operating Characteristics*.

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a) WRITE-WORD FORMAT

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	
	PRESET to 0b0001001			ChargingCurrent() = 0x14 ChargerVoltage() = 0x15		D7 D0		D15 D8		

b) READ-WORD FORMAT

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 BITS	1b	1b	8 BITS	1b		7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	
	PRESET to 0b0001001			DeviceID() = 0xFF ManufacturerID() = 0xFE			PRESET to 0b0001001			D7 D0		D15 D8		

LEGEND
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC LOW)
W = WRITE BIT (LOGIC LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC HIGH)
R = READ BIT (LOGIC HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 5. SMBus Write-Word and Read-Word Protocols

CCV, CCI, and LVC Control Blocks

The MAX8713 controls charge current (CCI control loop) or charge voltage (CCV control loop), depending on the operating condition. The two control loops CCV and CCI are brought together internally at the LVC (lowest voltage clamp) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage of CCV and CCI appears at the output of the LVC amplifier and clamps the remaining control loop to within 0.3V above the control point. Clamping the other control loop close to the lowest control loop ensures fast transition with minimal overshoot when switching between different regulation modes (see the *Compensation* section).

Continuous-Conduction Mode

With sufficient charge current, the MAX8713's inductor current never crosses zero, which is defined as continuous-conduction mode. The regulator switches at 400kHz (R_{FREQ} = 100kΩ) if it is not in dropout (V_{BATT} < 0.88 × V_{DCIN}). The controller starts a new cycle by turning on the high-side MOSFET and turning off the low-side MOSFET. When the charge-current feedback signal (CSI) is greater than the control point (LVC), the CCMP comparator output goes high and the controller initiates the off-time by turning off the high-side MOSFET and turning on the low-side MOSFET. The operating frequency is governed by the off-time and is dependent upon V_{DCIN}, V_{BATT}, and R_{FREQ}. See the *Setting the Switching Frequency* section for more information.

At the end of the fixed off-time, the controller initiates a new cycle if the control point (LVC) is greater than 100mV, and the peak charge current is less than the cycle-by-cycle current limit. Restated another way, IMIN must be high and IMAX must be low for the controller to initiate a new cycle. If the peak inductor current exceeds the IMAX comparator threshold, then the on-time is terminated. The cycle-by-cycle current limit effectively protects against overcurrent and short-circuit faults.

There is a 0.3µs minimum off-time when the (V_{DCSNS} - V_{BATT}) differential becomes too small. If $V_{BATT} \geq 0.88 \times V_{DCSNS}$, then the threshold for minimum off-time is reached and the off-time is fixed at 0.3µs. The switching frequency in this mode varies according to the equation:

$$f = \frac{V_{IN} - V_{OUT}}{0.3\mu s \times V_{IN}}$$

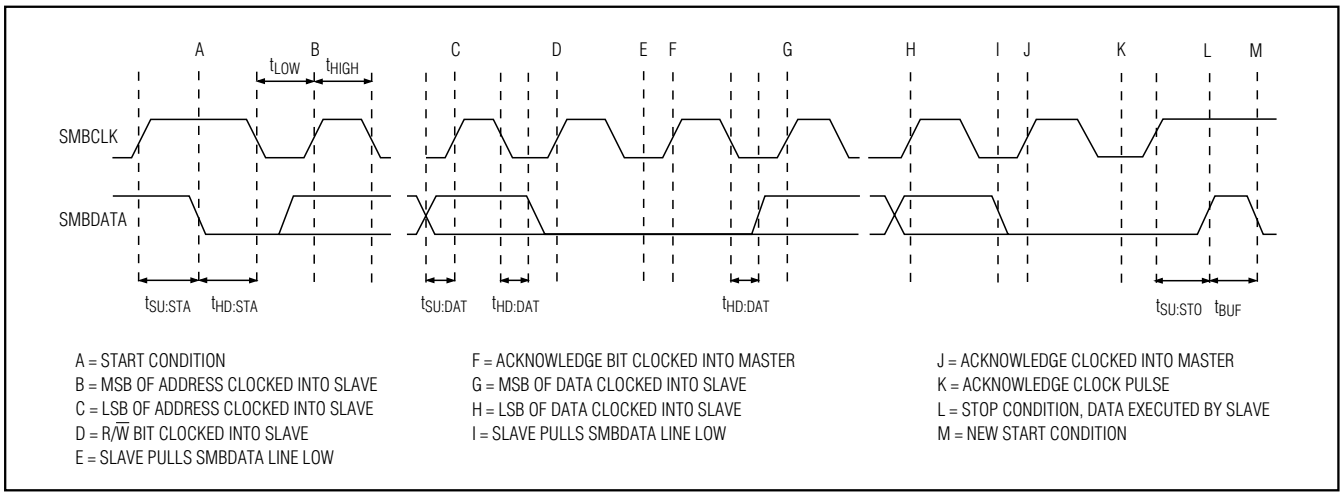

Figure 6. SMBUs Write Timing

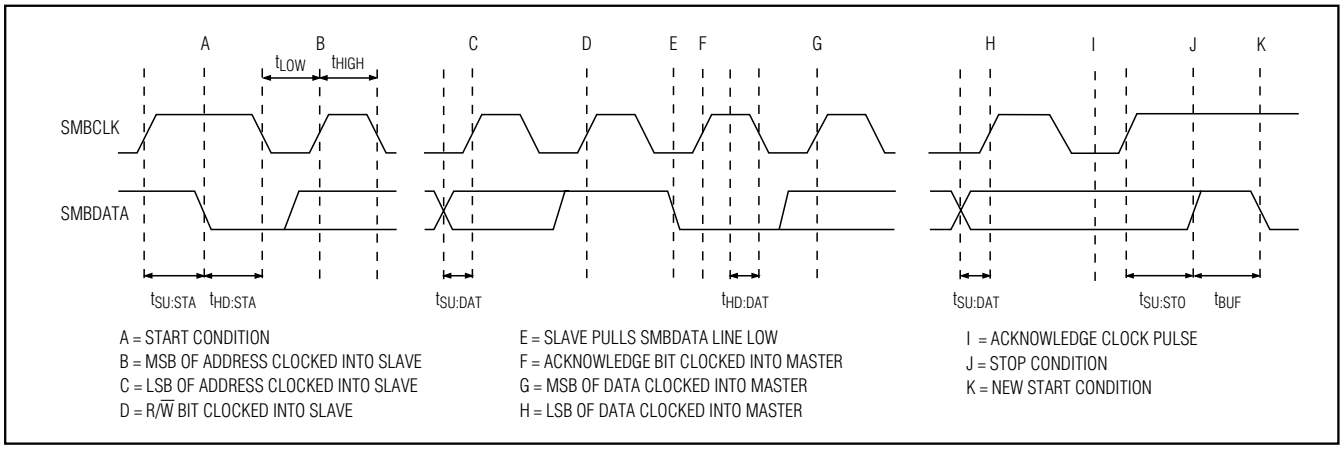

Figure 7. SMBus Read Timing

Table 4. Battery-Charger Command Summary

COMMAND	COMMAND NAME	READ/WRITE	DESCRIPTION	POR STATE
0x14	ChargeCurrent()	Write Only	6-Bit Charge Current Setting	0x0000
0x15	ChargeVoltage()	Write Only	11-Bit Charge Voltage Setting	0x0000
0xFE	ManufacturerID()	Read Only	Manufacturer ID	0x004D
0xFF	DeviceID()	Read Only	Device ID	0x0007

Discontinuous Conduction

The MAX8713 can also operate in discontinuous-conduction mode to ensure that the inductor current is always positive. The MAX8713 enters discontinuous-conduction mode when the output of the LVC control point falls below 100mV. For RS = 40mΩ, this corresponds to 62.5mA.

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$$I_{DIS} = 0.5 \times \frac{100mV}{20 \times RS} = 62.5mA$$

charge current for RS = 40mΩ

In discontinuous mode, a new cycle is not started until the LVC voltage rises above 100mV. Discontinuous-mode operation can occur during conditioning charge of overdischarged battery packs or when the charger is in constant voltage mode as the charge current drops to zero.

Compensation

The charge voltage and charge current-regulation loops are compensated separately and independently at CCV and CCI.

CCV Loop Compensation

The simplified schematic in Figure 9 is sufficient to describe the operation of the MAX8713 when the voltage loop (CCV) is in control. The required compensation network is a pole-zero pair formed with C_{CV} and R_{CV}. The pole is necessary to roll off the voltage loop's response at low frequency. The zero is necessary to compensate the pole formed by the output capacitor and the load. R_{ESR} is the equivalent series resistance (ESR) of the charger output capacitor (C_{OUT}). R_L is the equivalent charger output load, where $R_L = \Delta V_{BATT} / \Delta I_{CHG}$. The equivalent output impedance of the GMV amplifier, R_{OGMV}, is greater than 10MΩ. The voltage amplifier transconductance, GMV = 0.125µA/mV. The DC-DC converter transconductance is dependent upon the charge current-sense resistor RS:

$$GM_{OUT} = \frac{1}{A_{CSI} \times RS}$$

where A_{CSI} = 20 and RS = 0.04Ω in the typical application circuits, so GM_{OUT} = 1.25A/V.

The loop-transfer function is given by:

$$LTF = GM_{OUT} \times R_L \times GMV \times R_{OGMV} \times \left[\frac{(1+sC_{OUT} \times R_{ESR})(1+sC_{CV} \times R_{CV})}{(1+sC_{CV} \times R_{OGMV})(1+sC_{OUT} \times R_L)}\right]$$

The poles and zeros of the voltage loop-transfer function are listed from lowest frequency to highest frequency in Table 5.

Near crossover, C_{CV} is much lower impedance than R_{OGMV}. Since C_{CV} is in parallel with R_{OGMV}, C_{CV} dominates the parallel impedance near crossover. Additionally R_{CV} is much higher impedance than C_{CV} and dominates the series combination of R_{CV} and C_{CV}, so:

$$\frac{R_{OGMV} \times (1+sC_{CV} \times R_{CV})}{(1+sC_{CV} \times R_{OGMV})} \cong R_{CV}$$

C_{OUT} is also much lower impedance than R_L near crossover, so the parallel impedance is mostly capacitive and:

$$\frac{R_L}{(1+sC_{OUT} \times R_L)} \cong \frac{1}{sC_{OUT}}$$

If R_{ESR} is small enough, its associated output zero has a negligible effect near crossover and the loop-transfer function can be simplified as follows:

$$LTF = GM_{OUT} \times \frac{R_{CV}}{sC_{OUT}} \times G_{MV}$$

Setting LTF = 1 to solve for the unity-gain frequency yields:

$$f_{CO\_CV} = GM_{OUT} \times G_{MV} \times \frac{R_{CV}}{2\pi \times C_{OUT}}$$

For stability, choose a crossover frequency less than 1/10 of the switching frequency. For example, choosing a crossover frequency of 25kHz and solving for R_{CV} using the component values listed in Figure 1 yields: R_{CV} = 10kΩ.

V_{BATT} = 8.4V	GMV = 0.125mA/mV
I_{CHG} = 2A	GM_{OUT} = 1.25A/V
C_{OUT} = 10µF	f_{OSC} = 400kHz
R_L = 0.2Ω	f_{CO_CV} = 25kHz

$$R_{CV} = \frac{2\pi \times C_{OUT} \times f_{CO\_CV}}{GMV \times GM_{OUT}} \cong 10k\Omega$$

To ensure that the compensation zero adequately cancels the output pole, select $f_{Z\_CV} \le f_{P\_OUT}$.

$$C_{CV} \ge (R_L / R_{CV}) \times C_{OUT}$$

$C_{CV} \ge$ 200pF (assuming 2 cells and 2A maximum charge current).

Figure 10 shows the Bode plot of the voltage loop frequency response using the values calculated above.

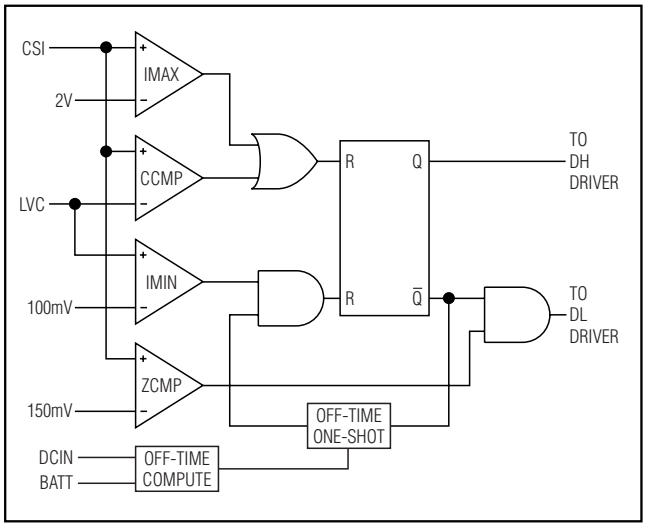


Figure 8. DC-DC Converter Block Diagram

CCI Loop Compensation

The simplified schematic in Figure 11 is sufficient to describe the operation of the MAX8713 when the battery current loop (CCI) is in control. Since the output capacitor's impedance has little effect on the response of the current loop, only a simple single pole is required to compensate this loop. A_{CSI} is the internal gain of the current-sense amplifier. RS is the charge current-sense resistor (40mΩ). R_{OGMI} is the equivalent output impedance of the GMI amplifier, which is greater than 10MΩ. GMI is the charge-current amplifier transconductance = 1µA/mV. GM_{OUT} is the DC-DC converter transconductance = 1.25A/V.

The loop-transfer function is given by:

$$LTF = GM_{OUT} \times A_{CSI} \times RS \times GMI \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}},$$

which describes a single-pole system.

$$\text{Since } GM_{OUT} = \frac{1}{A_{CSI} \times RS},$$

the loop-transfer function simplifies to:

$$LTF = GMI \frac{R_{OGMI}}{1 + sR_{OGMI} \times C_{CI}}$$

The crossover frequency is given by:

$$f_{CO\_CI} = \frac{GMI}{2\pi C_{CI}}$$

For stability, choose a crossover frequency lower than 1/10 of the switching frequency.

$C_{CI} > 10 \times GMI / (2\pi f_{OSC}) = 4nF$, for a 400kHz switching frequency (R_{FREQ} = 100kΩ).

Values for C_{CI} greater than ten times the minimum value may slow down the current-loop response. Choosing C_{CI}=10nF yields a crossover frequency of 15.9kHz. Figure 12 shows the Bode plot of the current-loop frequency response using the values calculated above.

MOSFET Drivers

The DHI and DLO outputs are optimized for driving moderate-sized power MOSFETs. The MOSFET drive capability is the same for both the low-side and high-side switches. This is consistent with the variable duty factor that occurs in the notebook computer environment where the battery voltage changes over a wide range. There must be a low-resistance, low-inductance path from the DLO driver to the MOSFET gate to prevent shoot-through. Otherwise, the sense circuitry in the MAX8713 will interpret the MOSFET gate as "off" while there is still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares or less (1.25mm to 2.5mm wide if the MOSFET is 25mm from the device). Unlike the DLO output, the DHI output uses a 50ns (typ) delay time to prevent the low-side MOSFET from turning on until DHI is fully off. The same considerations should be used for routing the DHI signal to the high-side MOSFET.

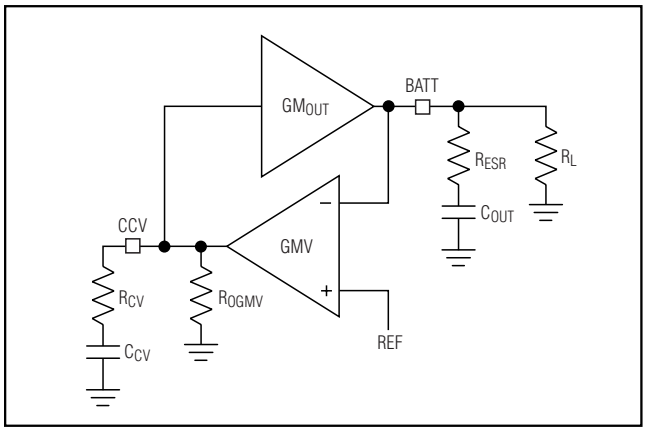


Figure 9. CCV Loop Diagram

Table 5. CCV Loop Poles and Zeros

NAME	EQUATION	DESCRIPTION
CCV Pole	$f_{P\_CV} = \frac{1}{2\pi R_{OGMV} \times C_{CV}}$	Lowest Frequency Pole Created by C_{CV} and GMV's Finite Output Resistance. Since R_{OGMV} is very large and not well controlled, the exact value for the pole frequency is also not well controlled (R_{OGMV} > 10MΩ).
CCV Zero	$f_{Z\_CV} = \frac{1}{2\pi R_{CV} \times C_{CV}}$	Voltage Loop-Compensation Zero. If this zero is at the same frequency or lower than the output pole f_{P_OUT}, then the loop-transfer function approximates a single-pole response near the crossover frequency. Choose C_{CV} to place this zero at least 1 decade below crossover to ensure adequate phase margin.
Output Pole	$f_{P\_OUT} = \frac{1}{2\pi R_L \times C_{OUT}}$	Output Pole Formed with the Effective Load Resistance (R_L) and the Output Capacitance (C_{OUT}). R_L influences the DC gain but does not affect the stability of the system or the crossover frequency.
Output Zero	$f_{Z\_OUT} = \frac{1}{2\pi R_{ESR} \times C_{OUT}}$	Output ESR Zero. This zero can keep the loop from crossing unity gain if f_{Z_OUT} is less than the desired crossover frequency; therefore, choose a capacitor with an ESR zero greater than the crossover frequency.

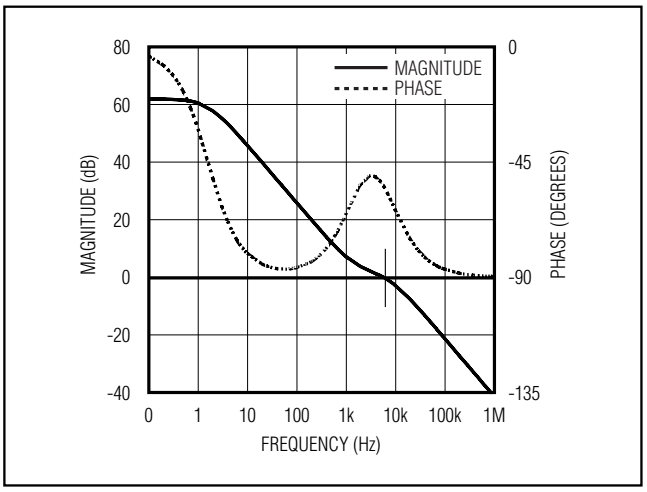


Figure 10. CCV Loop Response

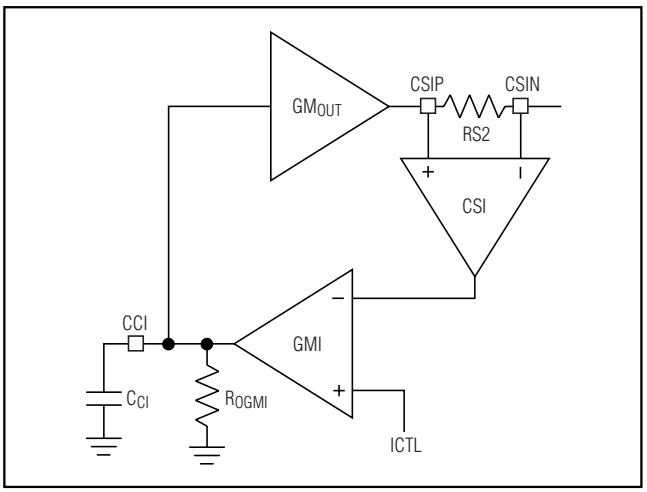


Figure 11. CCI Loop Diagram

The high-side driver (DHI) swings from LX to 5V above LX (BST) and has a typical impedance of 7Ω sourcing and 2Ω sinking. The low-side driver (DLO) swings from DLOV to ground and has a typical impedance of 2Ω sinking and 7Ω sourcing. This helps prevent DLO from being pulled up when the high-side switch turns on, due to capacitive coupling from the drain to the gate of the low-side MOSFET. This places some restrictions on the MOSFETs that can be used. Using a low-side MOSFET with smaller gate-to-drain capacitance can prevent these problems.

Design Procedure

MOSFET Selection

Choose the n-channel MOSFETs according to the maximum-required charge current. Low-current applications usually require less attention. The high-side MOSFET (M1) must be able to dissipate the resistive losses plus the switching losses at both $V_{DCIN(MIN)}$ and $V_{DCIN(MAX)}$. Calculate both of these sums.

Ideally, the losses at $V_{DCIN(MIN)}$ should be roughly equal to the losses at $V_{DCIN(MAX)}$, with lower losses in between. If the losses at $V_{DCIN(MIN)}$ are significantly

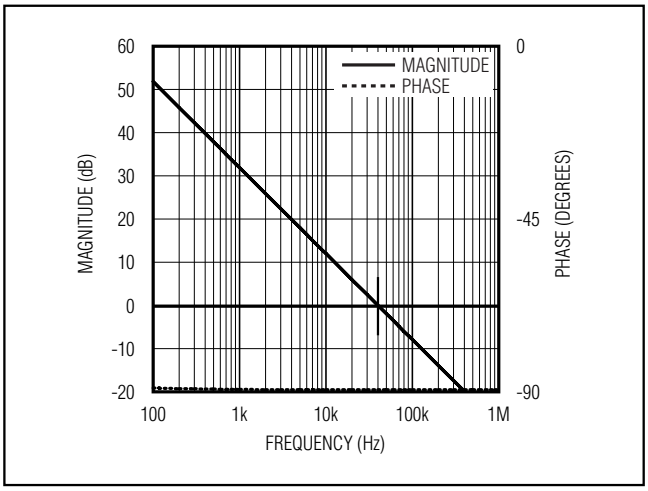


Figure 12. CCI Loop Response

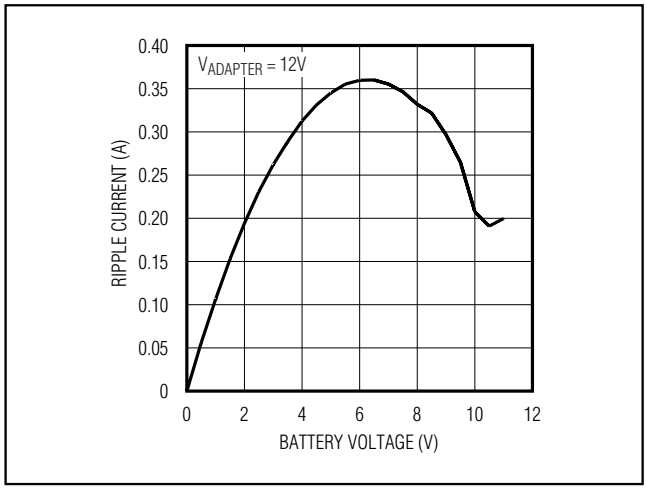


Figure 13. Ripple Current vs. Battery Voltage

higher than the losses at $V_{DCIN(MAX)}$, consider increasing the size of M1. Conversely, if the losses at $V_{DCIN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of M1. If DCIN does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses. Choose a low-side MOSFET that has the lowest-possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Make sure that the DLO gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur. Select devices that have short turn-off times, and make sure that M2($t_{DOFF(MAX)}$) - M1($t_{DON(MIN)}$) < 30ns, and M1($t_{DOFF(MAX)}$) - M2($t_{DON(MIN)}$) < 30ns. Failure to do so may result in efficiency-killing shoot-through currents.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET, the worst-case power dissipation (PD) due to resistance occurs at the minimum supply voltage:

$$PD_{(HIGH\text{-}SIDE)} = \left(\frac{V_{BATT}}{V_{DCIN}}\right)\left(\frac{I_{LOAD}}{2}\right)^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2f switching-loss equation. If the high-side MOSFET that was chosen for adequate $R_{DS(ON)}$ at low supply voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, then choose a MOSFET with lower losses. Calculating the power dissipation in M1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on M1:

$$PD_{(HS\_SWITCHING)} = \frac{V_{DCIN(MAX)}^2 \times C_{RSS} \times f_{SW} \times I_{LOAD}}{2 \times I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of M1, and I_{GATE} is the peak gate-drive source/sink current (0.7A sourcing and 2.5A sinking).

For the low-side MOSFET (M2), the worst-case power dissipation always occurs at maximum input voltage:

$$PD_{(LOW\text{-}SIDE)} = \left[1-\left(\frac{V_{BATT}}{V_{DCIN}}\right)\right]\left(\frac{I_{LOAD}}{2}\right)^2 \times R_{DS(ON)}$$

Simplified Multichemistry SMBus Battery Charger

Inductor Selection

The charge current, ripple, and operating frequency (off-time) determine the inductor characteristics. For optimum efficiency, choose the inductance according to the following equation:

$$L = V_{BATT} \times t_{OFF} / (0.3 \times I_{CHG})$$

This sets the ripple current to 1/3 of the charge current and results in a good balance between inductor size and efficiency. Higher inductor values decrease the ripple current. Smaller inductor values require high saturation current capabilities and degrade efficiency.

Inductor L1 must have a saturation current rating of at least the maximum charge current plus 1/2 of the ripple current (ΔIL):

$$I_{SAT} = I_{CHG} + (1/2)\ \Delta IL$$

The ripple current is determined by:

$$\Delta IL = V_{BATT} \times t_{OFF} / L$$

where $t_{OFF} = 2.5\mu s\ (V_{DCIN} - V_{BATT}) / V_{DCIN}$ for $V_{BATT} < 0.88\ V_{DCIN}$, or:

$$t_{OFF} = 0.3\mu s \text{ for } V_{BATT} > 0.88\ V_{DCIN}.$$

Figure 13 illustrates the variation of the ripple current vs. battery voltage when the circuit is charging at 2A with a fixed input voltage of 19V.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resilience to power-up surge currents.

$$I_{RMS} = I_{CHG}\left(\frac{\sqrt{V_{BATT}(V_{DCIN} - V_{BATT})}}{V_{DCIN}}\right)$$

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed approximately +10°C. The maximum ripple current occurs at 50% duty factor or $V_{DCIN} = 2 \times V_{BATT}$, which equates to $0.5 \times I_{CHG}$. If the application of interest does not achieve the maximum value, size the input capacitors according to the worst-case conditions.

Output Capacitor Selection

The output capacitor absorbs the inductor ripple current and must tolerate the surge current delivered from the battery when it is initially plugged into the charger. As such, both capacitance and ESR are important parameters in specifying the output capacitor as a filter and to ensure the stability of the DC-DC converter (see the *Compensation* section). Beyond the stability requirements, it is often sufficient to make sure that the output capacitor's ESR is simply much lower than the battery's ESR. Either tantalum or ceramic capacitors can be used on the output. Ceramic devices are preferable because of their good voltage ratings and resilience to surge currents.

Applications Information

Layout and Bypassing

Bypass DCIN with a 0.1µF ceramic to ground (Figure 1). D1 and D2 protect the MAX8713 when the DC power source input is reversed. A signal diode for D2 is adequate because DCIN only powers the LDO and the internal reference. Bypass V_{DD}, DCIN, LDO, DHIV, DLOV, SRC, DAC, and REF as shown in Figure 1.

Good PC board layout is required to achieve specified noise immunity, efficiency, and stable performance. The PC board layout artist must be given explicit instructions—preferably, a sketch showing the placement of the power switching components and high-current routing. Refer to the PC board layout in the MAX8713 evaluation kit for examples. A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections, the bottom layer for quiet connections, and the inner layers for uninterrupted ground planes.

Use the following step-by-step guide:

1) Place the high-power connections first, with their grounds adjacent:

- Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections.
- Minimize ground trace lengths in the high-current paths.
- Minimize other trace lengths in the high-current paths.
- Use >5mm-wide traces in the high-current paths.
- Connect C1 and C2 to the high-side MOSFET (10mm max length).
- Minimize the LX node (MOSFETs, rectifier cathode, inductor (15mm max length)). Keep LX on one side of the PC board to reduce EMI radiation.

Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the paddle. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems.

2) Place the IC and signal components. Keep the main switching node (LX node) away from sensitive analog components (current-sense traces and REF capacitor). **Note:** The IC must be no further than 10mm from the current-sense resistors. Quiet connections to REF, VMAX, IMAX, CCV, CCI, ACIN, and DCIN should be returned to a separate ground (GND) island. The appropriate traces are marked on the schematic with the () ground symbol. There is very little current flowing in these traces, so the ground island need not be very large. When placed on an inner layer, a sizable ground island can help simplify the layout because the low-current connections can be made through vias. The ground pad on the backside of the package should also be connected to this quiet ground island.
3) Keep the gate-drive traces (DHI and DLO) as short as possible (L < 20mm), and route them away from the current-sense lines and REF. These traces should also be relatively wide (W > 1.25mm).
4) Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Place the current-sense input filter capacitors under the part, connected directly to the GND pin.
5) Use a single-point star ground placed directly below the part at the PGND pin. Connect the power ground (ground plane) and the quiet ground island at this location.

Chip Information

TRANSISTOR COUNT: 8400

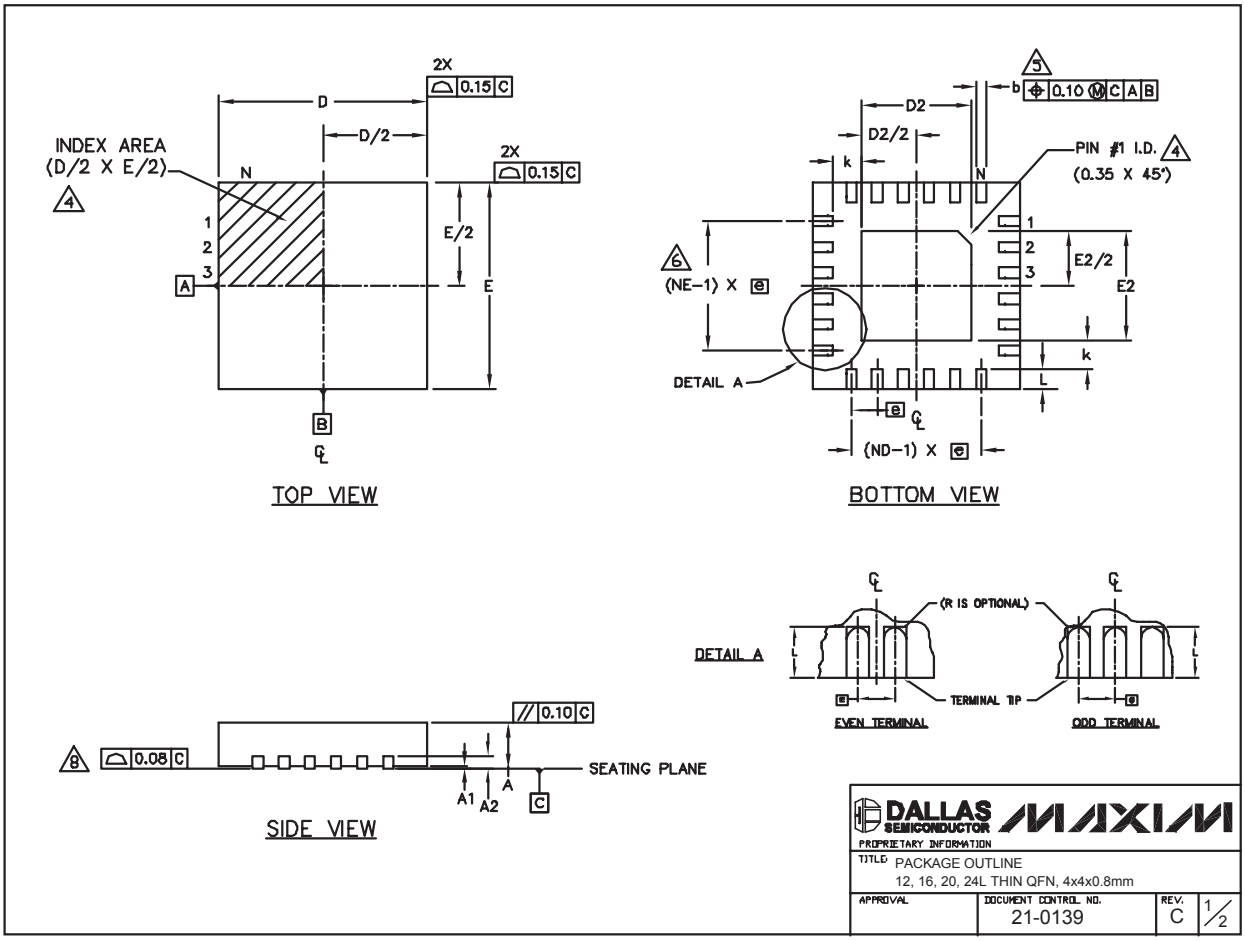
PROCESS: BiCMOS

Simplified Multichemistry SMBus Battery Charger

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12, 16, 20, 24L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	C	2/2