19-6376; Rev 0; 7/12

EVALUATION KIT AVAILABLE

MAX98096

Audio Hub with Wideband FlexSound Processor

General Description

The MAX98096 is a full-featured high performance audio hub with low power consumption and advanced signal processing, making it ideal for a wide range of portable applications.

Three differential analog microphone inputs and four 1-bit digital microphone inputs accept audio from main, accessory, and background microphones. Analog line inputs accept four single-ended or two differential audio signals.

Three digital audio interfaces supports standard PCM formats such as I²S, left justified, and TDM. Three integrated sample rate converters and highly configurable signal routing enable a wide range of use cases. The FlexSound™ audio processor provides low-power advanced signal processing, including equalization, dynamic range compression, speaker protection, microphone noise suppression during wideband calls, acoustic echo cancellation, and ambient aware outputs.

Integrated amplifiers can output signals from three DACs or any of the analog inputs. Amplifiers include a differential receiver amplifier, a stereo Class D speaker amplifier, a stereo Class H headphone amplifier, and four single-ended line outputs.

The 117-bump WLP (6.9mm x 4.7mm x 0.5mm pitch) package is fully specified over the -40°C to +85°C extended temperature range.

FlexSound is a trademark and DirectDrive is a registered trademark of Maxim Integrated Products, Inc.

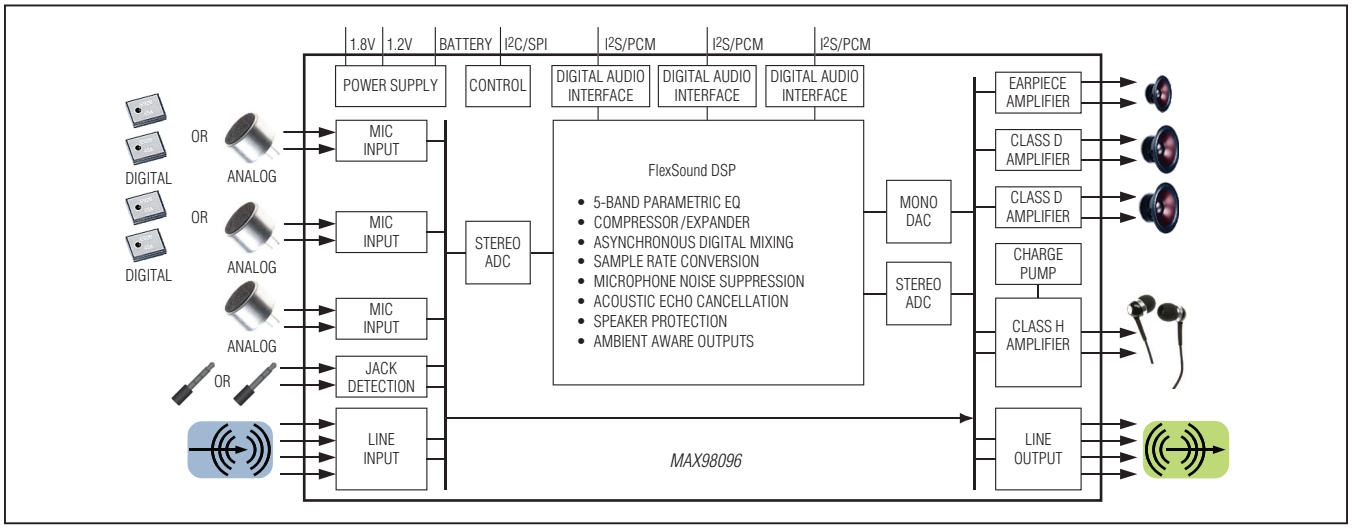
Benefits and Features

- **101dB DR Stereo DAC (8kHz < f_S < 96kHz)**
- **90dB DR Stereo ADC (8kHz < f_S < 96kHz)**
- **5.9mW Playback Power Consumption**
- **40kB Local Data RAM, 56kB Local Instruction ROM**
- **3 Stereo Single-Ended/Differential Analog Microphone Inputs (or 1 Analog/2 Stereo PDM Digital Microphone Inputs)**
- **2 Stereo Single-Ended/Mono Differential Line Inputs**
- **Three I²S/PCM/TDM Digital Audio Interfaces**
- **FlexSound Technology Signal Processing**
  - ✧ **Enhanced Speakerphone**
  - ✧ **Single/Dual Microphone Wideband Noise Suppression (16kHz Sampling Rate)**
  - ✧ **Ambient Aware Receiver Output**
  - ✧ **Acoustic Echo Cancellation**
- **Stereo Low EMI Class D Amplifiers**
  - ✧ **3.2W per Channel (4Ω, $V_{PVDD\_}$ = 5.0V)**
  - ✧ **1.2W per Channel (8Ω, $V_{PVDD\_}$ = 4.2V)**
- **Stereo DirectDrive® Headphone Amplifiers**
  - ✧ **Jack Detection and Identification**
- **Differential Receiver Amplifier/Stereo Line Output**
- **Asynchronous Digital Mixing and Sample Rate Conversion**

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maxim-ic.com/MAX98096.related.

Simplified Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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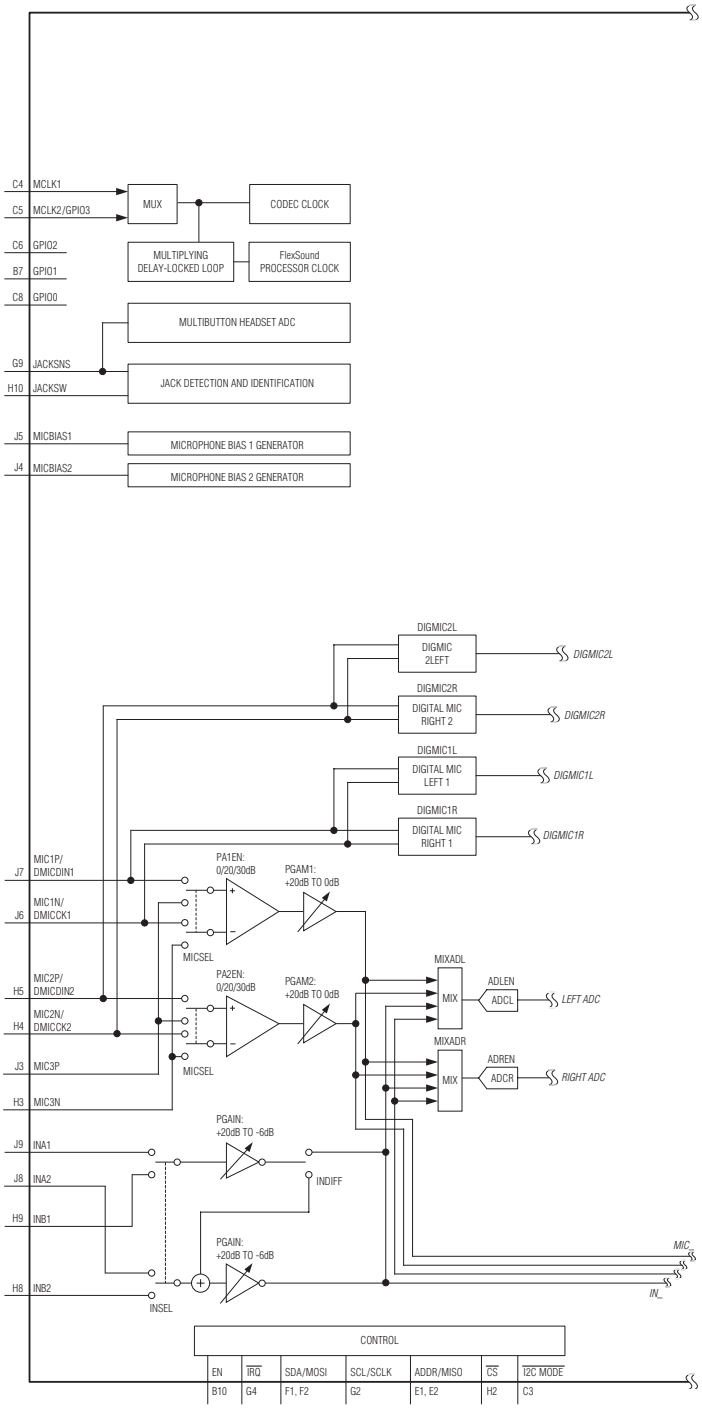
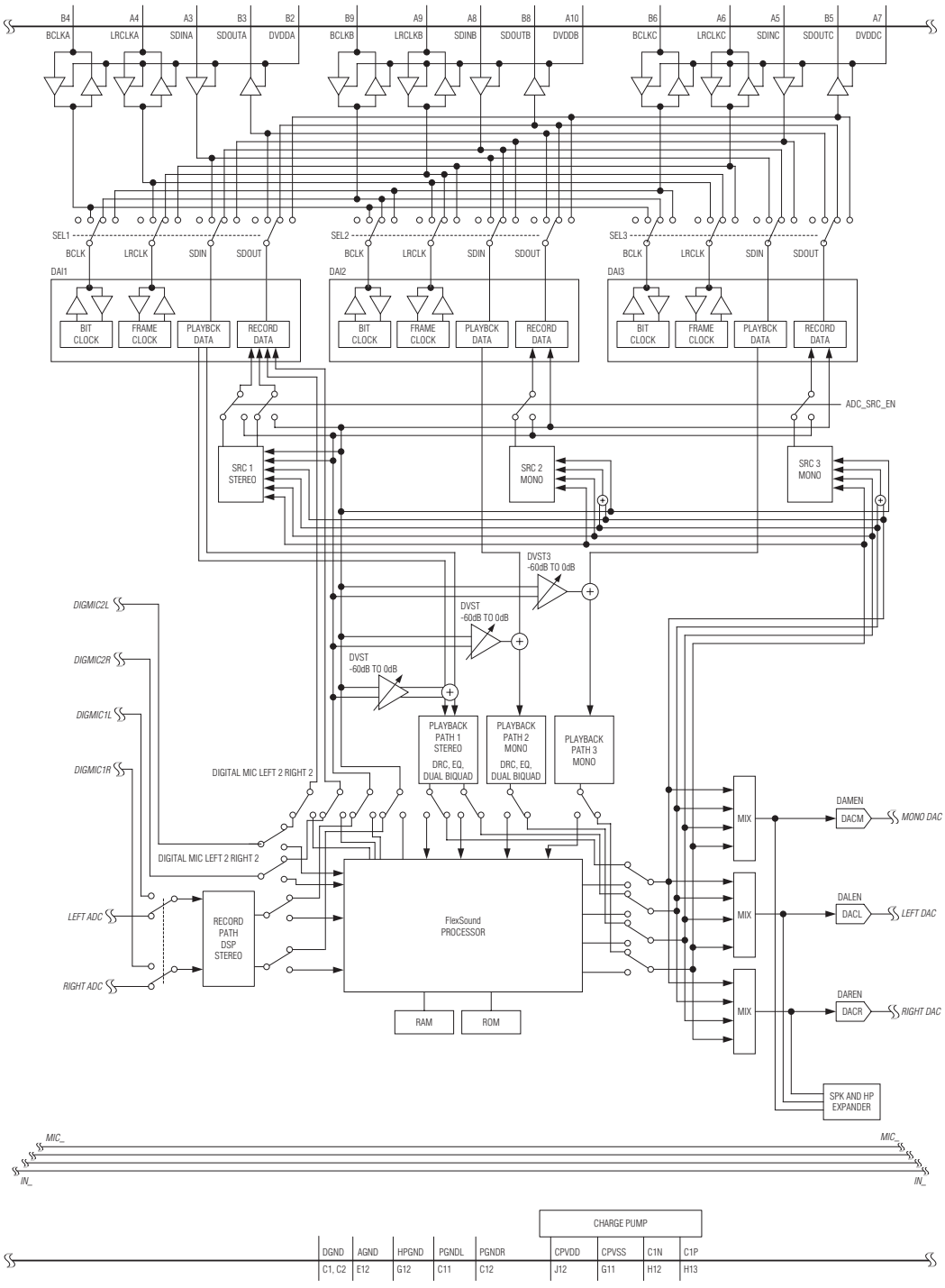
Functional Diagram (1 of 3)



Audio Hub with Wideband FlexSound Processor

Functional Diagram (2 of 3)



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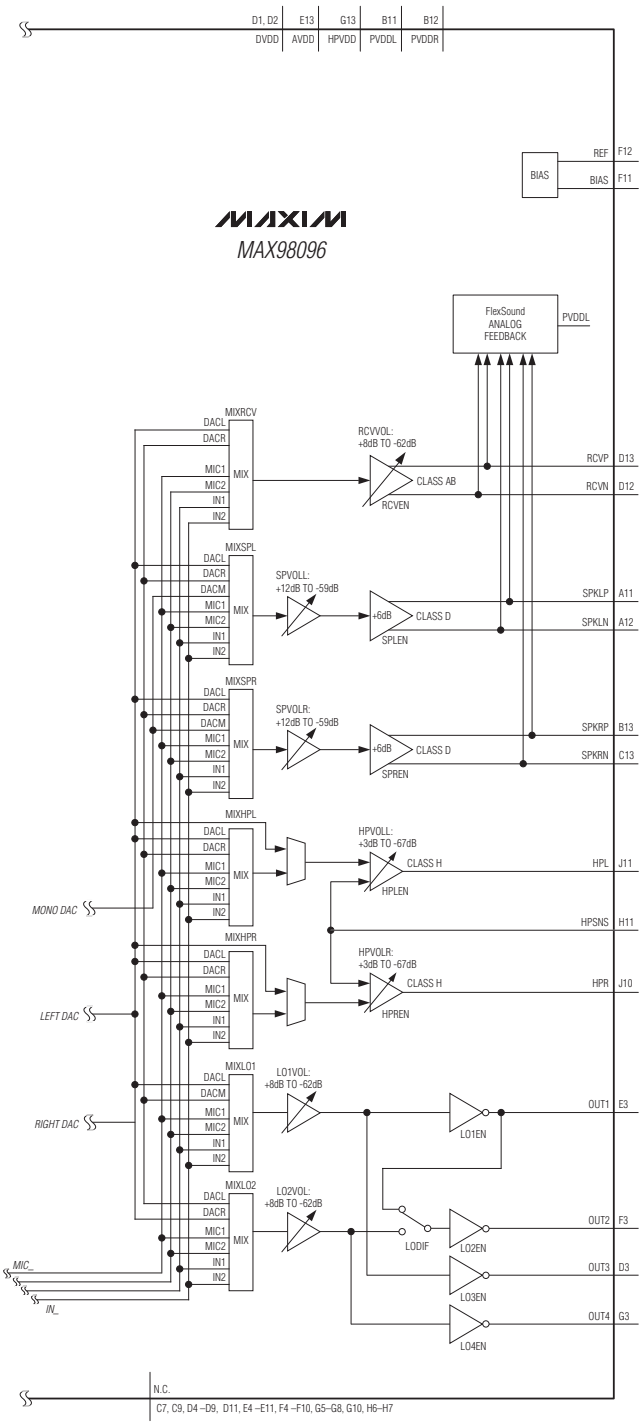
Functional Diagram (3 of 3)



ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND unless otherwise noted.)
DVDD, AVDD, HPVDD, CPVDD ..... -0.3V to +2.2V
HPVDD ..... (V_{AVDD} - 0.1V) to (V_{AVDD} + 0.1V)
PVDDL, PVDDR, DVDDA, DVDDB, DVDDC ..... -0.3V to +6.0V
DGND, HPGND, PGNDL, PGNDR ..... -0.1V to +0.1V
PVDDL to PVDDR ..... -0.1V to +0.1V
CPVDD ..... (V_{HPGND} - 0.3V) to (V_{HPVDD} + 0.3V)
CPVSS ..... (V_{HPGND} - 2.2V) to (V_{HPGND} + 0.3V)
C1N ..... (V_{HPGND} - 0.3V) to (V_{HPGND} + 0.3V)
C1P ..... (V_{HPGND} - 0.3V) to (V_{HPVDD} + 0.3V)
MICBIAS1, MICBIAS2 ..... -0.3V to (V_{PVDDR} + 0.3V)
JACKSW ..... -2.2V to +6.0V
MCLK1, SDINA, SDINB, SDINC, SDA/MOSI, SCL/SCLK, $\overline{CS}$, $\overline{IRQ}$, EN, $\overline{I2CMODE}$ ..... -0.3V to +6.0V
LRCLKA, BCLKA, SDOUTA, ADDR/MISO ..... -0.3V to (V_{DVDDA} + 0.3V)
LRCLKB, BCLKB, SDOUTB, GPIO0, GPIO1, GPIO2, MCLK2/GPIO3 ..... -0.3V to (V_{DVDDB} + 0.3V)
LRCLKC, BCLKC, SDOUTC ..... -0.3V to (V_{DVDDC} + 0.3V)
BIAS, INA1, INA2, INB1, INB2, MIC3P, MIC3N ..... -0.3V to +2.2V
MIC1P/DMICDIN1, MIC1N/DMICCK1, MIC2P/DMICDIN2, MIC2N/DMICCK2 ..... -0.3V to (V_{AVDD} + 0.3V)
HPSNS ..... (V_{HPGND} - 0.3V) to (V_{HPGND} + 0.3V)
JACKSNS ..... -0.3 to MIN (V_{CPVSS} + 6V, PVDDL)
HPL, HPR ..... (V_{CPVSS} - 0.3V) to (V_{CPVDD} + 0.3V)
RCVP, RCVN, OUT1, OUT2, OUT3, OUT4 ..... -0.3V to (V_{PVDDR} + 0.3V)
SPKLP, SPKLN ..... (V_{PGNDL} - 0.3V) to (V_{PVDDL} + 0.3V)
SPKRP, SPKRN ..... (V_{PGNDR} - 0.3V) to (V_{PVDDR} + 0.3V)
REF, TEMPSNSP, TEMPSNSN ..... -0.3V to (V_{AVDD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
117-Bump WLP (derate 47.6mW/°C above +70°C) 3.64W
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range (Note 3)		Guaranteed by PSRR	V_{PVDDL}, V_{PVDDR}	2.7		5.5	V
			V_{AVDD}, V_{HPVDD}	1.65	1.8	2	
			V_{DVDD}	1.33	1.8	2	
			V_{DVDDA}, V_{DVDDB}, V_{DVDDC}	1.65		3.6	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Current (Note 4)	I_{VDD}	Mono full duplex, microphone input, receiver output, fs = 8kHz (Note 5)	Analog		2.5	4.2	mA
			Speaker		1.5	2.5	
			Digital		2.1	3	
		Low-power stereo DAC playback, headphone outputs (Note 5)	Analog		1.3	2.1	
			Speaker		0	0.02	
			Digital		1.95	3.3	
		Stereo full duplex, line inputs, speaker outputs (Note 5)	Analog		3.0	5.4	
			Speaker		2.8	4	
			Digital		5.6	7.2	
Shutdown Supply Current (Note 4)		T_A = +25°C, EN = 0V	Analog		0.4	2	µA
			Speaker		0.1	1	
			Digital		8	50	
		T_A = +25°C	Analog		0.9	3	µA
			Speaker		4	10	
			Digital		10.5	50	
REF Voltage					1.25		V
BIAS Voltage					V_{AVDD} x 7/16		V
MICROPHONE TO ADC PATH							
Dynamic Range (Note 6)	DR	f = 1kHz, $AV_{MICPRE\_}$ = 0dB		75	88		dB
Total Harmonic Distortion + Noise	THD+N	$AV_{MICPRE\_}$ = 0dB, V_{IN} = -10dBV			-77	-65	dB
		$AV_{MICPRE\_}$ = 20dB, V_{IN} = -30dBV, f = 1kHz			-82		
		$AV_{MICPRE\_}$ = +30dB, V_{IN} = -40dBV, f = 1kHz			-71		
Common-Mode Rejection Ratio	CMRR	V_{IN} = -30dBV, f = 217Hz			65		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 2.0V, input referred, MIC inputs unconnected		50	60		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, input referred			60		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, input referred			60		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, input referred			55		
Absolute Gain Accuracy		DC accuracy (Note 7)		-1.5	0	+1	dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from analog input to digital output	MODE = 0 (IIR voice) 8kHz		2.2		ms
			MODE = 0 (IIR voice) 16kHz		1.1		
			MODE = 1 (FIR music) 8kHz		4.5		
			MODE = 1 (FIR music) 48kHz		0.76		
DIGITAL MICROPHONE PATH							
Dynamic Range (Note 6)	DR	f = 1kHz, f_S = 8kHz, $AV_{ADCGAIN}$ = AV_{ADCLVL} = 0dB	MCLK = 12.288MHz		90		dB
			MCLK = 13MHz		90		
		f = 1kHz, f_S = 24kHz, $AV_{ADCGAIN}$ = AV_{ADCLVL} = 0dB	MCLK = 12.288MHz		90		
			MCLK = 13MHz		90		
		f = 1kHz, f_S = 48kHz, $AV_{ADCGAIN}$ = AV_{ADCLVL} = 0dB	MCLK = 12.288MHz		90		
			MCLK = 13MHz		90		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, f_S = 8kHz, $AV_{ADCGAIN}$ = AV_{ADCLVL} = 0dB	MCLK = 12.288MHz		-85		dB
			MCLK = 13MHz		-75		
		f = 1kHz, f_S = 24kHz, $AV_{ADCGAIN}$ = AV_{ADCLVL} = 0dB	MCLK = 12.288MHz		-80		
			MCLK = 13MHz		-75		
		f = 1kHz, f_S = 48kHz, $AV_{ADCGAIN}$ = AV_{ADCLVL} = 0dB	MCLK = 12.288MHz		-72		
			MCLK = 13MHz		-72		
Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from analog input to digital output	MODE = 0 (IIR voice) 8kHz		2.2		ms
			MODE = 0 (IIR voice) 16kHz		1.1		
			MODE = 1 (FIR music) 8kHz		4.5		
			MODE = 1 (FIR music) 48kHz		0.76		
MICROPHONE TO LINE OUT PATH							
Dynamic Range (Note 6)	DR	f = 1kHz, $AV_{MICPRE\_}$ = 0dB		80	93		dB
Total Harmonic Distortion + Noise	THD+N	$AV_{MICPRE\_}$ = 0dB, V_{IN} = -10dBV, f = 1kHz			-80	-65	
Absolute Gain Accuracy		DC accuracy (Note 7)		-1.5	0	+1	dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MICROPHONE PREAMP							
Input Range	V_{IN}	$AV_{MICPRE\_}$ = 0dB			1.4		V_{P-P}
		$AV_{MICPRE\_}$ = 20dB			0.14		
		$AV_{MICPRE\_}$ = 30dB			0.045		
Preamplifier Gain	$AV_{MICPRE\_}$	(Note 8)	PA1EN/PA2EN = 01		0		dB
			PA1EN/PA2EN = 10	19.5	20	20.5	
			PA1EN/PA2EN = 11	29.4	30	30.5	
PGA Gain	$AV_{MICPGA\_}$	$AV_{MICPRE\_}$ = 0dB (Note 8)	PGAM1/PGAM2 = 0x00	19.5	20	20.5	dB
			PGAM1/PGAM2 = 0x14		0		
MIC Input Resistance	R_{IN_MIC}	All gain settings, measured at MIC1P/MIC1N/MIC2P/MIC2N/MIC3P/MIC3N		6.5	10		kΩ
MICROPHONE BIAS							
MICBIAS Output Voltage	$V_{MICBIAS}$	I_{LOAD} = 1mA, MIC_BIAS_ = 00		2.14	2.2	2.25	V
		I_{LOAD} = 1mA, MIC_BIAS_ = 01		2.33	2.4	2.45	
		I_{LOAD} = 1mA, MIC_BIAS_ = 10		2.53	2.6	2.66	
		I_{LOAD} = 1mA, MIC_BIAS_ = 11		2.72	2.8	2.87	
Load Regulation		MIC_BIAS_ = 00			0.8	11	mV/mA
Line Regulation		V_{PVDDR} = 2.7V to 5.5V, MIC_BIAS_ = 00		70	82		dB
Ripple Rejection		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}			92		dB
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}			83		
Noise Voltage		A-weighted, f = 20Hz–20kHz			3.8		µV_{RMS}
LINE INPUT TO ADC PATH							
Dynamic Range (Note 6)	DR	MODE = 1 (FIR audio)			96		dB
Total Harmonic Distortion + Noise	THD+N	V_{IN} = -10dBV, f = 1kHz			-80		dB
Absolute Gain Accuracy		DC accuracy (Note 6)		-1	0	+1	dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINE INPUT AMPLIFIER							
Level Adjust Gain	$AV_{PGAIN\_}$	T_A = +25°C, (Note 7)	PGAIN = 0x0	19	20	21	dB
			PGAIN = 0x1	13	14	15	
			PGAIN = 0x2	2	3	4	
			PGAIN = 0x3		0		
			PGAIN = 0x4	-4	-3	-2	
			PGAIN = 0x5, 0x6, 0x7	-1	0	+1	
Input Range	V_{IN}	$AV_{PGAIN\_}$ = +20dB			0.14		V_{P-P}
		$AV_{PGAIN\_}$ = +14dB			0.28		
		$AV_{PGAIN\_}$ = +3dB			1		
		$AV_{PGAIN\_}$ = 0dB			1.4		
		$AV_{PGAIN\_}$ = -3dB			2		
Input Resistance	R_{IN}	$AV_{PGAIN\_}$ = +20dB		7.3	10	13.7	kΩ
		$AV_{PGAIN\_}$ = +14dB			10		
		$AV_{PGAIN\_}$ = +3dB			10		
		$AV_{PGAIN\_}$ = 0dB		7.3	10	13.7	
		$AV_{PGAIN\_}$ = -3dB			10		
Feedback Resistance	R_{IN_FB}	INEXT = 1	T_A = +25°C	18.5	20	21.5	kΩ
			T_A = T_{MIN} to T_{MAX}	17		23	
ADC LEVEL CONTROL							
ADC Conversion Gain	AV_{ADCVFS}				0.707		V/FFS
ADC Level Adjust Range	AV_{ADCLVL}	AVL/AVR = 0xF to 0x0 (Note 8)		-12		3	dB
ADC Level Adjust Step Size					1		dB
ADC Gain Adjust Range	$AV_{ADCGAIN}$	AVLG/AVRG = 00 to 11 (Note 8)		0		18	dB
ADC Gain Adjust Step Size					6		dB
ADC DIGITAL FILTERS							
VOICE MODE IIR LOWPASS FILTER (MODE_ = 0)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff		0.441 x f_S			Hz
		-3dB cutoff		0.449 x f_S			
Passband Ripple		f < f_{PLP}		-0.1		0.1	dB
Stopband Cutoff	f_{SLP}					0.47 x f_S	Hz
Stopband Attenuation (Note 9)		f > f_{SLP}		74			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOICE MODE IIR HIGHPASS FILTER (MODE_ = 0)						
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1 (elliptical tuned for f_S = 16kHz + 217Hz notch)			0.0161 x f_S	Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)			0.0319 x f_S	
		AVFLT = 0x3 (elliptical tuned for f_S = 8kHz + 217Hz notch)			0.0321 x f_S	
		AVFLT = 0x4 (500Hz Butterworth tuned for fs = 8kHz)			0.0632 x f_S	
		AVFLT = 0x5 (f_S/240 Butterworth)			0.0043 x f_S	
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (elliptical tuned for f_S = 16kHz + 217Hz notch)	0.0139 x f_S			Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)	0.0156 x f_S			
		AVFLT = 0x3 (elliptical tuned for f_S = 8kHz + 217Hz notch)	0.0279 x f_S			
		AVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)	0.0312 x f_S			
		AVFLT = 0x5 (f_S/240 Butterworth)	0.0018 x f_S			
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
AUDIO MODE FIR LOWPASS FILTER (MODE_ = 1, DHF1 = 0, LRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.48 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation (Note 9)		f < f_{SLP}	60			dB
ADC AUDIO MODE FIR LOWPASS FILTER (MODE_ = 1, DHF1 = 1, LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.208 x f_S			Hz
		-3dB cutoff	0.28 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		0.1	dB
Stopband Cutoff	f_{SLP}				0.417 x f_S	Hz
Stopband Attenuation		f < f_{SLP}	60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC AUDIO MODE DC BLOCKING HIGHPASS FILTER (MODE_ = 1)							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT ≠ 000				0.000125 x f_S	Hz
DC Attenuation	DC_{Atten}	AVFLT ≠ 000			90		dB
ADC TO DAC DIGITAL SIDETONE (MODE_ = 0)							
Sidetone Gain Adjust Range	AV_{STGA}	DVST = 0x01			-0.5		dB
		DVST = 0x1F			-60.5		
Sidetone Gain Adjust Step Size					2		dB
Sidetone Path Phase Delay		1kHz, 0dB input, highpass filter disabled	8kHz		2.2		ms
			16kHz		1.1		
ADC TO DAC DIGITAL LOOP-THROUGH PATH							
Dynamic Range (Note 6)	DR	f = 1kHz, MODE = 1 (FIR audio)		80	91		dB
Total Harmonic Distortion	THD	f = 1kHz, MODE = 1 (FIR audio)			-71	-66	dB
SAMPLE RATE CONVERTER							
Dynamic Range (Note 5)	DR	f = 1kHz		88	95		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz		-60			dB
DAC LEVEL CONTROL							
DAC Conversion Gain	AV_{DACVFS}				1		V/FFS
DAC Attenuation Range	$AV_{DACATTN}$	DV1\DV2 = 0xF to 0x0 (Note 8)		-15		0	dB
DAC Attenuation Step Size					1		dB
DAC Gain Adjust Range	$AV_{DACGAIN}$	DV1G = 00 to 11 (Note 8)		0		18	dB
DAC Gain Adjust Step Size					6		dB
DAC DIGITAL FILTERS							
VOICE MODE IIR LOWPASS FILTER (MODE_ = 0)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff		0.448 x f_S			Hz
		-3dB cutoff		0.451 x f_S			
Passband Ripple		f < f_{PLP}		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}					0.476 x f_S	Hz
Stopband Attenuation (Note 9)		f > f_{SLP}		75			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOICE MODE IIR HIGHPASS FILTER (MODE_ = 0)						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1 (elliptical tuned for f_S = 16kHz + 217Hz notch)			0.0161 x f_S	Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)			0.0312 x f_S	
		DVFLT = 0x3 (elliptical tuned for f_S = 8kHz + 217Hz notch)			0.0321 x f_S	
		DVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)			0.0625 x f_S	
		DVFLT = 0x5 (f_S/240 Butterworth)			0.0042 x f_S	
Stopband Cutoff (-30dB from Peak)	f_{DHPSB}	DVFLT = 0x1 (Elliptical tuned for f_S = 16kHz + 217Hz notch)	0.0139 x f_S			Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for f_S = 16kHz)	0.0156 x f_S			
		DVFLT = 0x3 (Elliptical tuned for f_S = 8kHz + 217Hz notch)	0.0279 x f_S			
		DVFLT = 0x4 (500Hz Butterworth tuned for f_S = 8kHz)	0.0312 x f_S			
		DVFLT = 0x5 (f_S/240 Butterworth)	0.0021 x f_S			
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000		90		dB
AUDIO MODE FIR LOWPASS FILTER (MODE_ = 1, DHF1/DHF2 = 0, TLRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.47 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		0.1	dB
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation (Note 9)		f > f_{SLP}	60			dB
AUDIO MODE FIR LOWPASS FILTER (MODE_ = 1, DHF1/DHF2 = 1 for LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.24 x f_S			Hz
		-3dB cutoff	0.31 x f_S			
Passband Ripple		f < f_{PLP}	-0.1		0.1	dB
Stopband Cutoff	f_{SLP}				0.477 x f_S	Hz
Stopband Attenuation (Note 9)		f < f_{SLP}	60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEREO AUDIO MODE DC BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT_ ≠ 000				0.000104 x f_S	Hz
DC Attenuation	DC_{Atten}	DVFLT_ ≠ 000			90		dB
AUTOMATIC LEVEL CONTROL							
Filter Order					2		
Gain Range				0		12	dB
Compression Ratio		ALCCMP_ = 000 to 011		1:1		∞:1	
Compression Threshold		ACLTHC_ = 0x1F to 0x00		-31		0	dBFS
Expansion Ratio		ALCEXP_ = 000 to 010		1:1		4:1	
Expansion Threshold		ALCTHE_ = 0x1F to 0x00		-66		-35	dBFS
Compression Attack Time		ALCATK_ = 000 to 111		0.5		200	ms
Compression Release Time		ALCRLS_ = 101 to 000		0.25		8	sec
Expansion Attack Time		ALCRLS_ = 101 to 000		0.25		8	sec
Expansion Release Time		ALCATK_ = 000 to 111		0.5		200	ms
PARAMETRIC EQUALIZER							
Number of Bands					5		Bands
Per Band Gain Range				-12		12	dB
Preattenuator Gain Range				-15		0	dB
Preattenuator Step Size					1		dB
FLEXSOUND PROGRAMMABLE DSP							
Maximum Clock Frequency		V_{DVDD} = 1.4V		40			MHz
		V_{DVDD} = 1.8V		100			
DAC TO RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 6)	DR	f_S = 48kHz, MCLK = 12.288MHz, f = 1kHz			96		dB
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 25mW, R_{RCV} = 32Ω			-70	-63	dB
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, AV_{REC} = 0dB	Into shutdown		-70		dBV
			Out of shutdown		-73		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Absolute Gain Accuracy		DC accuracy (Note 7)		-1	0	+1	dB
Mixer Gain		MIXRCVGAIN = 00			0		dB
		MIXRCVGAIN = 01			-6		
		MIXRCVGAIN = 10			-9		
		MIXRCVGAIN = 11			-12		
Power-Supply Rejection Ratio	PSRR	V_{PVDDR} = 2.7V to 5.5V		60	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}			75		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}			74		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}			74		
LINE INPUT TO RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 6)	DR	Referenced to full-scale output level			92		dB
				80			
Total Harmonic Distortion + Noise	THD+N				-70		dB
Power-Supply Rejection Ratio	PSRR	V_{PVDDR} = 2.7V to 5.5V		55	74		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}			70		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}			70		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}			58		
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, AV_{REC} = 0dB	Into shutdown		-57		dBV
			Out of shutdown		-55		
Absolute Gain Accuracy		DC accuracy (Note 7)		-1.5	0	+1	dB
Mixer Gain		MIXRCVGAIN = 00			+9		dB
		MIXRCVGAIN = 01			+3		
		MIXRCVGAIN = 10			0		
		MIXRCVGAIN = 11			-3		
RECEIVER AMPLIFIER							
Output Power	P_{OUT}	R_{REC} = 32Ω, f = 1kHz, THD = 1%			100		mW
Full-Scale Output		(Note 10)			1		V_{RMS}
Volume Control	AV_{REC}	(Note 8)	RCVVOL = 0x00		-58		dB
			RCVVOL = 0x1F	+7.5	+8	+8.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Volume Control Step Size		+8dB to +6dB			0.5		dB
		+6dB to +0dB			1		
		0dB to -14dB			2		
		-14dB to -38dB			3		
		-38dB to -62dB			4		
Mute Attenuation		f = 1kHz			95		dB
Output Offset Voltage	V_{OS}	AV_{REC} = -62dB, T_A = +25°C			±0.13	±3	mV
Capacitive Drive Capability		No sustained oscillations	R_{REC} = 32Ω		500		pF
			R_{REC} = ∞		100		
DAC TO SPEAKER AMPLIFIER PATH							
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 500mW, Z_{SPK} = 8Ω + 68µH			-71		dB
						-50	
Crosstalk		SPL to SPR and SPR to SPL, unloaded, f = 1kHz			-104		dB
		SPL to SPR and SPR to SPL, P_{OUT} = 640mW, f = 1kHz			-75		
Output Noise					43		$µV_{RMS}$
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{SPK\_}$ = 0dB	Into shutdown		-65		dBV
			Out of shutdown		-65		
Absolute Gain Accuracy		DC accuracy (Note 7)		5	6	7	dB
Mixer Gain		MIXSP_GAIN = 00			0		dB
		MIXSP_GAIN = 01			-6		
		MIXSP_GAIN = 10			-9		
		MIXSP_GAIN = 11			-12		
Power-Supply Rejection Ratio	PSRR	V_{PVDDL} = V_{PVDDR} = 2.7V to 5.5V		50	70		dB
		f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$			62		
		f = 1kHz, V_{RIPPLE} = $100mV_{P-P}$			62		
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$			60		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINE INPUT TO SPEAKER AMPLIFIER PATH							
Dynamic Range (Note 6)	DR	Referenced to full-scale output level	AVSPK_= 0dB		87		dB
				80			
			AVSPK_= +8dB		88.5		
Output Noise					56		μV_{RMS}
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 200mW, R_L = 8Ω + 68µH			-66		dB
Power-Supply Rejection Ratio	PSRR	V_{PVDDL} = V_{PVDDR} = 2.7V to 5.5V		50	60		dB
		f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$			75		
		f = 1kHz, V_{RIPPLE} = $100mV_{P-P}$			73		
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$			50		
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{SPK\_}$ = 0dB	Into shutdown		-48		dBV
			Out of shutdown		-50		
Absolute Gain Accuracy		DC accuracy (Note 7)		4.5	6	7	dB
Mixer Gain		MIXSP_GAIN = 00			+9		dB
		MIXSP_GAIN = 01			+3		
		MIXSP_GAIN = 10			0		
		MIXSP_GAIN = 11			-3		
SPEAKER AMPLIFIER							
Output Power	P_{OUT}	f = 1kHz, THD = 10%, Z_{SPK} = 4Ω + 33µH	V_{PVDDL} = V_{PVDDR} = 5.0V		3.2		W
			V_{PVDDL} = V_{PVDDR} = 4.2V		2		
			V_{PVDDL} = V_{PVDDR} = 3.7V		1.4		
		f = 1kHz, THD = 1%, Z_{SPK} = 4Ω + 33µH	V_{PVDDL} = V_{PVDDR} = 5.0V		2.4		
			V_{PVDDL} = V_{PVDDR} = 4.2V		1.6		
			V_{PVDDL} = V_{PVDDR} = 3.7V		1		
		f = 1kHz, THD = 10%, Z_{SPK} = 8Ω + 68µH	V_{PVDDL} = V_{PVDDR} = 5.0V		1.7		
			V_{PVDDL} = V_{PVDDR} = 4.2V		1.2		
			V_{PVDDL} = V_{PVDDR} = 3.7V		0.9		
		f = 1kHz, THD = 1%, Z_{SPK} = 8Ω + 68µH	V_{PVDDL} = V_{PVDDR} = 5.0V		1.4		
			V_{PVDDL} = V_{PVDDR} = 4.2V		0.95		
			V_{PVDDL} = V_{PVDDR} = 3.7V		0.7		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Scale Output		(Note 10)			2		V_{RMS}
Volume Control	$AV_{SPK\_}$	(Note 8)	SPVOLL/SPVOLR = 0x00		-59		dB
			SPVOLL/SPVOLR = 0x27	-11.5	+12	+12.5	
Volume Control Step Size		+12dB to +6dB			0.5		dB
		+6dB to -3dB			1		
		-3dB to -19dB			2		
		-19dB to -59dB			4		
Mute Attenuation		f = 1kHz			86		dB
Output Offset Voltage	V_{OS}	$AV_{SPK\_}$ = -59dB, T_A = +25°C			±0.25	±3	mV
Switching Frequency	f_{SW}				300		kHz
DAC TO HEADPHONE AMPLIFIER PATH							
Dynamic Range (Note 6)	DR	f_S = 48kHz, MCLK = 12.288MHz, T_A = +25°C	High-performance mode	94	102		dB
			Low-power mode	92	100		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 20mW	R_{HP} = 16Ω		-80	-72	dB
			R_{HP} = 32Ω		-80		
		f = 1kHz, V_{OUT} = $1V_{RMS}$, R_{HP} = 10kΩ			-85		
Crosstalk		f = 1kHz, input = -1dBFS, R_{HP} = 10kΩ			-106		dB
		HPL to HPR and HPR to HPL, P_{OUT} = 5mW, f = 1kHz, R_{HP} = 32Ω			-100		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{HPVDD} = 1.65V to 2.0V		50	70		dB
		f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$, AV_{VOL} = 0dB			85		
		f = 1kHz, V_{RIPPLE} = $100mV_{P-P}$, AV_{VOL} = 0dB			85		
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$, AV_{VOL} = 0dB			75		
DAC Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from digital input to analog output	MODE_ = 0 (voice) 8kHz		2.2		ms
			MODE_ = 0 (voice) 16kHz		1.1		
			MODE_ = 1 (music) 8kHz		4.5		
			MODE_ = 1 (music) 48kHz		0.76		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Absolute Gain Accuracy		DC accuracy (Note 7)		-1	0	+1	dB
Channel Gain Mismatch					0.5		%
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{HP\_}$ = 0dB	Into shutdown		-66		dBV
			Out of shutdown		-67		
Mixer Gain		MIXHP_GAIN = 00			0		dB
		MIXHP_GAIN = 01			-6		
		MIXHP_GAIN = 10			-9		
		MIXHP_GAIN = 11			-12		
LINE INPUT TO HEADPHONE AMPLIFIER PATH							
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $1V_{P-P}$, f = 1kHz, R_L = 32Ω			-70		dB
Dynamic Range (Note 6)					91		dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{HPVDD} = 1.65V to 2.0V		42	66		dB
		f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$			62		
		f = 1kHz, V_{RIPPLE} = $100mV_{P-P}$			57		
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$			41		
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, $AV_{HP\_}$ = 0dB	Into shutdown		-62		dBV
			Out of shutdown		-60		
Absolute Gain Accuracy		DC accuracy (Note 7)		-1.5	0	+1	dB
Mixer Gain		MIXHP_GAIN = 00			+9		dB
		MIXHP_GAIN = 01			+3		
		MIXHP_GAIN = 10			0		
		MIXHP_GAIN = 11			-3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HEADPHONE AMPLIFIER							
Output Power	P_{OUT}	f = 1kHz, THD = 1	R_L = 32Ω		33		mW
			R_L = 16Ω		40		
Full-Scale Output		(Note 10)			1		V_{RMS}
Volume Control	$AV_{HP\_}$	(Note 8)	HPVOL_ = 0x00	-69	-67	-65	dB
		T_A = +25°C	HPVOL_ = 0x1F	+2.5	+3	+3.5	
Volume Control Step Size		+3dB to +1dB			0.5		dB
		+1dB to -5dB			1		
		-5dB to -19dB			2		
		-19dB to -43dB			3		
		-43dB to -67dB			4		
Mute Attenuation		f = 1kHz			108		dB
Output Offset Voltage	V_{OS}	$AV_{HP\_}$ = -67dB	T_A = +25°C		±0.2	±1	mV
			T_A = T_{MIN} to T_{MAX}			±2	
Capacitive Drive Capability		No sustained oscillations	R_{HP} = 32Ω		500		pF
			R_{HP} = ∞		100		
CHARGE PUMP							
Charge-Pump Frequency		V_{HPL} = V_{HPR} = 0V			82.5		kHz
		V_{HPL} = V_{HPR} = 0.2V			667		
		V_{HPL} = V_{HPR} = 0.5V			500		
Positive Output Voltage	V_{HPVDD}	V_{OUT} > V_{TH}			V_{HPVDD}		V
		V_{OUT} < V_{TH}			V_{HPVDD}/2		
Negative Output Voltage	V_{HPVSS}	V_{OUT} > V_{TH}			-V_{HPVDD}		V
		V_{OUT} < V_{TH}			-V_{HPVDD} /2		
Output Voltage Threshold	V_{TH}	Output voltage at which the charge pump switches modes, V_{OUT} rising or falling			±V_{HPVDD} x 0.25		V
Mode Transition Timeouts		Time it takes for the charge pump to transition from Invert to split mode			32		ms
		Time it takes for the charge pump to transition from split to invert mode			20		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPEAKER AND HEADPHONE EXPANDER						
Minimum Attack Time		Duration required for noise gate to adjust from 0dB attenuation to 12dB attenuation		0.25		s
Maximum Attack Time		Duration required for noise gate to adjust from 0dB attenuation to 12dB attenuation		8		s
Release Time		Time constant of the release time's exponential response		10		ms
Expansion Ratio	EXP_{RATIO}	The actual PGA settings is determined by [EXP_{TH}(dB) - V_{DAC}(dBFS)]/EXP_{RATIO}		0.75		dB/step
Threshold Level	EXP_{TH}		-72		-30	dB
Threshold Step Size				3		dB
Attenuation Range			0		12	dB
DAC TO LINE OUTPUTS						
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, V_{OUT} = -3dBFS, R_L = 10kΩ		-75	-70	dB
Dynamic Range (Notes 6, 9)	DR	AV_{LO} = 0dB		97		dB
Power-Supply Rejection Ratio (Note 9)	PSRR	V_{PVDDR} = 2.7V to 5.5V	66	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{LO} = 0dB		70		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{LO} = 0dB		60		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{LO} = 0dB		50		
Full-Scale Output		AV_{LO} = 0dB, LODIF= 0		1		V_{RMS}
		AV_{LO} = 0dB, LODIF= 1		2		
Absolute Gain Accuracy		DC accuracy (Note 7)	-1	0	+1	dB
Mixer Gain		MIXLO_GAIN = 00		0		dB
		MIXLO_GAIN = 01		-6		
		MIXLO_GAIN = 10		-9		
		MIXLO_GAIN = 11		-12		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINE INPUT TO LINE OUTPUTS						
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, V_{OUT} = -3dBFS, R_L = 10kΩ		-75		dB
Dynamic Range (Notes 6, 9)	DR	AV_{LO}=0dB		94		dB
Absolute Gain Accuracy		DC accuracy (Note 7)	-1.5	0	+1	dB
Mixer Gain		MIXLO_GAIN = 00		+9		dB
		MIXLO_GAIN = 01		+3		
		MIXLO_GAIN = 10		0		
		MIXLO_GAIN = 11		-3		
Power-Supply Rejection Ratio (Note 9)	PSRR	V_{PVDDR} = 2.7V to 5.5V	66	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{LO} = 0dB		70		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{LO} = 0dB		60		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{LO} = 0dB		50		
LINE OUTPUT AMPLIFIER						
Volume Control	AV_{RCV}	LO_VOL = 0x00		-59		dB
		LO_VOL = 0x1F	+7.5	+8	+8.5	
Volume Control Step Size		+8dB to +6dB		0.5		dB
		+6dB to -0dB		1		
		0dB to -14dB		2		
		-14dB to -38dB		3		
		-38dB to -62dB		4		
Mute Attenuation		f = 1kHz		100		dB
		f = 20Hz–20kHz	60			
Output Impedance	R_{OUT}		200	295	390	Ω
Common-Mode Bias		LO_VCM = 0		1.5		V
		LO_VCM = 1		1.25		
Capacitive Drive Capability		No sustained oscillations		400		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JACK DETECTION							
Microphone Impedance (Note 10)	Z_{MIC}	TTYTH = 00		2	2.7	3.5	kΩ
		TTYTH = 01		2.4	3.2	4.2	
		TTYTH = 10		3	3.8	5.3	
		TTYTH = 11		3.6	4.7	6.3	
TTY Device Impedance		TTYTH = 00		0.5		2	kΩ
		TTYTH = 01		0.5		2.4	
		TTYTH = 10		0.5		3	
		TTYTH = 11		0.5		3.6	
Video Cable Removal Detection Thresholds		V_{REMTH} = 00		0.585 x V_{HPVDD}	0.61 x V_{HPVDD}	0.635 x V_{HPVDD}	kΩ
		V_{REMTH} = 01		0.675 x V_{HPVDD}	0.7 x V_{HPVDD}	0.725 x V_{HPVDD}	
		V_{REMTH} = 10		0.775 x V_{HPVDD}	0.8 x V_{HPVDD}	0.825 x V_{HPVDD}	
		V_{REMTH} = 11		0.825 x V_{HPVDD}	0.85 x V_{HPVDD}	0.875 x V_{HPVDD}	
DC Ramp Test Slew Time	t_{DCTST}	DCSLEW = 0x00			4		ms
		DCSLEW = 0xFF			1024		
DC Coupled Headphone Impedance	Z_{HP}					600	Ω
Line Audio Load Impedance	Z_{ALLI}	T_A = +25°C		2		47	kΩ
AC-Coupling Capacitance	C_{AC}				1		µF
Video Load Impedance	Z_{VL}				75		Ω
JACKSNS Weak Pullup Resistance				75	105	140	kΩ
JACKSW Weak Pullup Resistance					450		kΩ
KEYPRESS ADC							
ADC Clock Frequency	f_{ADC}	10 cycles per conversion			100		kHz
ADC Trip Level	V_{TRIP}	Coarse and fine ranges, automatic			0.29 x MICBIAS2		V
ADC Coarse Range		LSB = 10mV	Maximum		0.29 x V_{ADCREF}		V
			Minimum		0.09 x V_{ADCREF}		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Fine Range		LSB = 2mV	Maximum		0.09 x VADCREF		V
			Minimum		0		
ADC Debounce Time	t_{DEB}	KEY_DEB = 0x00 to 0xFF		1		256	ms
ADC Delay Time	t_{DEL}	KEY_DEL = 0x00 to 0xFF, time from when conversion is completed to when $\overline{IRQ}$ goes low		4		1024	ms
SPEAKER OUTPUT VOLTAGE ADC							
Sample Rate	f_S			46.6	48	49.44	kHz
Signal to Noise Ratio	SNR			45			dB
Gain Error	A_V					±0.5	%
Full-Scale Range		VPVDDL = VPVDDR = 5.5V			5.5		VP
TEMPERATURE ADC							
Sample Rate	f_S				0.1		Hz
Temperature Resolution					1		°C
Absolute Accuracy					±3.5		°C
Temperature Range		Guaranteed by absolute accuracy		-40		+125	°C
BATTERY ADC							
Full-Scale Range		Maximum			5.5		V
		Minimum			2.5		
Resolution					50		mV
INL	INLB					16	LSB
DNL	DNLB					16	LSB
Gain Error						6	%

DIGITAL INPUTS/OUTPUTS CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK1						
Input High Voltage	V_{IH}		0.7 x V_{DVDDA}			V
Input Low Voltage	V_{IL}				0.29 x V_{DVDDA}	V
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDA} = 3.6V, V_{IN} = 0V, 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
GPIO0, GPIO1, GPIO2, MCLK2/GPIO3—INPUT						
Input High Voltage	V_{IH}		0.75 x V_{DVDDB}			V
Input Low Voltage	V_{IL}				0.25 x V_{DVDDB}	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDB} = 3.6V, V_{IN} = 0V, 3.6V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
GPIO0, GPIO1, GPIO2, MCLK2/GPIO3—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDB} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDB} = 1.65V, I_{OH} = 3mA	V_{DVDDB} - 0.4			V
SDINA, BCLKA, LRCLKA, $\overline{CS}$, $\overline{I2CMODE}$						
Input High Voltage	V_{IH}		0.7 x V_{DVDDA}			V
Input Low Voltage	V_{IL}				0.29 x V_{DVDDA}	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDA} = 3.6V, V_{IN} = 0V, 3.6V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF

DIGITAL INPUTS/OUTPUTS CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BCLKA, LRCLKA, SDOUTA, ADDR/MISO—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDA} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDA} = 1.65V, I_{OH} = 3mA	V_{DVDDA} - 0.4			V
Output Leakage Current	I_{IH}, I_{IL}	V_{DVDDA} = 3.6V, V_{IN} = 0V, 3.6V, T_A = +25°C, high-impedance state	-1		+1	µA
SDINB/TRST, BCLKB, LRCLKB—INPUT						
Input High Voltage	V_{IH}		0.7 x V_{DVDDB}			V
Input Low Voltage	V_{IL}				0.29 x V_{DVDDB}	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDB} = 3.6V, V_{IN} = 0V, 3.6V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
BCLKB, LRCLKB, SDOUTB—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDB} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDB} = 1.65V, I_{OH} = 3mA	V_{DVDDB} - 0.4			V
Output Leakage Current	I_{IH}, I_{IL}	V_{DVDDB} = 3.6V, V_{IN} = 0V, 3.6V, T_A = +25°C, high-impedance state	-1		+1	µA
SDINC/TDI, BCLKC/TMS, LRCLKC/TCK—INPUT						
Input High Voltage	V_{IH}		0.7 x V_{DVDDC}			V
Input Low Voltage	V_{IL}				0.29 x V_{DVDDC}	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDDC} = 3.6V, V_{IN} = 0V, 3.6V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF

DIGITAL INPUTS/OUTPUTS CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BCLKC/TMS, LRCLKC/TCK, SDOUTC/TDO—OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDDC} = 1.65V, I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDDC} = 1.65V, I_{OH} = 3mA	V_{DVDDC} - 0.4			V
Output Leakage Current	I_{IH}, I_{IL}	V_{DVDDC} = 3.6V, V_{IN} = 0V, 3.6V, T_A = +25°C, high-impedance state	-1		+1	µA
ADDR/MISO INPUT						
Input High Voltage	V_{IH}		0.7 x V_{AVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{AVDD}	V
Input Hysteresis				210		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{AVDD} = 1.65V, V_{IN} = 0V, 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
EN INPUT						
Input High Voltage	V_{IH}		1.35			V
Input Low Voltage	V_{IL}				0.5	V
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V, 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
SDA/MOSI, SCL/SCLK INPUT						
Input High Voltage	V_{IH}	$\overline{I2CMODE}$ = 0	0.7 x V_{AVDD}			V
		$\overline{I2CMODE}$ = 1	0.7 x V_{DVDDA}			
Input Low Voltage	V_{IL}	$\overline{I2CMODE}$ = 0			0.3 x V_{AVDD}	V
		$\overline{I2CMODE}$ = 1			0.29 x V_{DVDDA}	
Input Hysteresis				210		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{AVDD} = 1.65V, V_{IN} = 0V, 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF

DIGITAL INPUTS/OUTPUTS CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA/MOSI, $\overline{IRQ}$—OUTPUT						
Output High Current	I_{OH}	V_{OUT} = 5.5V, T_A = +25°C			1	µA
Output Low Voltage	V_{OL}	V_{AVDD} = 1.65V, I_{OL} = 3mA			0.2 x V_{AVDD}	V
MIC1N/DMICDIN1, MIC2N/DMICDIN2 INPUT						
Input High Voltage	V_{IH}		0.65 x V_{AVDD}			V
Input Low Voltage	V_{IL}				0.35 x V_{AVDD}	V
Input Hysteresis				125		mV
Input Leakage Current	I_{IH}, I_{IL}	V_{DVDD} = 2.0V, V_{IN} = 0V, 2.0V, T_A = +25°C	-36		+36	µA
Input Capacitance				10		pF
DIGMICCLK1/2 - OUTPUT						
Output Low Voltage	V_{OL}	V_{DVDD} = 1.65V, I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	V_{DVDD} = 1.65V, I_{OH} = 1mA	V_{AVDD} - 0.4			V
SCLK Clock Period	t_{CP}	Guaranteed by SCL pulse-width low and high	40			ns
SCLK Pulse-Width Low	t_{CL}		18			ns
SCLK Pulse-Width High	t_{CH}		18			ns
Setup Time	t_{CSS}		20			ns
Hold Time	t_{CSH}		20			ns
Minimum Pulse-Width High	t_{CSW}		20			ns
DIN Setup Time	t_{DS}		5			ns
DIN Hold Time	t_{DH}		5			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD} = 50pF	5	9	13	ns
Output Data Enable Time	t_{DEN}				5	ns
Output Data Disable Time	t_{DZ}				5	ns

INPUT CLOCK CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC} = +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK Input Frequency	f_{MCLK}		10		60	MHz
MCLK Input Duty Cycle		PSCLK = 01	40	50	60	%
		PSCLK = 10 or 11	30		70	
Maximum MCLK Input Jitter		No performance degradation		50		ppm
LRCLK Sample Rate (Note 12)		DHF_ = 0	8		48	kHz
		DHF_ = 1	48		96	
DAI1 LRCLK Average Frequency Error (Note 13)		FREQ1 = 0x8 to 0xF	0		0	%
		FREQ1 = 0x0	-0.025		+0.025	
DAI2 LRCLK Average Frequency Error (Note 13)			-0.025		+0.025	%
PLL Lock Time		Rapid-lock mode		2	7	ms
		Nonrapid lock mode		12	25	
Maximum LRCLK Jitter to Maintain PLL Lock					±100	ns
Soft-Start/Stop Time				10		ms

DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line Output Loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BCLK Cycle Time	t_{BCLK}	Slave mode		90			ns
BCLK High Time	t_{BCLKH}	Slave mode		20			ns
BCLK Low Time	t_{BCLKL}	Slave mode		20			ns
BCLK or LRCLK Rise and Fall Time	t_r, t_f	Master mode, C_L = 15pF			5		ns
SDIN to BCLK Setup Time	t_{SETUP}			20			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$	Slave mode		20			ns
SDIN to BCLK Hold Time	t_{HOLD}			20			ns
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$	Slave mode		20			ns
Minimum Delay Time from LSB BCLK Falling Edge to High-Impedance State	t_{HIZOUT}	Master mode	TDM_ = 1, FSW_ = 1		42		ns
			TDM_ = 1, FSW_ = 0		42		
LRCLK Rising Edge to SDOUT MSB Delay	t_{SYNCTX}	C_L = 30pF, TDM_ = 1, FSW_ = 1				56	ns
BCLK to SDOUT Delay	t_{CLKTX}	C_L = 30pF	TDM_ = 1, BCLK rising edge			56	ns
			TDM_ = 0			50	ns
Delay Time from BCLK to LRCLK	$t_{CLKSYNC}$	Master mode	TDM_ = 1	-15		+15	ns
			TDM_ = 0			0.8 x t_{BCLK}	ns
Delay Time from LRCLK to BCLK after LSB	$t_{ENDSYNC}$	Master mode	TDM_ = 1, FSW_ = 1	20			ns

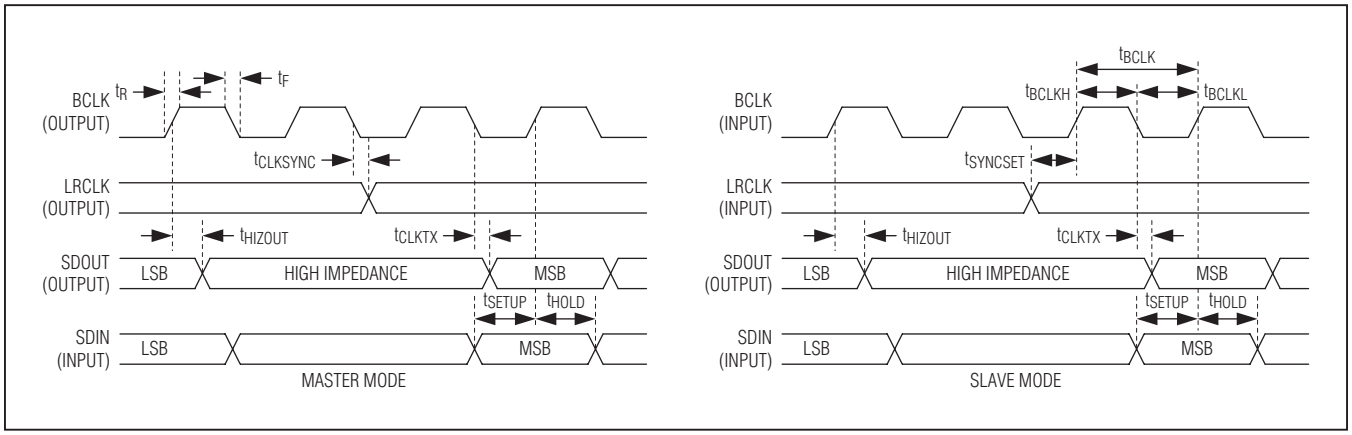


Figure 1. Non-TDM Audio Interface Timing Diagrams (TDM_ = 0)

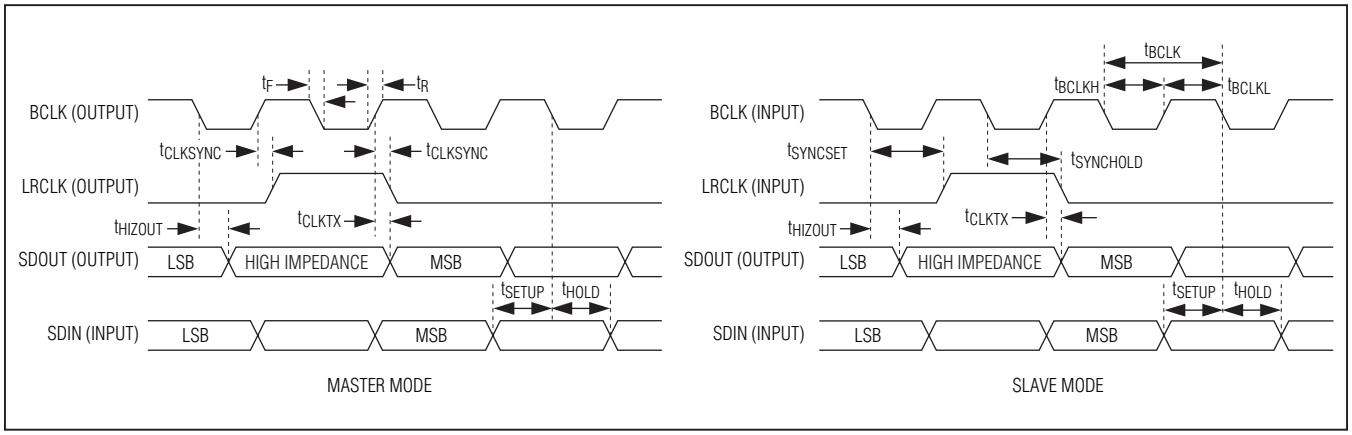


Figure 2. TDM Audio Interface Timing Diagram (TDM_ = 1, FSW_ = 0)

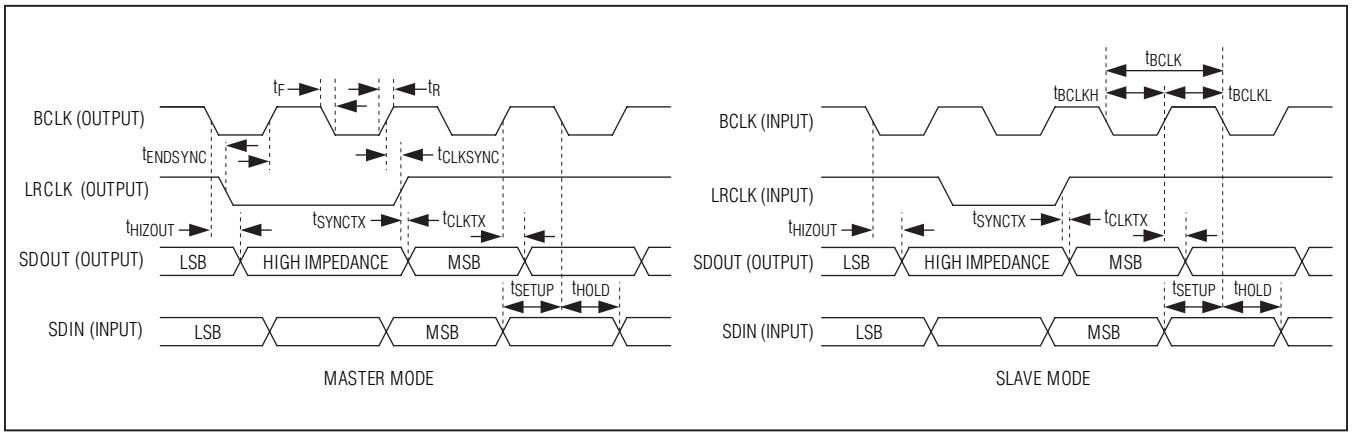


Figure 3. TDM Audio Interface Timing Diagram (TDM_ = 1, FSW_ = 1)

DIGITAL MICROPHONE TIMING CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC} = +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line Output Loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGMICCLK Frequency	f_{MICCLK}	MICCLK = 00		MCLK/8		MHz
		MICCLK = 01		MCLK/6		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU,MIC}$	Either clock edge	20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD,MIC}$	Either clock edge	0			ns

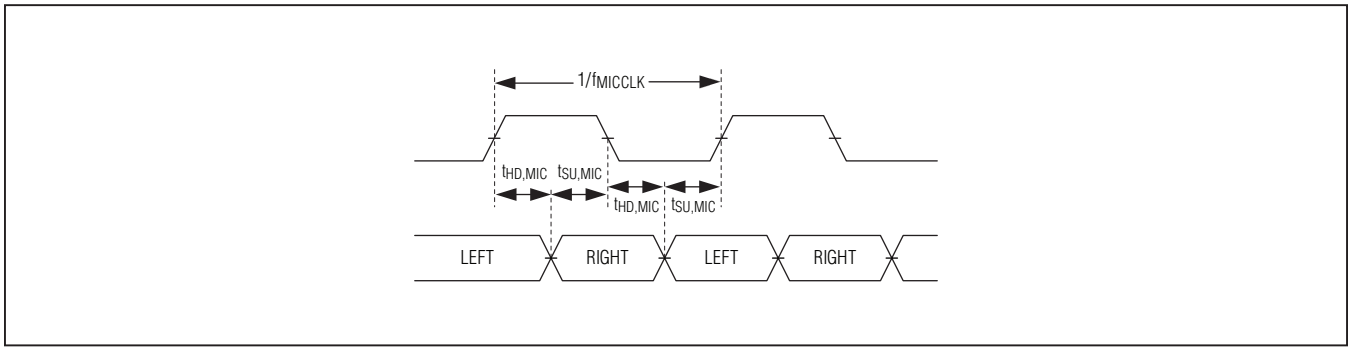


Figure 4. Digital Microphone Timing Diagram

I²C TIMING CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC} = +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line Output Loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}	Guaranteed by SCL pulse-width low and high	0		400	kHz
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
LOW period of the SCL clock	t_{LOW}		1.3			µs
HIGH period of the SCL clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	R_{PU} = 475Ω, C_B = 100pF, 400pF	0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 14)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 14)	20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Bus Capacitance	C_B	Guaranteed by SDA transmitting fall time			400	pF
SDA Transmitting Fall Time	t_F	RPU = 475Ω, C_B = 100pF, 400pF (Note 14)	20 + 0.05C_B		250	ns
Pulse Width of Suppressed Spike	t_{SP}				50	Ns

I²C TIMING CHARACTERISTICS (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC} = +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line Output Loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	tCP	Guaranteed by SCL pulse-width low and high	40			ns
SCLK Pulse-Width Low	tCL		18			ns
SCLK Pulse-Width High	tCH		18			ns
Setup Time	tCSS		20			ns
Hold Time	tCSH		20			ns
Minimum Pulse-Width High	tCSW		20			ns
DIN Setup Time	tDS		5			ns
DIN Hold Time	tDH		5			ns
Output Data Propagation Delay	tDO	C_{LOAD} = 50pF	5	9	13	ns
Output Data Enable Time	tDEN				5	ns
Output Data Disable Time	tDZ				5	ns

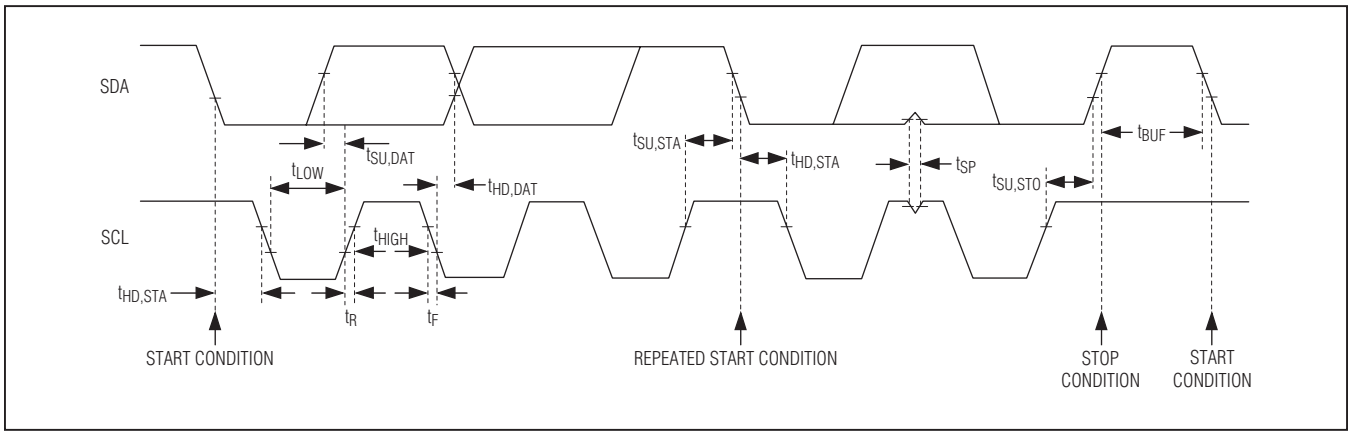


Figure 5. I²C Interface Timing Diagram

SPI TIMING CHARACTERISTICS

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are valid for T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}	Guaranteed by SCL pulse-width low and high	40			ns
SCLK Pulse-Width Low	t_{CL}		18			ns
SCLK Pulse-Width High	t_{CH}		18			ns
Setup Time	t_{CSS}		20			ns
Hold Time	t_{CSH}		20			ns
Minimum Pulse-Width High	t_{CSW}		20			ns
DIN Setup Time	t_{DS}		5			ns
DIN Hold Time	t_{DH}		5			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD} = 50pF		44	60	ns
Output Data Enable Time	t_{DEN}				60	ns
Output Data Disable Time	t_{DZ}				60	ns

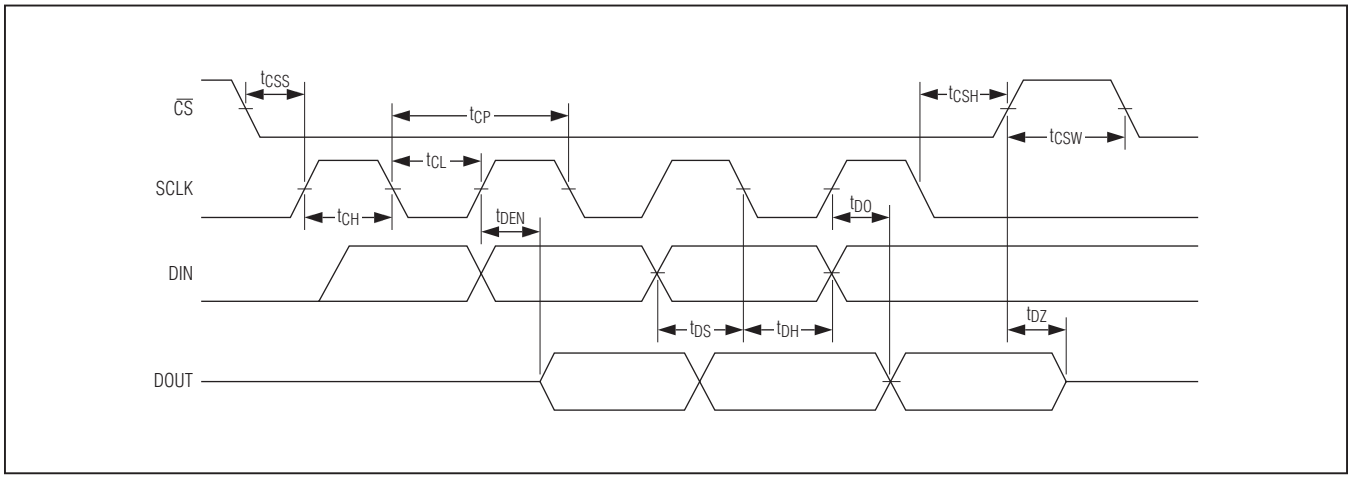


Figure 6. SPI Interface Timing Diagram

Note 2: The device is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: V_{DVDD} must be less than or equal to V_{HPVDD} for proper jack detection operation.
Note 4: Analog supply current = I_{AVDD} + I_{HPVDD}. Speaker supply current = I_{PVDDL} + I_{PVDDR}. Digital supply current = I_{DVDD} + I_{DVDDA} + I_{DVDDB} + I_{DVDDC}.
Note 5: Clocking all zeros into the DAC. Slave mode. Analog inputs AC-coupled to AGND.
Note 6: Dynamic range measured using the EIAJ method. -60dBFS 1kHz output signal, A-weighted, and normalized to 0dBFS. f = 20Hz–20kHz.
Note 7: DC accuracy measured with all PGAs set to 0dB.
Note 8: Gain measured relative to the 0dB setting.
Note 9: The filter specification is accurate only for synchronous clocking modes, where NI is a multiple of 0x1000.
Note 10: 0dBFS for DAC input. $1V_{P-P}$ for INA/INB input.
Note 11: Min/Max defines the RANGE of threshold values above which MIC_IN set high. So the minimum value of microphone impedance which is guaranteed to always trip the threshold is equal to ZMIC_MAX
Note 12: LRCLK may be any rate in the indicated range. Asynchronous or noninteger MCLK/LRCLK ratios might exhibit some full-scale performance degradation compared to synchronous integer related MCLK/LRCLK ratios.
Note 13: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 14: CB is in pF.

Power Consumption

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC} = 1.8V, V_{DVDD} = 1.8V, V_{PVDDL} = V_{PVDDR} = 4.2V.)

MODE	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDC} + I_{DVDDB} + I_{DVDDC} (mA)	I_{PVDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
PLAYBACK TO HEADPHONE ONLY							
DAC Playback 48kHz Stereo HP DAC → HP Low power mode, 24 bit, music filters, 256Fs	0.81	0.5	1.86	0.11	0.01	5.92	74.9
DAC Playback 48kHz Stereo HP DAC → HP Low power mode, 16 bit, music filters, 256Fs, 0.1mW/channel, R_{HP} = 16Ω	0.81	2.75	1.86	0.11	0.01	10.01	—
DAC Playback 48kHz Stereo HP DAC → HP Low power mode, 16 bit, music filters, 256Fs, 0.1mW/channel, R_{HP} = 32Ω	0.81	2.1	1.86	0.11	0.01	8.86	—
DAC Playback 48kHz Stereo HP DAC → HP 24 bit, music filters, 256Fs	1.67	1.27	4.38	0.11	0.1	13.8	101.1
DAC Playback 48kHz Stereo HP DAC → HP 24 bit, music filters, 256Fs, 0.1mW/channel, R_{HP} = 16Ω	1.6	3.24	4.41	0.18	0.1	17.4	—

Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC} = 1.8V, V_{DVDD} = 1.8V, V_{PVDDL} = V_{PVDDR} = 4.2V.)

MODE	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDC} + I_{DVDDB} + I_{DVDDC} (mA)	I_{PVDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
DAC Playback 48kHz Stereo HP DAC → HP 24 bit, music filters, 256Fs, 0.1mW/channel, R_{HP} = 32Ω	1.6	2.54	4.47	0.18	0.1	16.2	—
Mono MIC Playback Mono HP MIC1 → ADCL, DAC → HP	3.24	1.27	6.2	0.12	0.47	21.47	—
DAC PLAYBACK TO CLASS D SPEAKER							
DAC Playback 48kHz Stereo SPK DAC → SPK 24 bit, music filters	1.43	0.01	4.35	0.1	3.76	26.4	88.6
DAC Playback 48kHz Mono SPK DAC → SPK 24 bit, music filters	0.9	0.01	4.25	0.1	2.61	20.4	—
Stereo MIC Playback Stereo SPK MIC → ADC, DAC → SPK	3.95	0.01	6.31	0.14	4.22	36.4	—
Stereo MIC Playback Mono SPK MIC_ → ADC, DACL → SPKL	3.41	0.01	6.2	0.14	3.07	30.5	—
Mono MIC Playback Stereo SPK MIC1 → ADCL, DAC → SPK	3.07	0.01	6.2	0.11	4.13	34.26	—
Mono MIC Playback Mono SPK MIC1 → ADCL, DACL → SPKL	2.53	0.01	6.1	0.11	2.99	28.29	—
DAC PLAYBACK TO RECEIVER							
DAC Playback 8kHz RCV DAC→RCV 24 bit, voice filter	1.04	0.01	5.88	0.1	1.17	17.54	98.0
Stereo MIC Playback RCV MIC_→RCV	3.54	0.01	6.21	0.14	1.54	24.66	—
Mono MIC Playback RCV MIC1→RCV	2.68	0.01	6.1	0.11	1.54	22.48	—
DAC PLAYBACK TO LINE OUT							
DAC Playback 48kHz Stereo LINE OUT DAC→OUT1/2 (SE) 24 bit, music filters	1.26	0.01	7.5	0.1	0.97	20.01	97.9

Power Consumption (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC} = 1.8V, V_{DVDD} = 1.8V, V_{PVDDL} = V_{PVDDR} = 4.2V.)

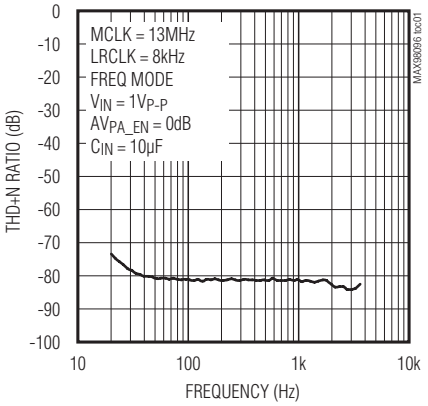
MODE	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{DVDD} (mA)	I_{DVDDC} + I_{DVDDB} + I_{DVDDC} (mA)	I_{PVDD} (mA)	POWER (mW)	DYNAMIC RANGE (dB)
MIC RECORD							
MIC Mono Record 48kHz MIC1→ADCL 24 bit, music filters	1.94	0.01	6.46	0.17	0.19	16.23	88.7
MIC Stereo Record 8kHz MIC→ADC 24 bit, voice filters	2.88	0.01	6.06	0.13	0.57	18.7	87.4
MIC Mono Record 8kHz MIC1→ADCL 24 bit, voice filters	1.99	0.01	5.96	0.11	0.48	16.5	87.4
LINE RECORD							
Line Stereo Record 48kHz INA (SE)→ADC 24 bit, music filters	2.55	0.01	5.98	0.22	0.28	16.94	87.0

Typical Operating Characteristics

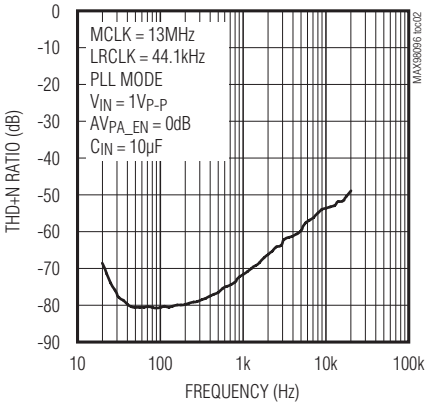
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

Microphone to ADC

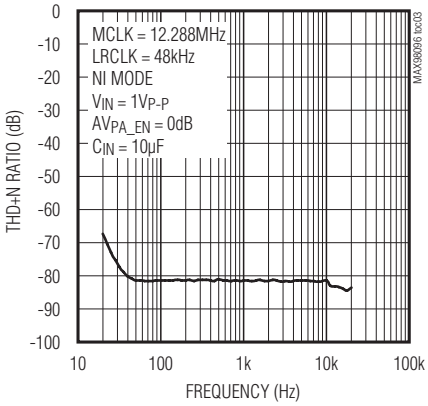
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



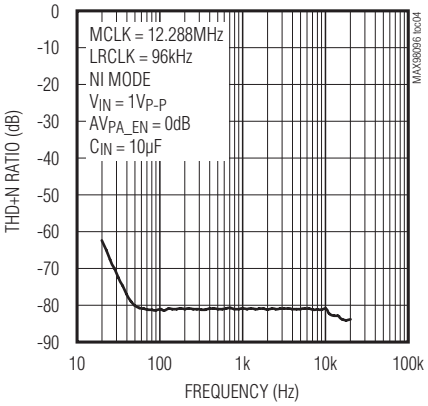
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



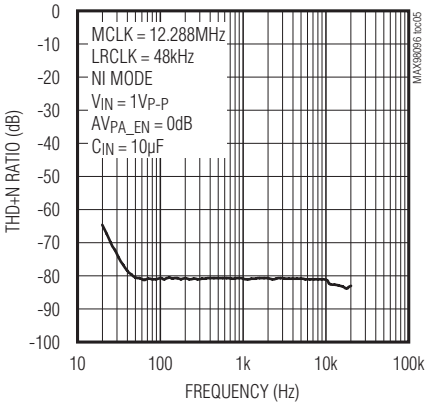
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



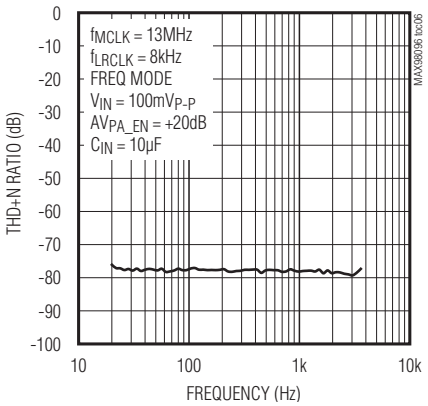
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



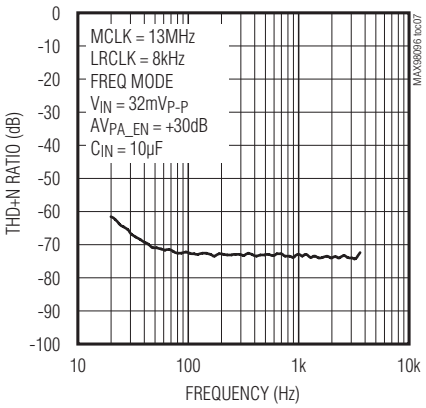
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



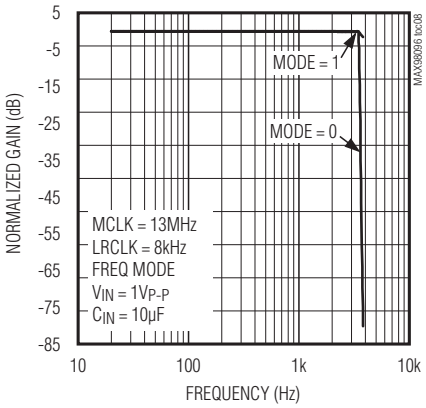
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

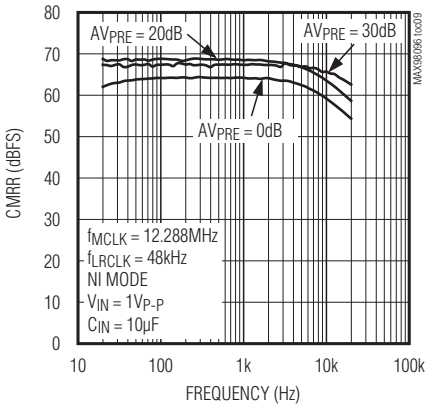
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)



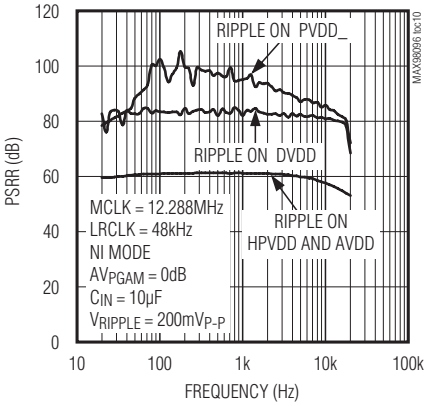
GAIN vs. FREQUENCY (MIC TO ADC)



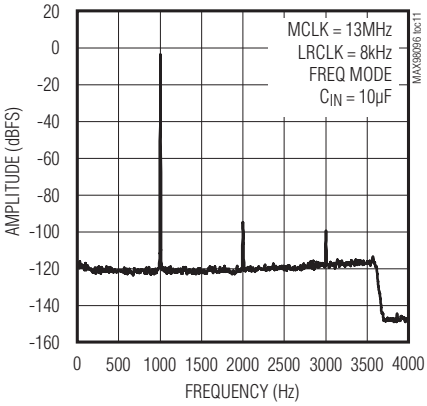
COMMON-MODE REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



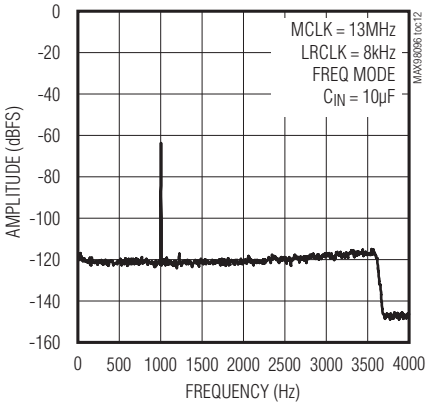
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



INBAND OUTPUT SPECTRUM, 0dBFS (MIC TO ADC)



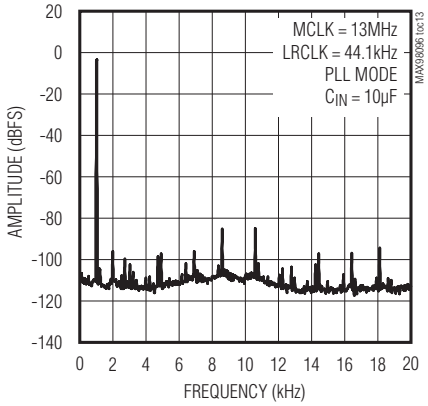
INBAND OUTPUT SPECTRUM, -60dBFS (MIC TO ADC)



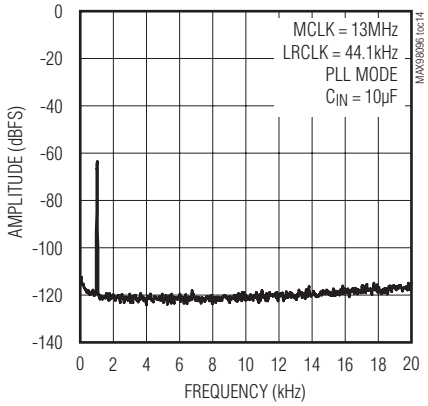
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

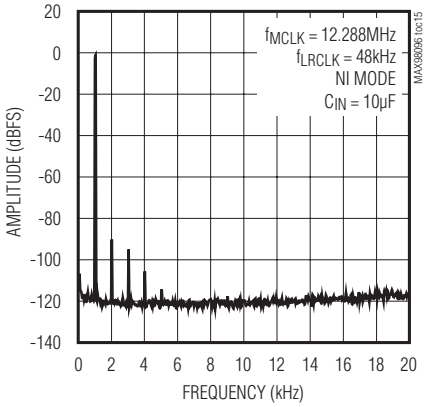
INBAND OUTPUT SPECTRUM, 0dBFS (MIC TO ADC)



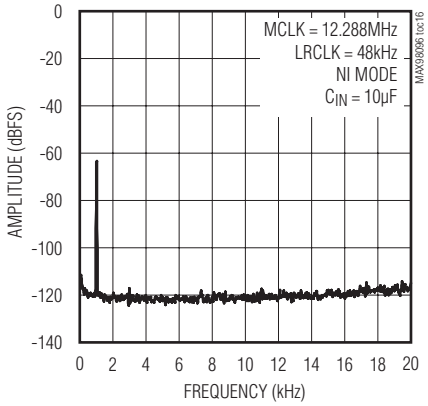
INBAND OUTPUT SPECTRUM, -60dBFS (MIC TO ADC)



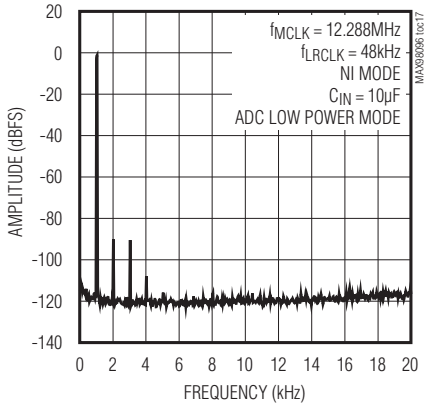
INBAND OUTPUT SPECTRUM, 0dBFS (MIC TO ADC)



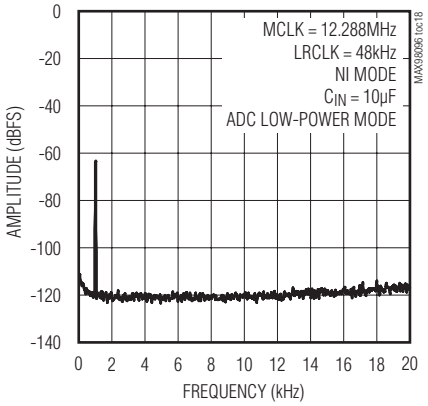
INBAND OUTPUT SPECTRUM, -60dBFS (MIC TO ADC)



INBAND OUTPUT SPECTRUM, 0dBFS (MIC TO ADC)



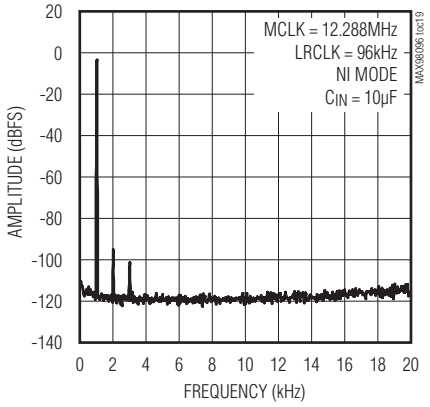
INBAND OUTPUT SPECTRUM, -60dBFS (MIC TO ADC)



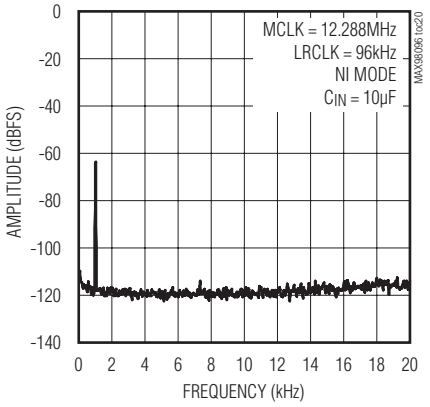
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

INBAND OUTPUT SPECTRUM, 0dBFS (MIC TO ADC)

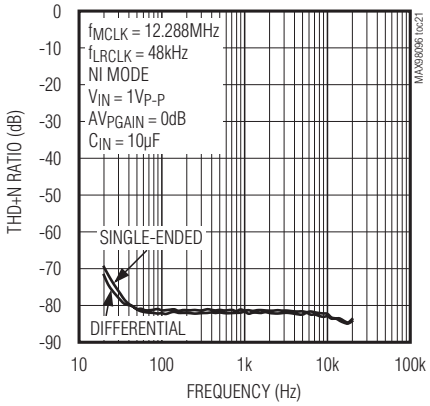


INBAND OUTPUT SPECTRUM, -60dBFS (MIC TO ADC)

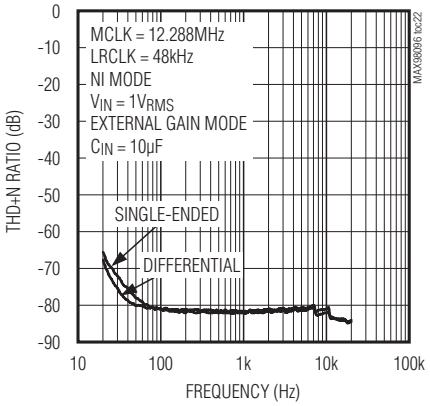


Line In to ADC

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



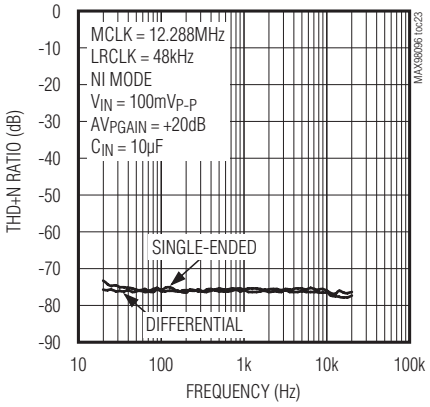
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)



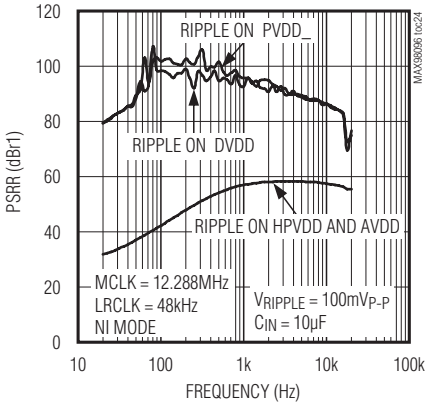
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)

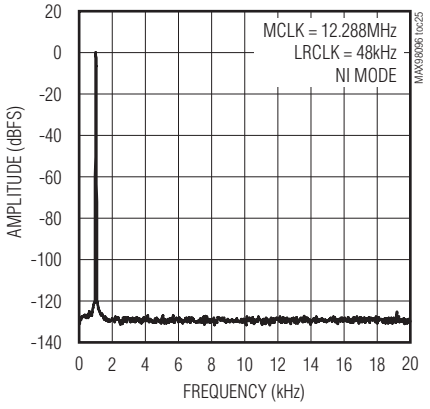


POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO ADC)

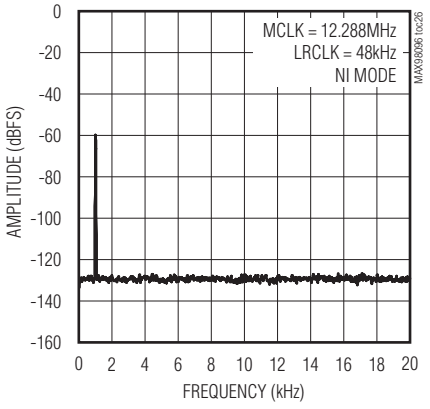


Digital Loopback–I²S In to I²S Out

INBAND OUTPUT SPECTRUM vs. FREQUENCY (DIGITAL LOOPBACK)



INBAND OUTPUT SPECTRUM vs. FREQUENCY (DIGITAL LOOPBACK)

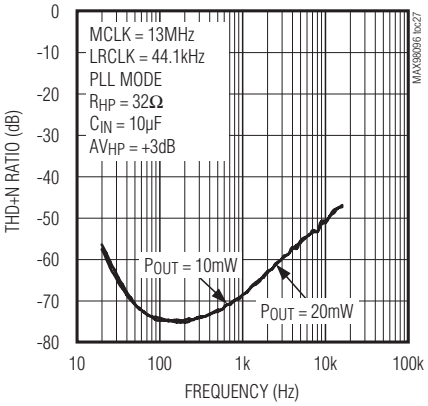


Typical Operating Characteristics (continued)

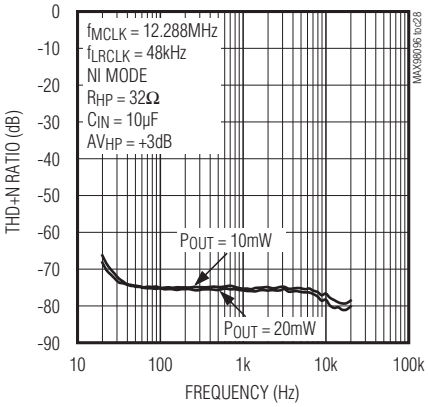
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

Analog Loopback–Line Input to Headphone Output

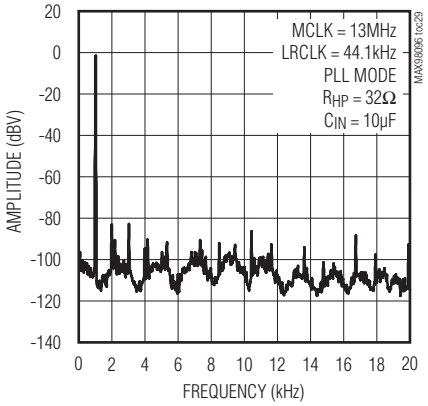
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



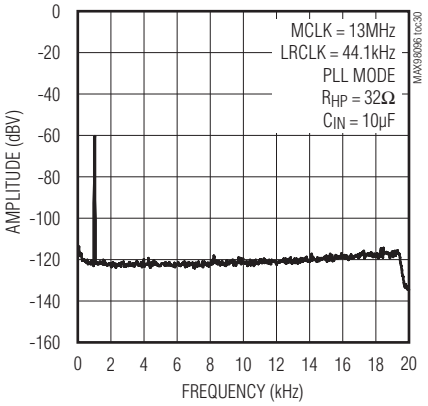
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



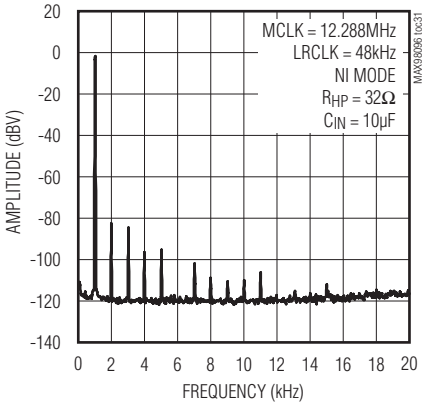
INBAND OUTPUT SPECTRUM, 0dBFS (LINE TO ADC TO DAC TO HEADPHONE)



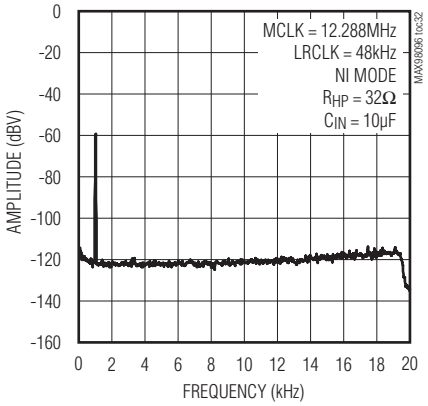
INBAND OUTPUT SPECTRUM, -60dBFS (LINE TO ADC TO DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, 0dBFS (LINE TO ADC TO DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -60dBFS (LINE TO ADC TO DAC TO HEADPHONE)

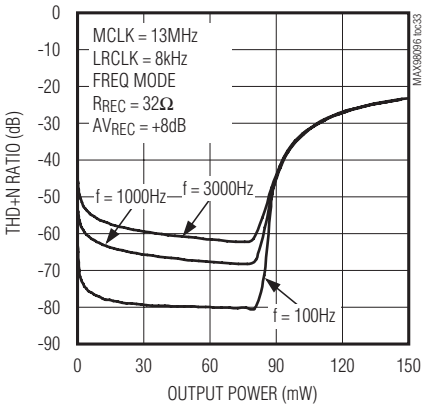


Typical Operating Characteristics (continued)

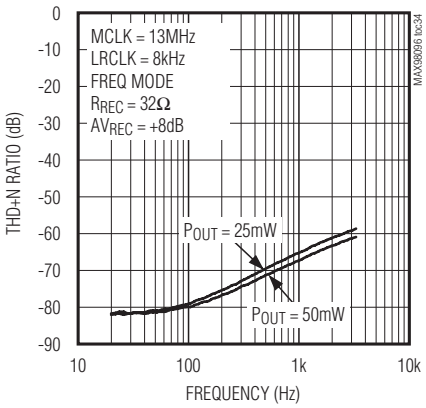
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

DAC to Receiver

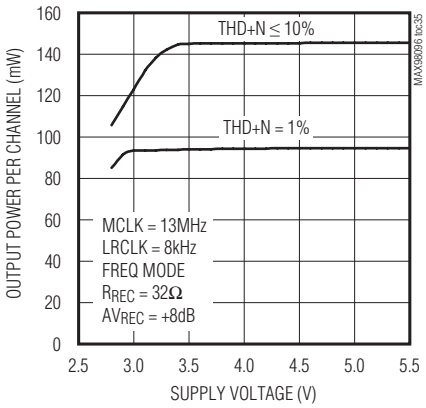
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER (DAC TO RECEIVER)



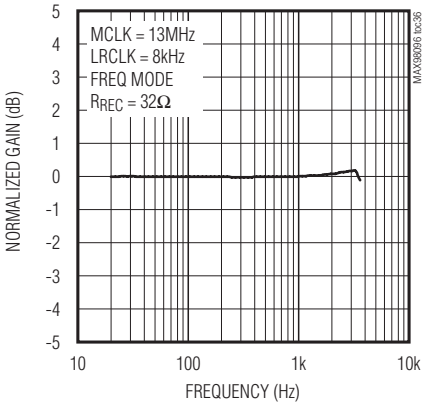
TOTAL HARMONIC DISTORTION vs. FREQUENCY (DAC TO RECEIVER)



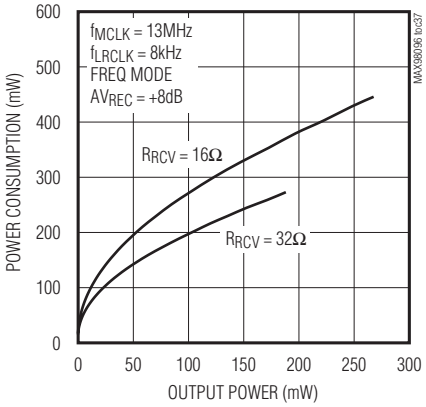
OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO RECEIVER)



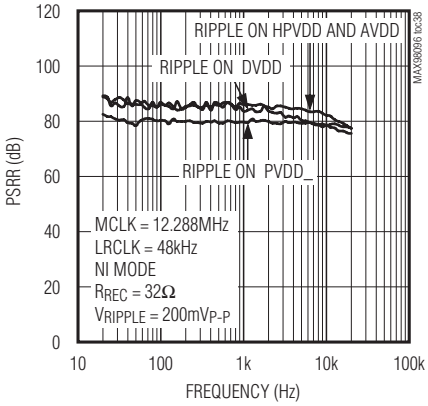
GAIN vs. FREQUENCY (DAC TO RECEIVER)



POWER CONSUMPTION vs. OUTPUT POWER (DAC TO RECEIVER)



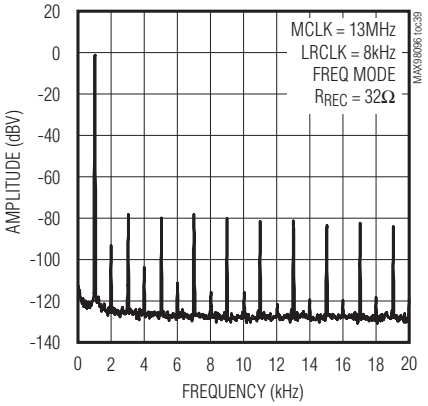
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO RECEIVER)



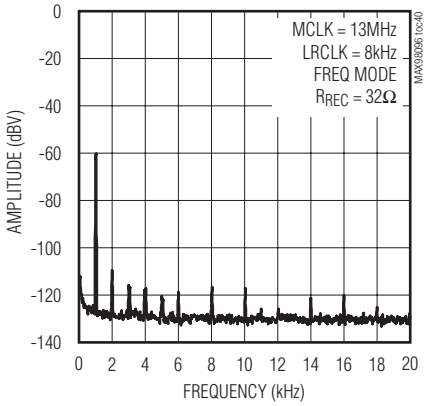
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

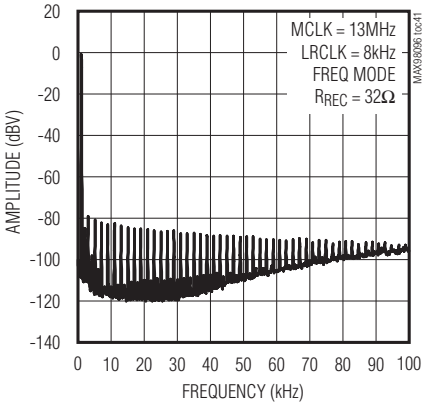
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO RECEIVER)



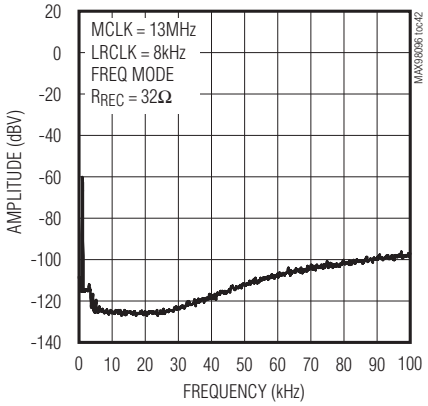
INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO RECEIVER)



WIDEBAND OUTPUT SPECTRUM, 0dBFS (DAC TO RECEIVER)



WIDEBAND OUTPUT SPECTRUM, -60dBFS (DAC TO RECEIVER)

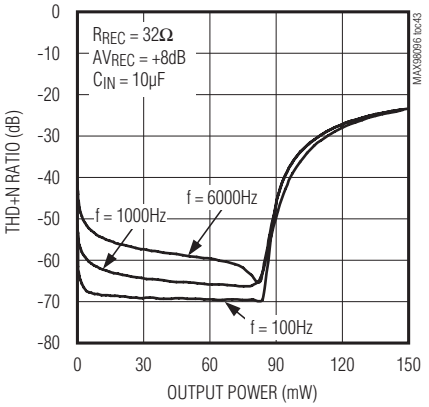


Typical Operating Characteristics (continued)

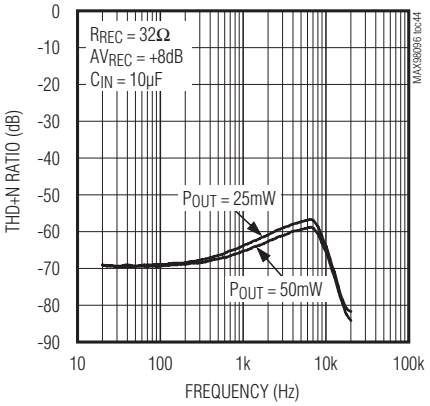
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

Line In to Receiver

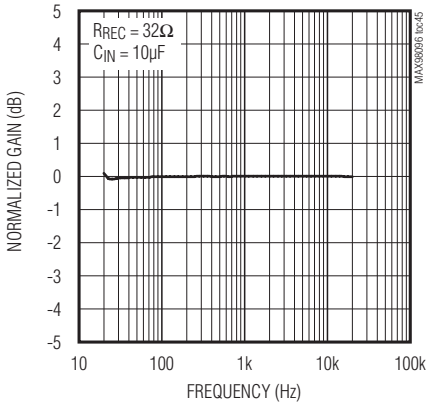
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO RECEIVER)



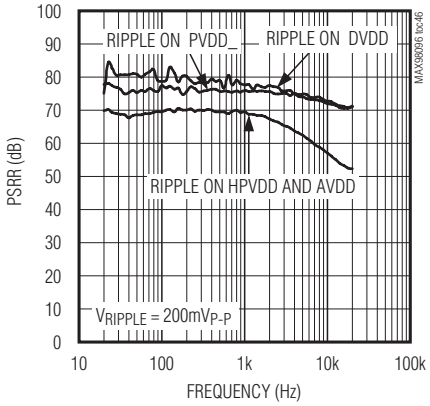
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO RECEIVER)



GAIN vs. FREQUENCY (LINE TO RECEIVER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO RECEIVER)



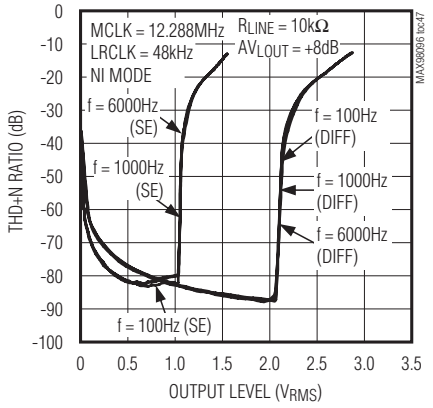
Audio Hub with Wideband FlexSound Processor

Typical Operating Characteristics (continued)

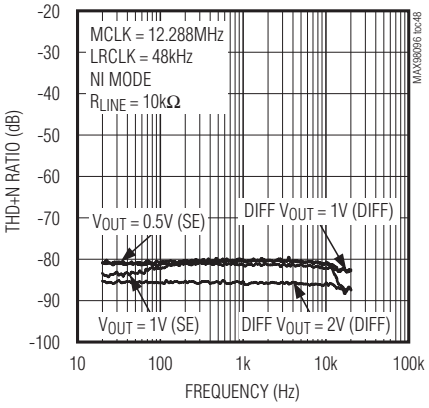
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

DAC to Line Output (Single-Ended and Differential Output)

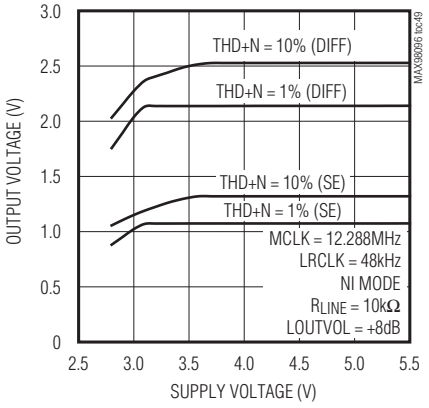
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT LEVEL (DAC TO LINE)



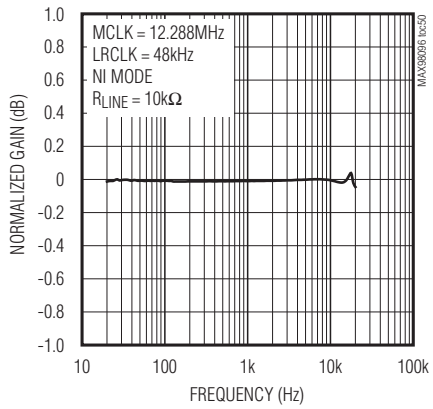
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO LINE)



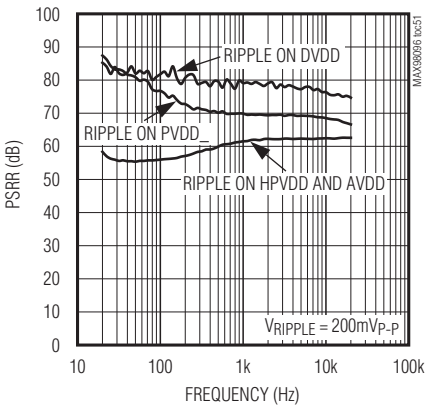
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (DAC TO LINE)



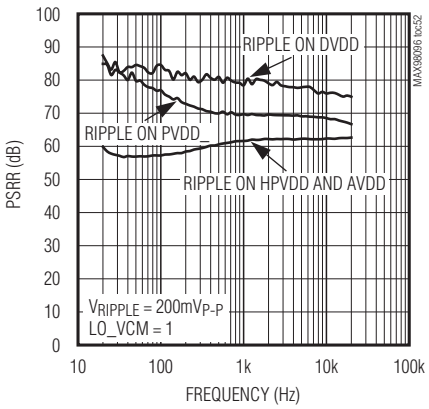
GAIN vs. FREQUENCY (DAC TO LINE)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO LINE OUT)



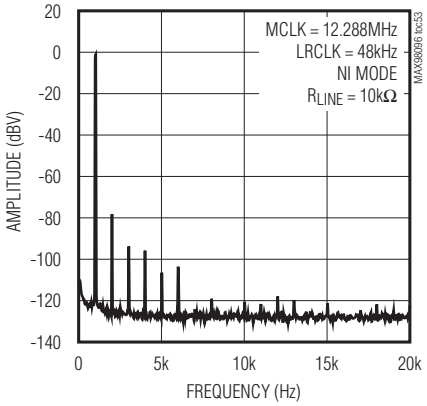
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO LINE OUT)



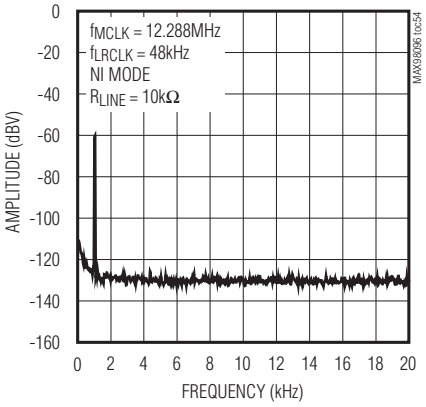
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

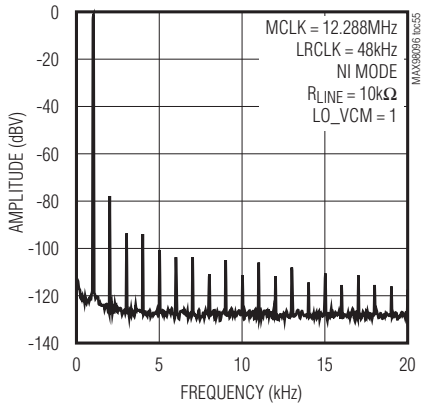
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO LINE)



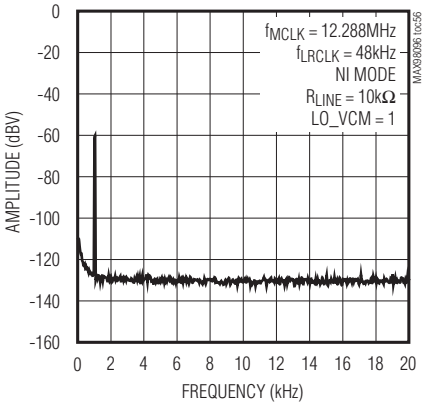
INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO LINE)



INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO LINE)



INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO LINE)

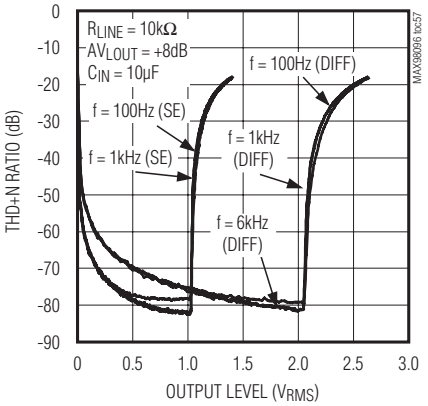


Typical Operating Characteristics (continued)

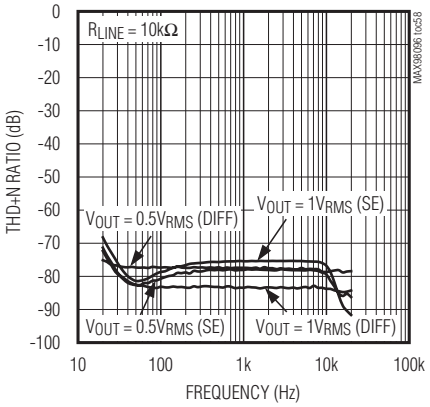
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

Line In to Line Out (Single-Ended and Differential Output)

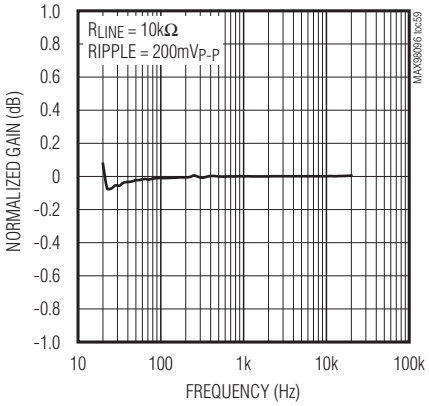
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT LEVEL (LINE IN TO LINE OUT)



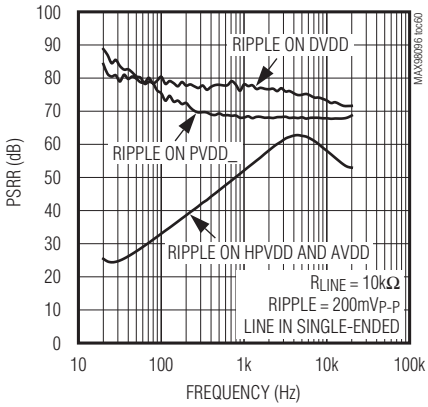
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO LINE OUT)



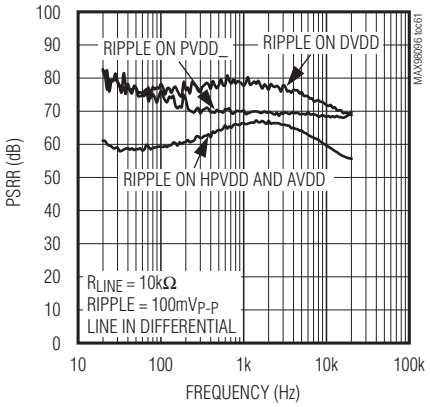
GAIN vs. FREQUENCY (LINE IN TO LINE OUT)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE IN TO LINE OUT)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE IN TO LINE OUT)

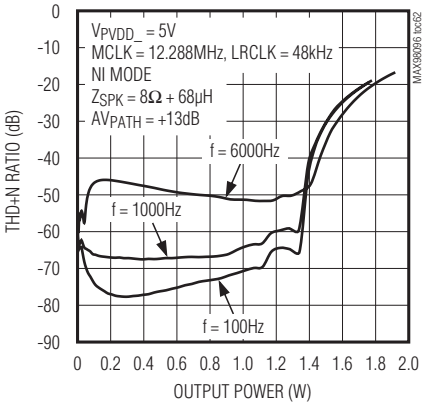


Typical Operating Characteristics (continued)

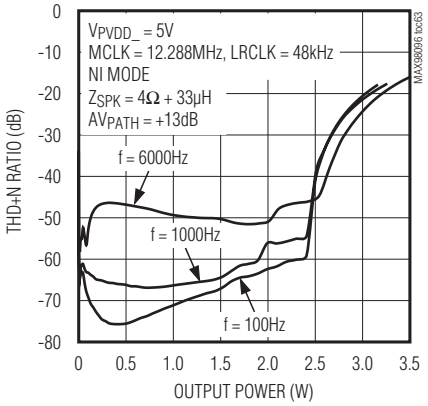
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

DAC to Speaker

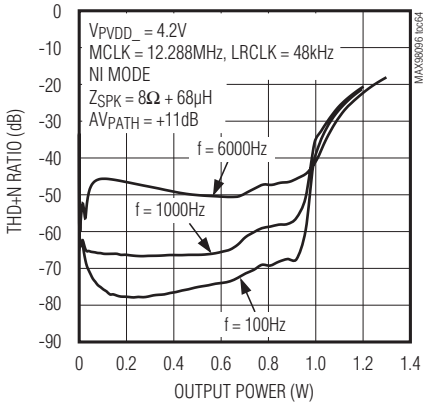
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



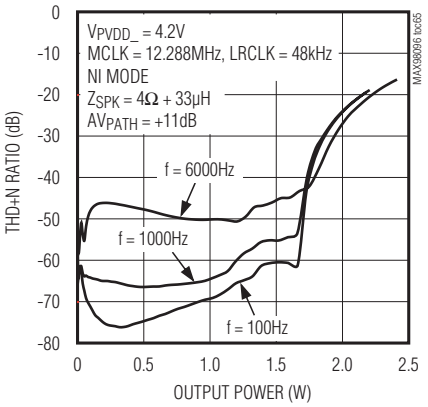
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



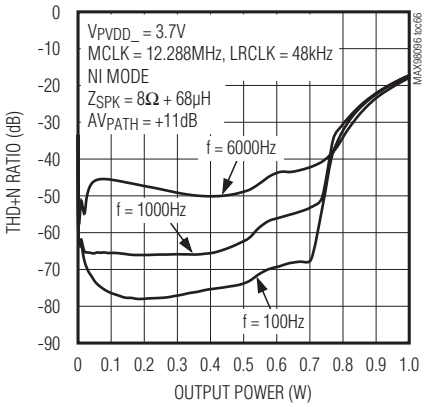
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



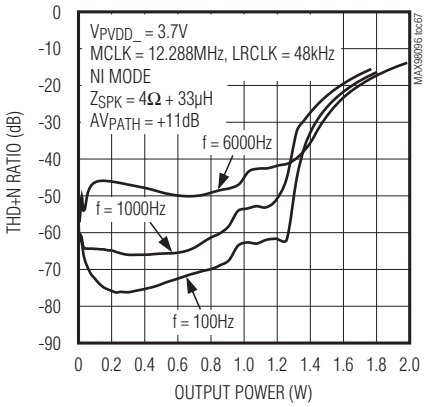
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



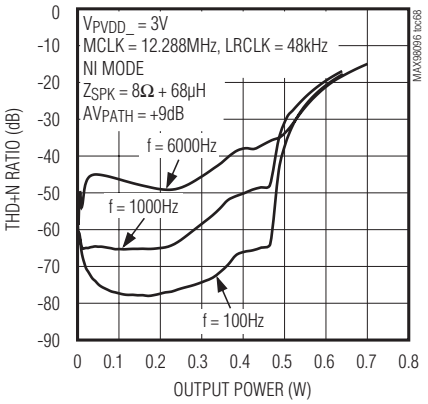
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



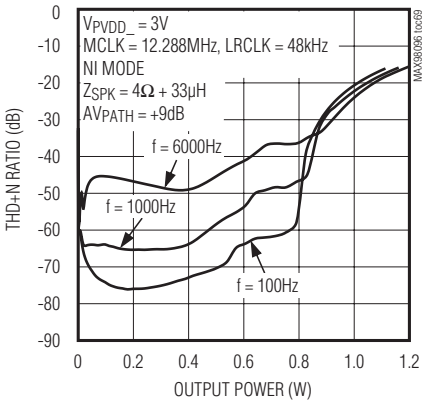
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

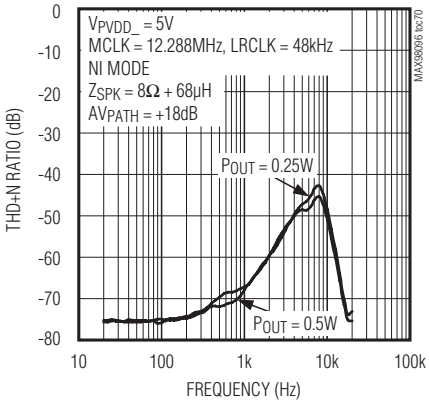
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



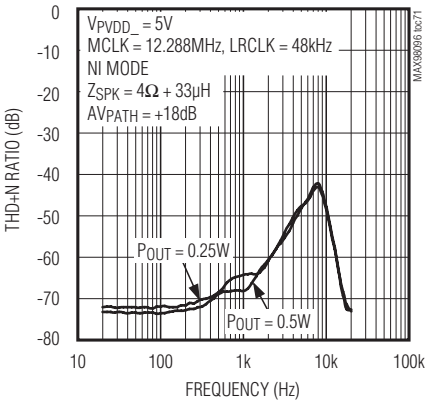
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)



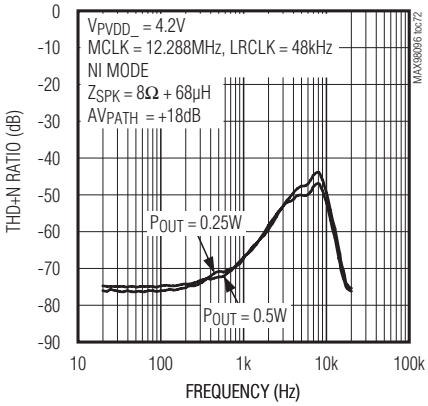
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



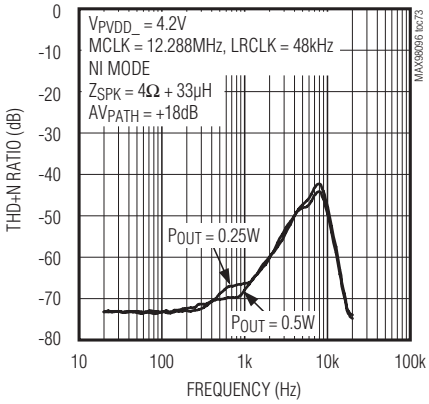
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



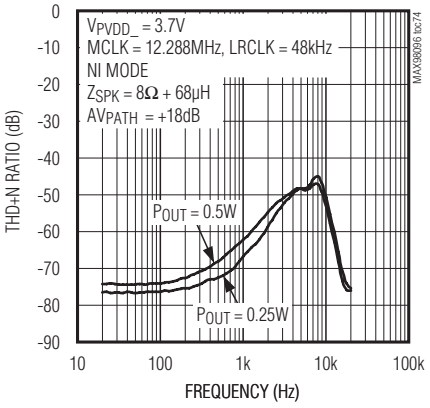
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



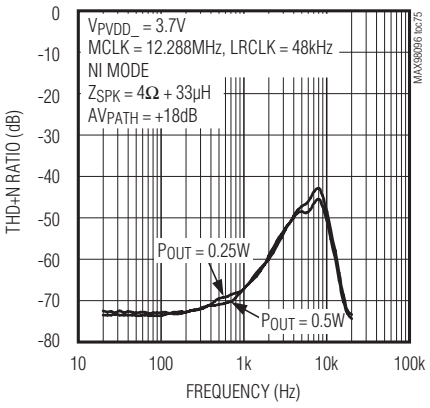
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

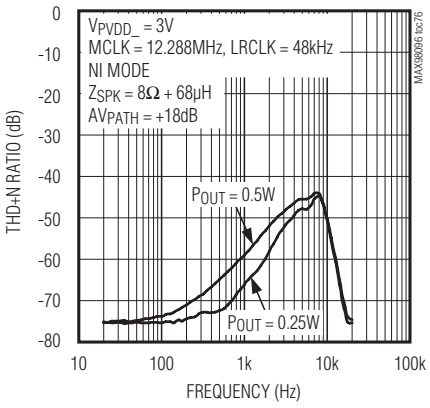
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



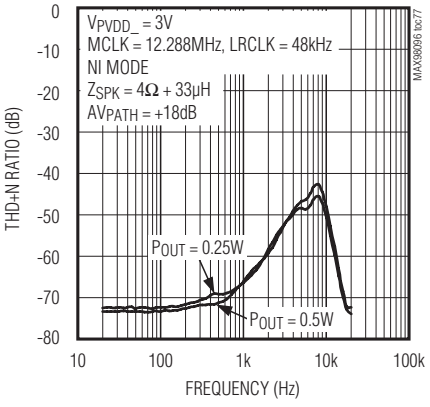
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



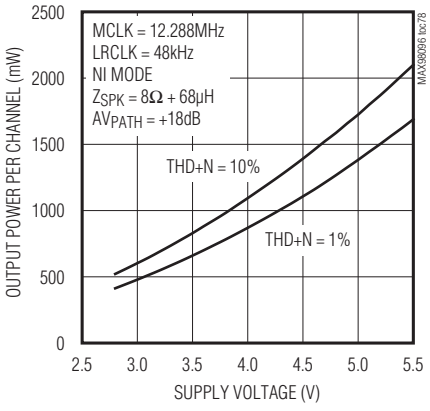
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



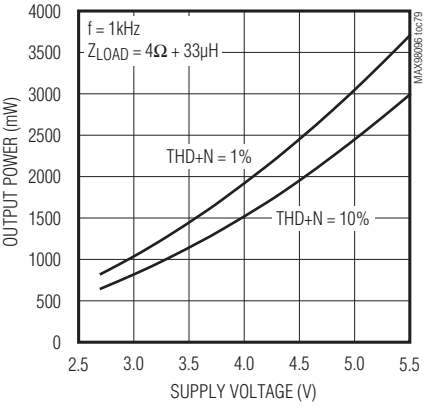
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)



OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



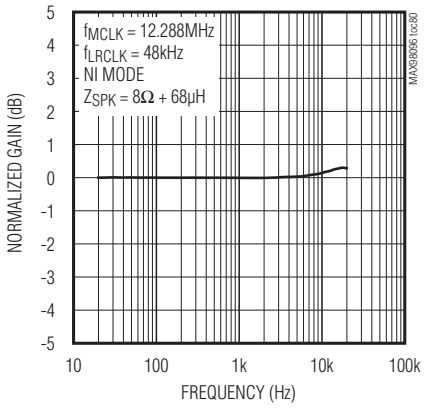
OUTPUT POWER vs. SUPPLY VOLTAGE



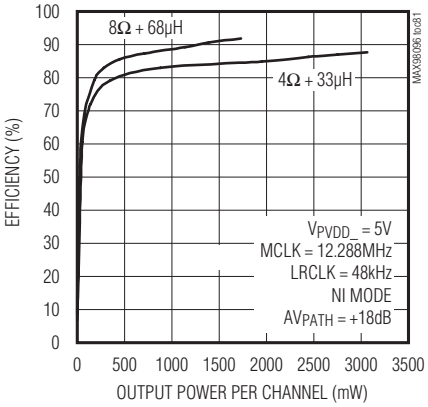
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

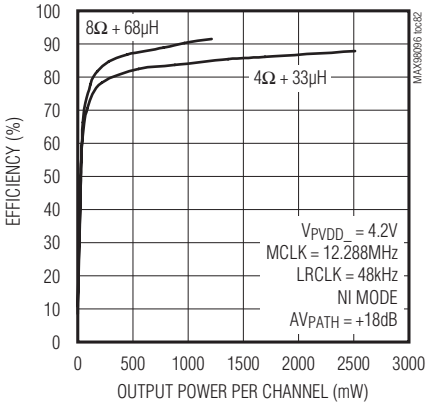
GAIN vs. FREQUENCY (DAC TO SPEAKER)



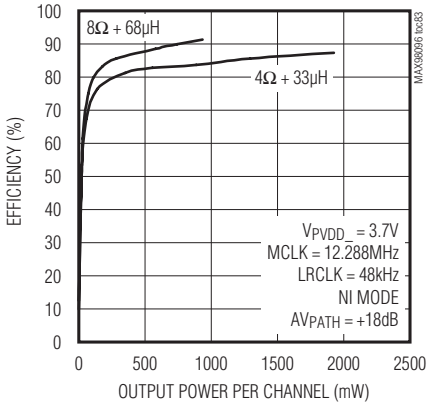
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



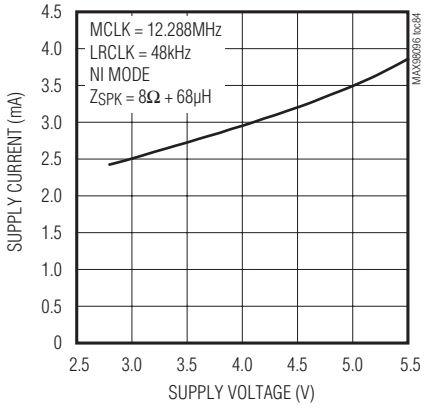
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



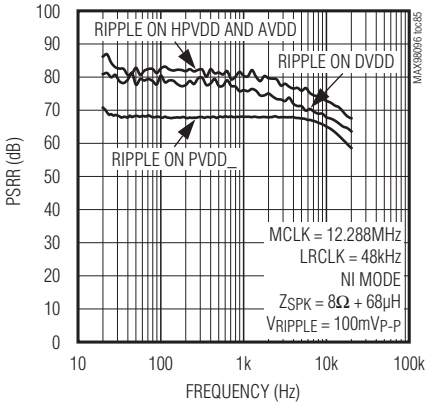
EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)



PVDD_ SUPPLY CURRENT vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



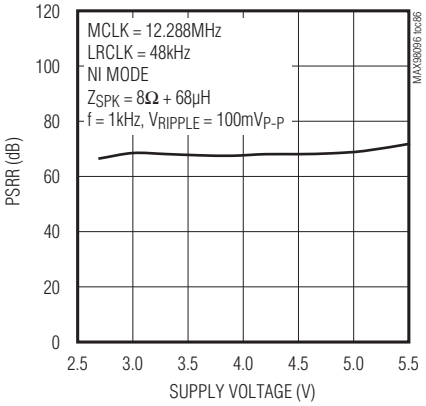
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



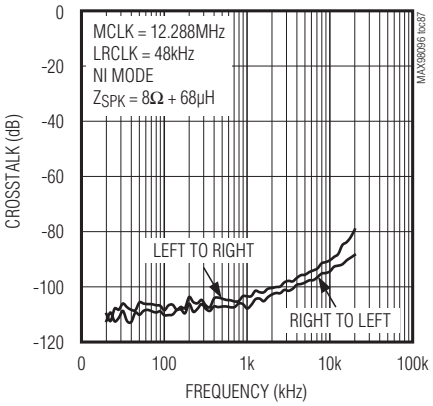
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

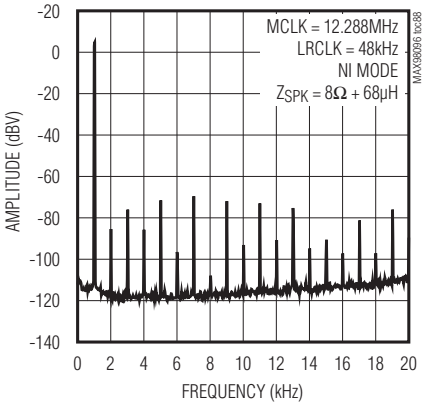
POWER-SUPPLY REJECTION RATION vs. SUPPLY VOLTAGE (DAC TO SPEAKER)



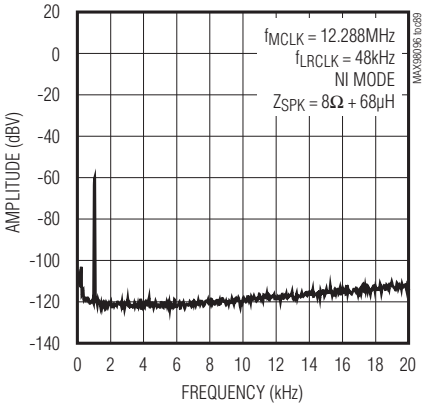
CROSSTALK vs. FREQUENCY (DAC TO SPEAKER)



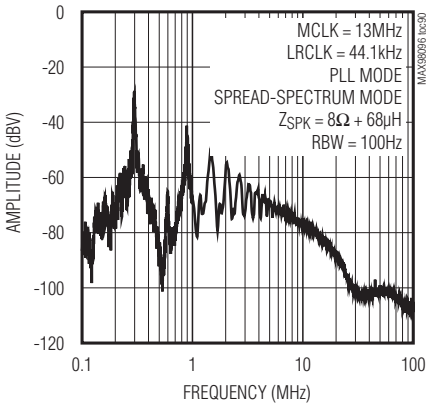
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO SPEAKER)



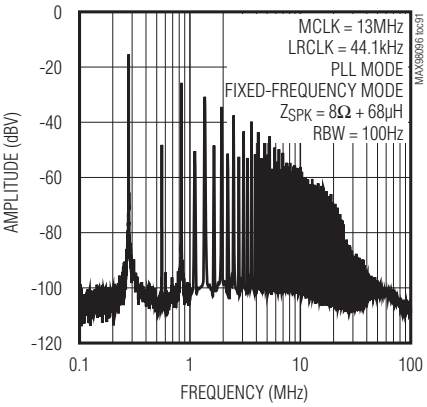
INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO SPEAKERS)



WIDEBAND FREQUENCY SPECTRUM, (DAC TO SPEAKER)



WIDEBAND FREQUENCY SPECTRUM, (DAC TO SPEAKER)

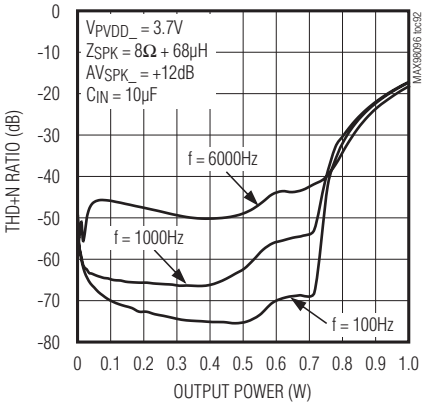


Typical Operating Characteristics (continued)

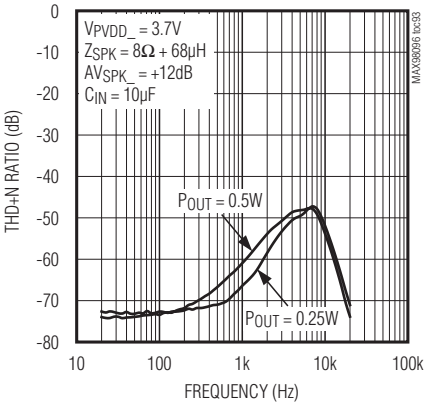
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

Line In to Speaker

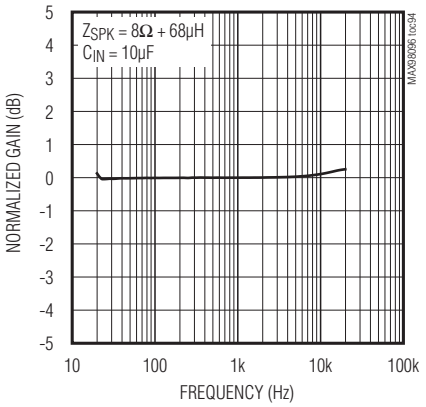
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO SPEAKER)



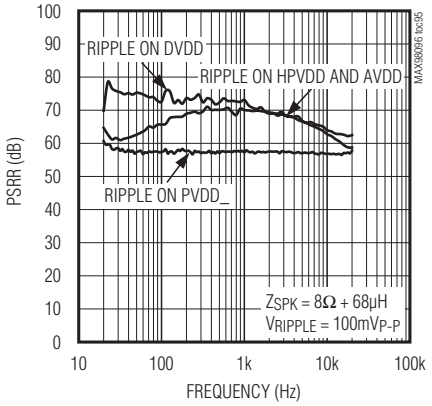
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO SPEAKER)



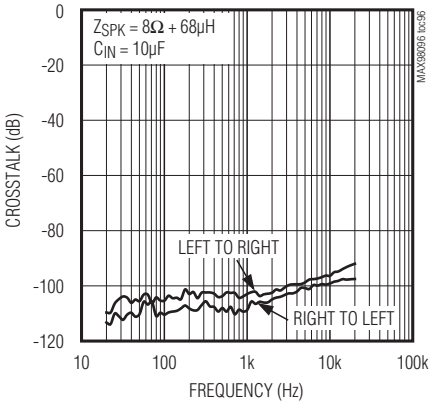
GAIN vs. FREQUENCY (LINE TO SPEAKER)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO SPEAKER)



CROSSTALK vs. FREQUENCY (LINE TO SPEAKER)

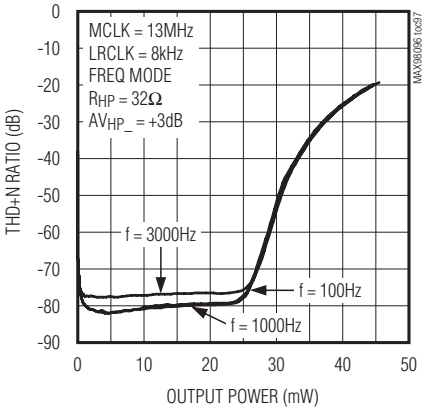


Typical Operating Characteristics (continued)

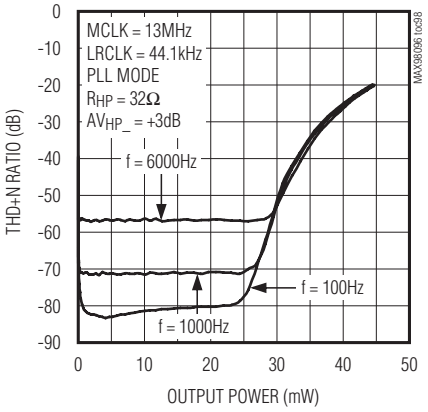
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

DAC to Headphone

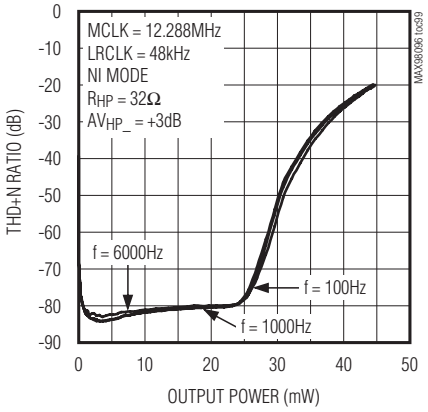
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



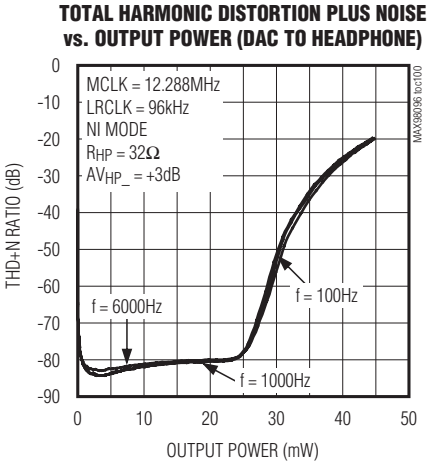
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



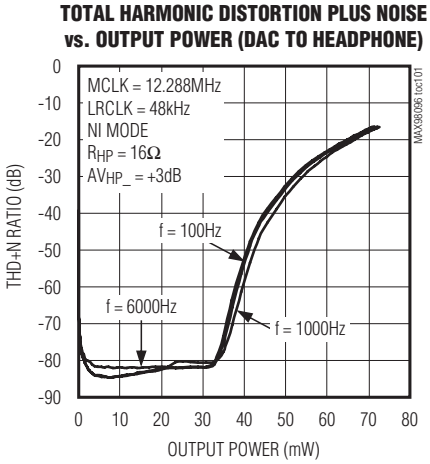
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



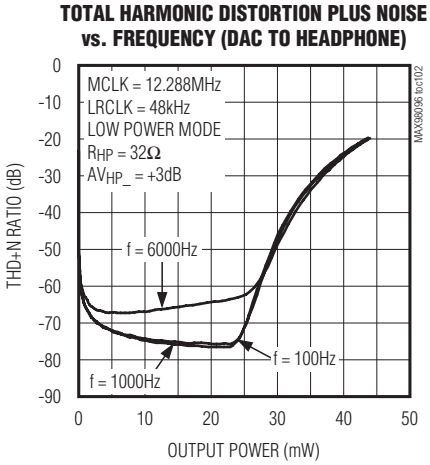
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)



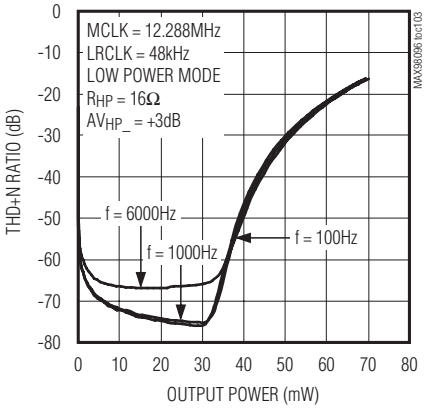
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



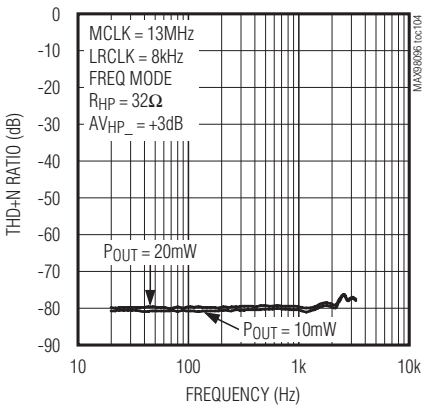
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

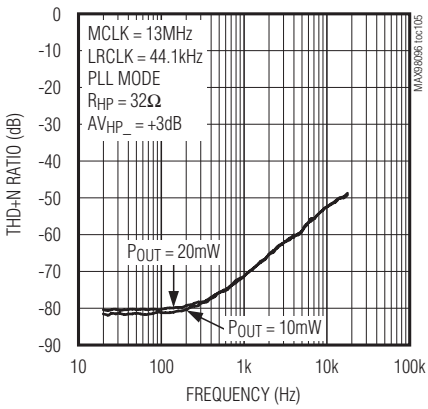
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



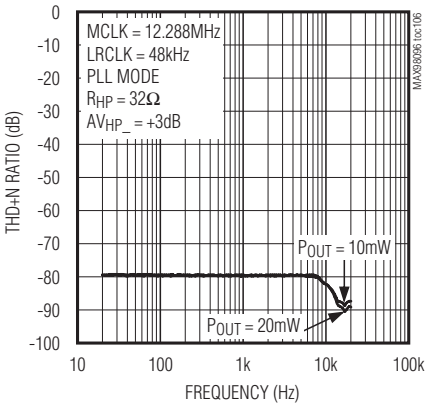
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



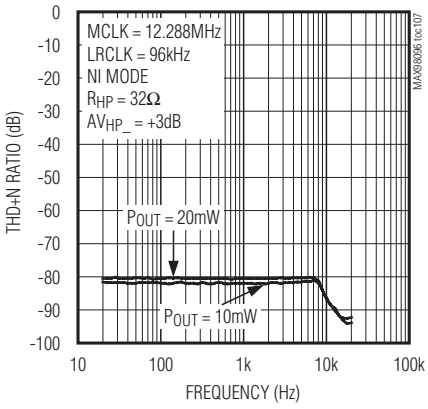
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



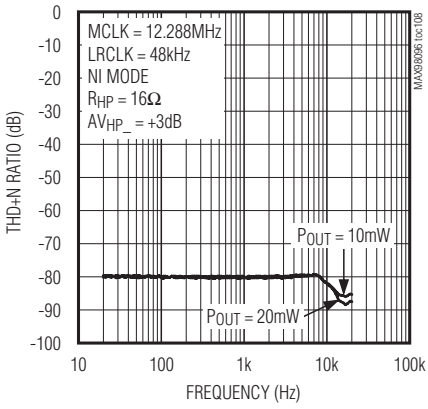
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



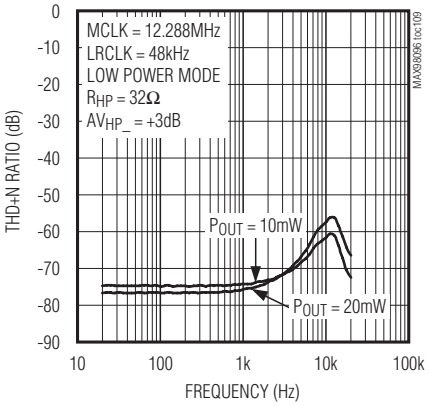
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



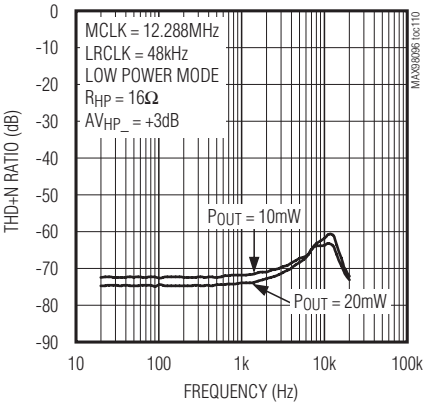
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

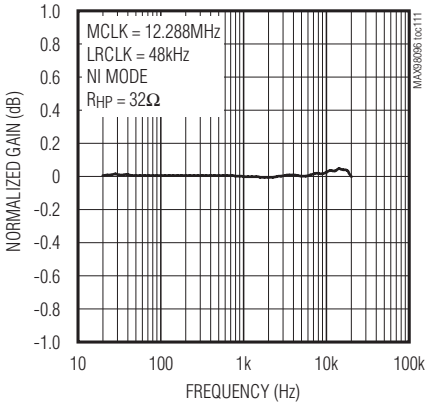
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



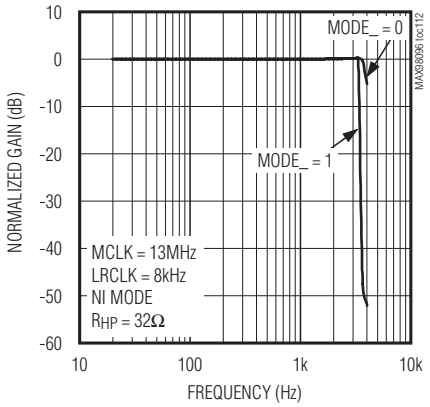
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)



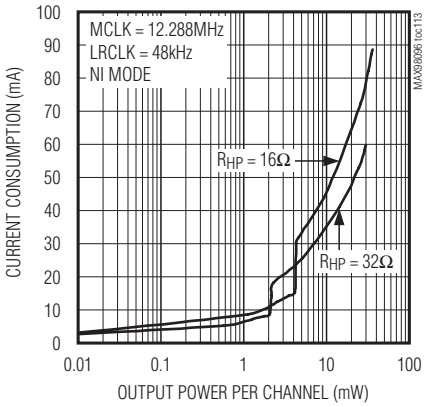
GAIN vs. FREQUENCY (DAC TO HEADPHONE)



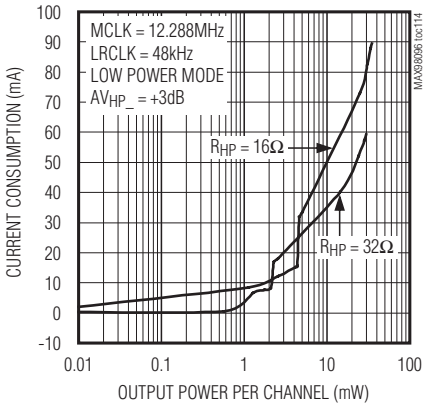
GAIN vs. FREQUENCY (DAC TO HEADPHONE)



CURRENT CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)



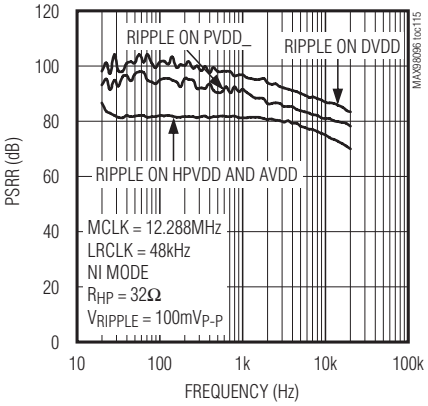
CURRENT CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)



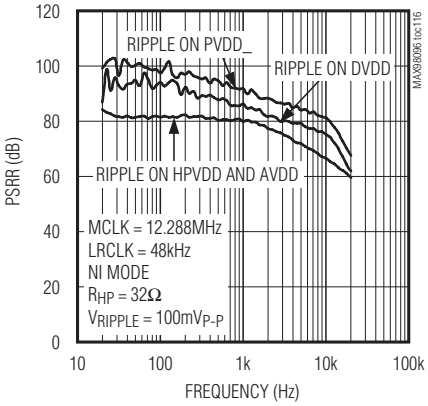
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

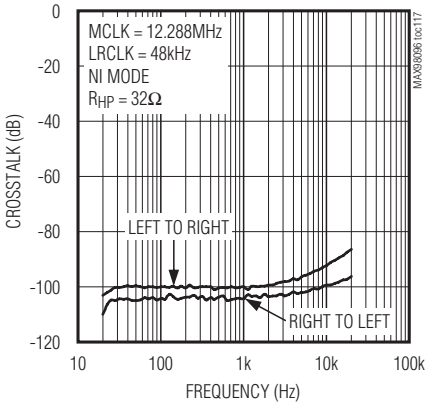
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



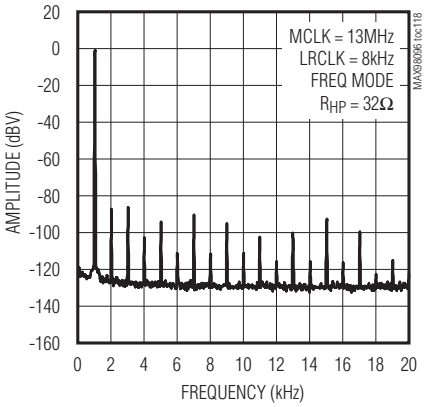
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



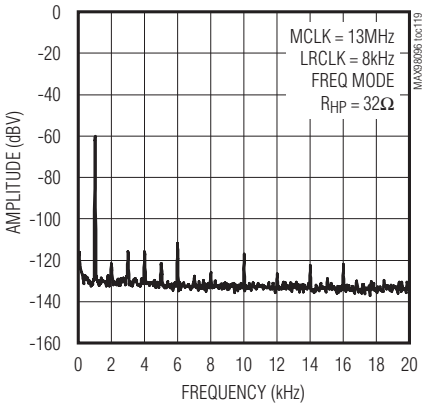
CROSSTALK vs. FREQUENCY (DAC TO HEADPHONE)



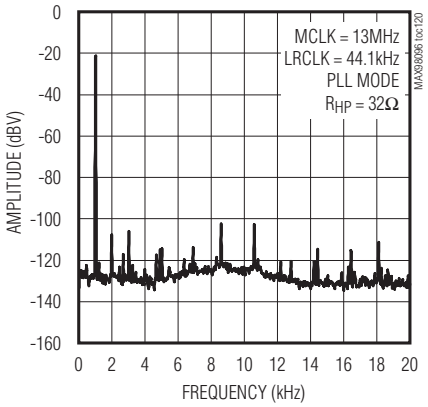
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO HEADPHONE)



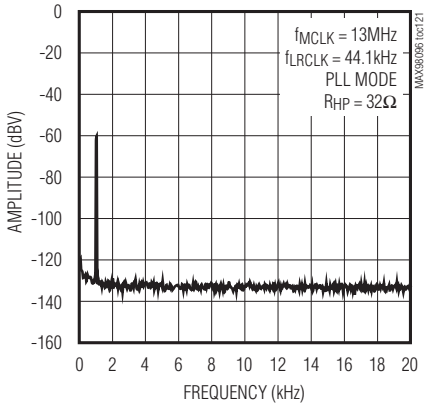
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO HEADPHONE)



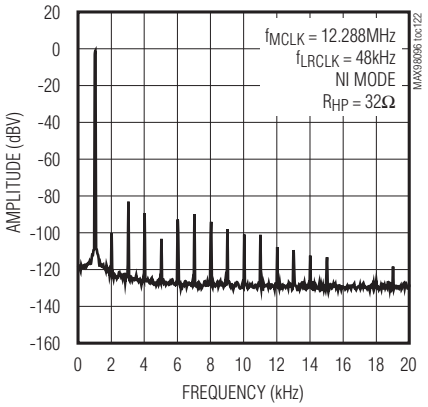
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

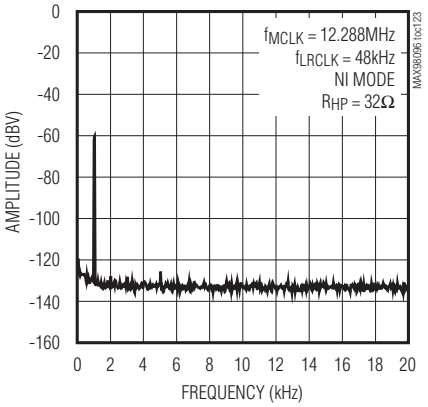
INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO HEADPHONE)



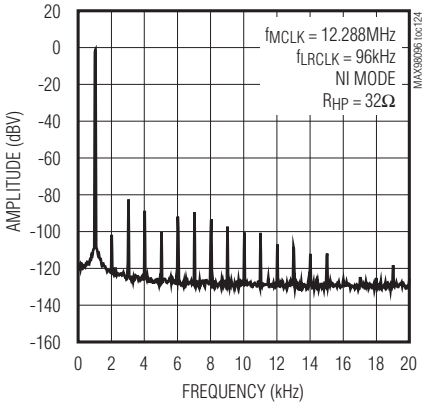
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO HEADPHONE)



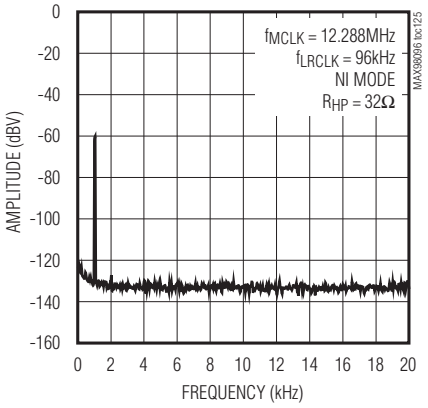
INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO HEADPHONE)



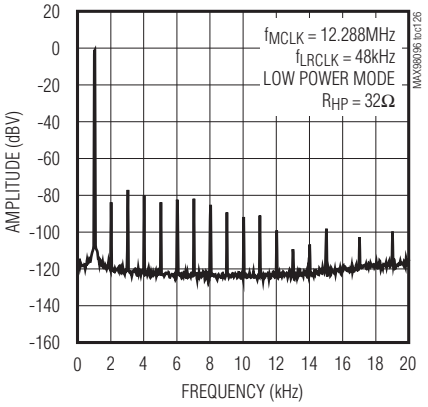
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO HEADPHONE)



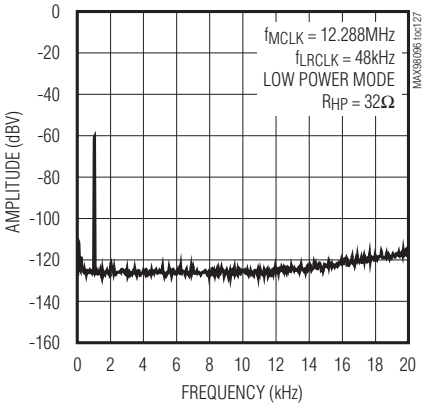
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO HEADPHONE)



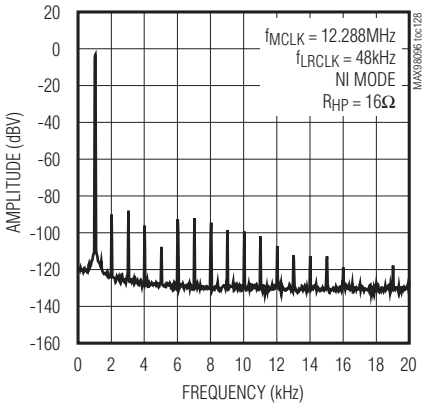
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

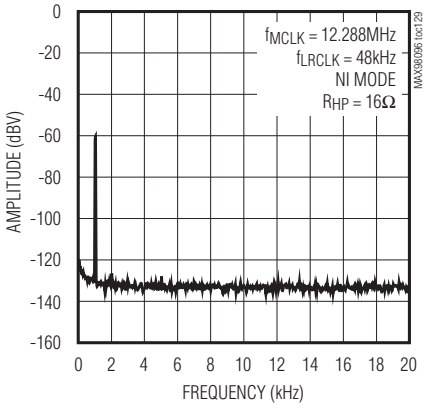
INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO HEADPHONE)



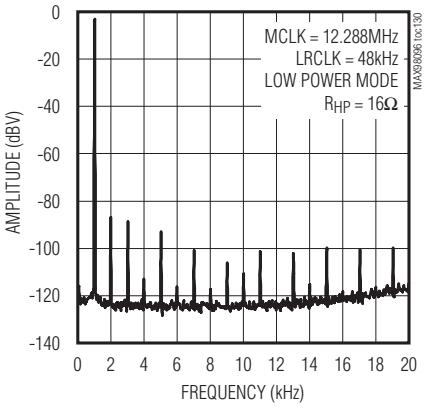
INBAND OUTPUT SPECTRUM, -2dBFS (DAC TO HEADPHONE)



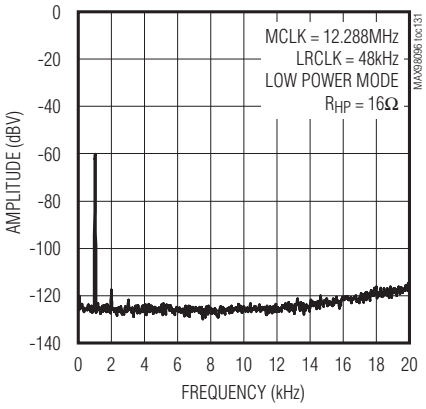
INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO HEADPHONE)



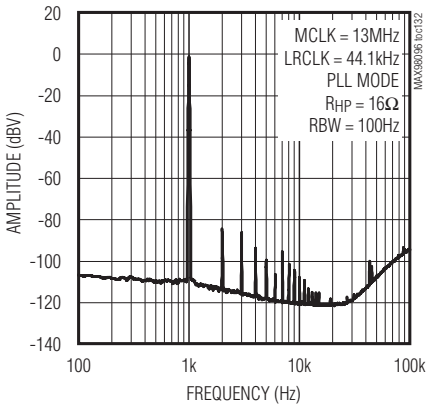
INBAND OUTPUT SPECTRUM, 0dBFS (DAC TO HEADPHONE)



INBAND OUTPUT SPECTRUM, -60dBFS (DAC TO HEADPHONE)



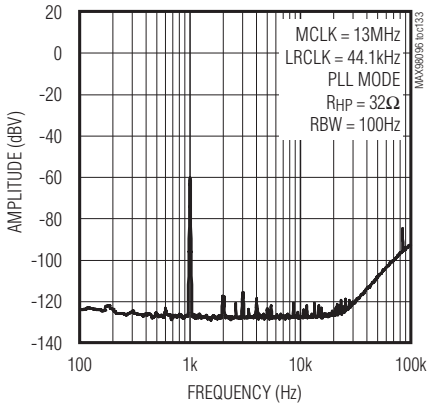
WIDEBAND FREQUENCY SPECTRUM, 0dBFS (DAC TO HEADPHONE)



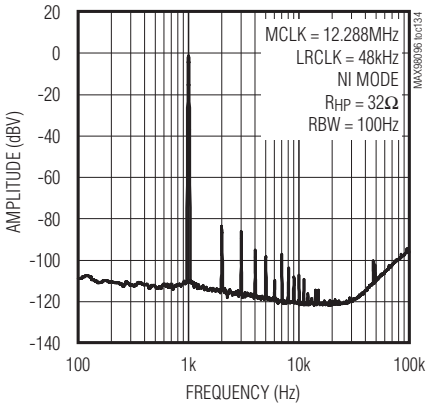
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

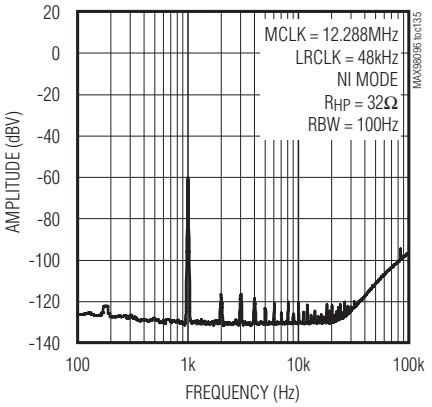
WIDEBAND FREQUENCY SPECTRUM, -60dBFS (DAC TO HEADPHONE)



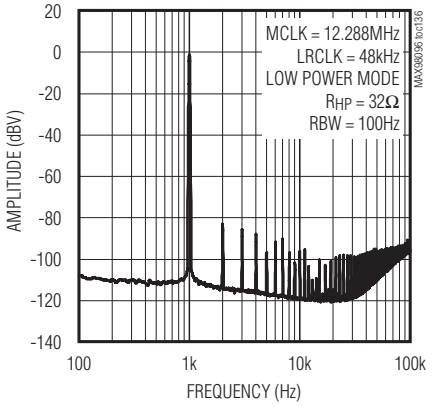
WIDEBAND FREQUENCY SPECTRUM, 0dBFS (DAC TO HEADPHONE)



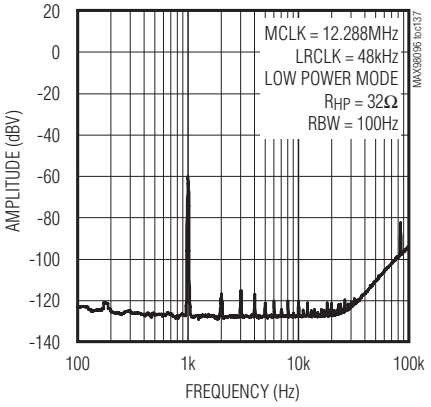
WIDEBAND FREQUENCY SPECTRUM, -60dBFS (DAC TO HEADPHONE)



WIDEBAND FREQUENCY SPECTRUM, 0dBFS (DAC TO HEADPHONE)



WIDEBAND FREQUENCY SPECTRUM, -60dBFS (DAC TO HEADPHONE)

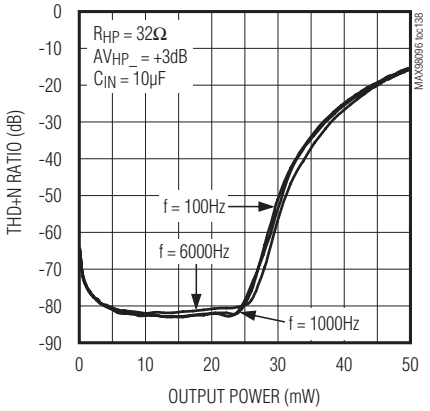


Typical Operating Characteristics (continued)

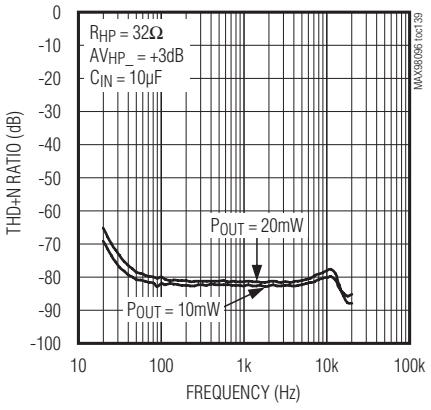
(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

Line In to Headphone

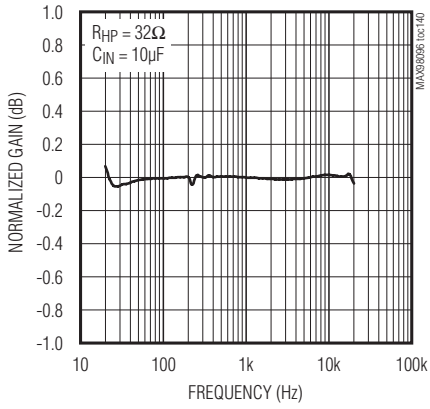
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO HEADPHONE)



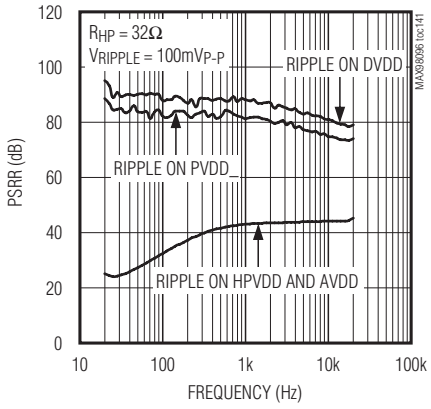
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO HEADPHONE)



GAIN vs. FREQUENCY (LINE TO HEADPHONE)



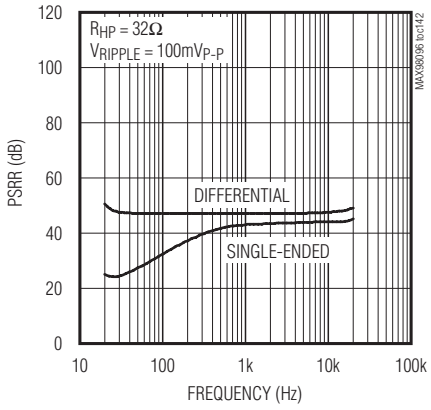
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONES)



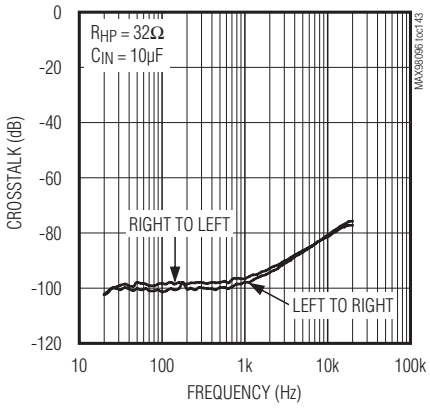
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{HPVDD} = V_{DVDDA} = V_{DVDDB} = V_{DVDDC}= +1.8V, V_{DVDD} = +1.8V, V_{PVDDL} = V_{PVDDR} = +4.2V. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. Receiver load (R_{RCV}) connected between RCVP and RCVN. Headphone loads (R_{HP}) connected from HPL or HPR to ground. Line output loads (R_{LO}) connected from OUT1, OUT2, OUT3, or OUT4 to ground. R_{HP} = ∞, R_{RCV} = ∞, Z_{SPK} = ∞, R_{LO} = ∞, C_{REF} = 2.2µF, $C_{MICBIAS1}$ = $C_{MICBIAS2}$ = C_{REG} = 1µF, $C_{C1N-C1P}$ = 1µF, C_{CPVDD} = C_{CPVSS} = 1µF. $AV_{MICPRE\_}$ = +20dB. All other gain settings are 0dB, unless otherwise stated. MCLK = 12.288MHz, LRCLK = 48kHz, MAS = 0, 24-bit source data.

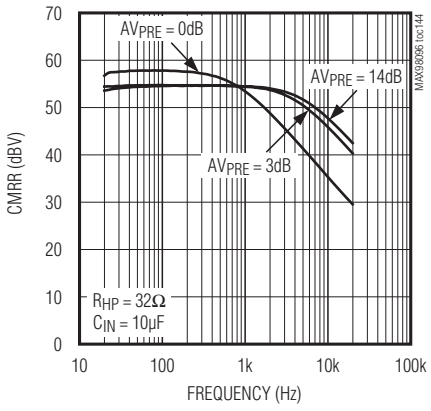
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)



CROSSTALK vs. FREQUENCY (LINE TO HEADPHONE)

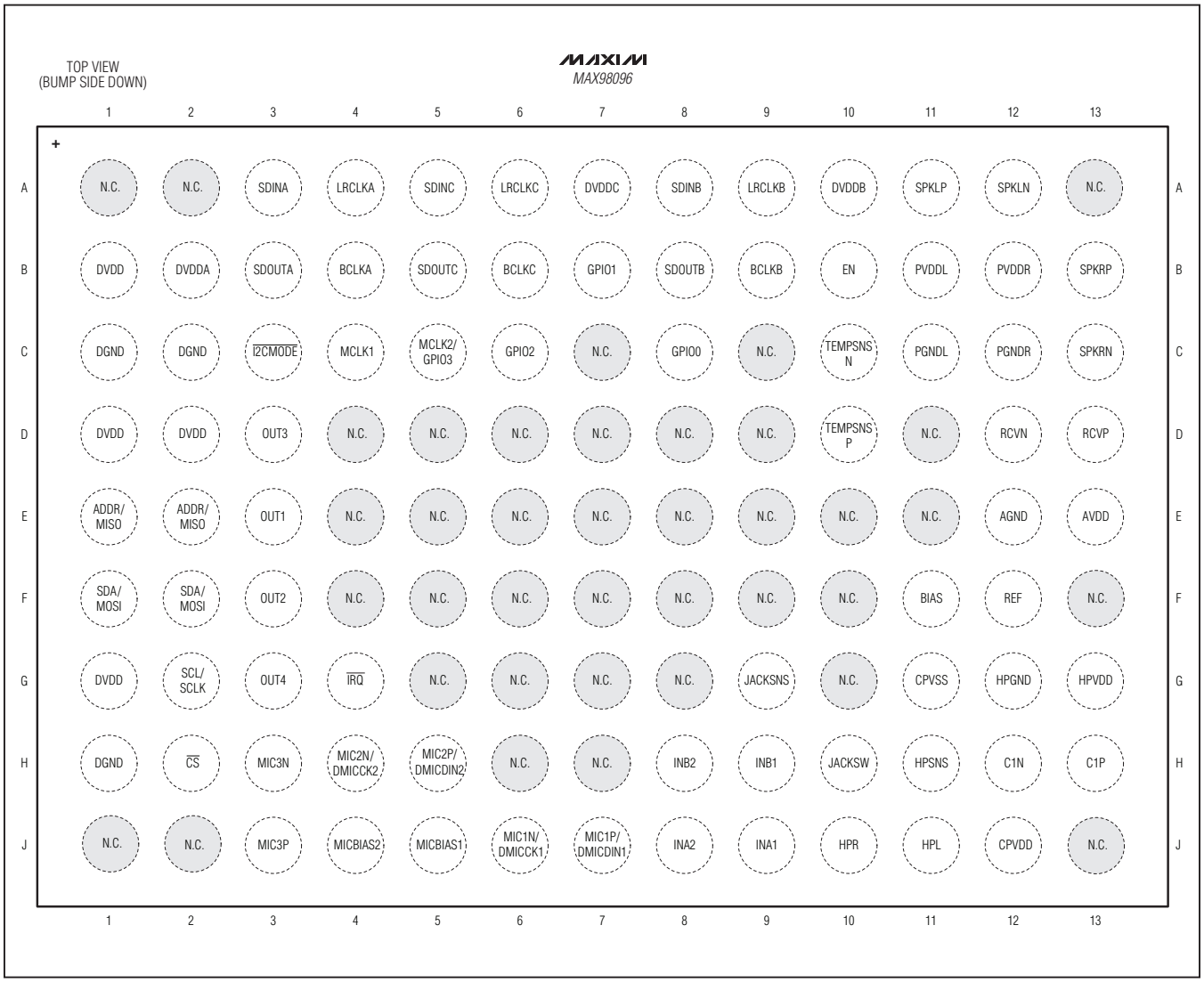


COMMON-MODE REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)



Audio Hub with Wideband FlexSound Processor

Bump Configuration



Bump Description

BUMP	NAME	LOGIC REFERENCE	FUNCTION
A1, A2, A3, C7, C9, D4–D9, D11, E4–E11, F4–F10, F13, G5–G8, G10, H6, H7, J1, J2, J13	N.C.	—	No Connection. Not internally connected. Use to route other signals as necessary.
A3	SDINA	DVDDA	Digital Audio Port A Serial-Data Input (DAC Input)
A4	LRCLKA	DVDDA	Digital Audio Port A Left-Right Clock Input/Output. LRCLKA is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLKA is a frame sync pulse. LRCLKA is an input when the IC is in slave mode and an output when in master mode.
A5	SDINC	DVDDC	Digital Audio Port C Serial-Data Input (DAC Input)
A6	LRCLKC	DVDDC	Digital Audio Port C Left-Right Clock Input/Output. LRCLKC is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLKC is a frame sync pulse. LRCLKC is an input when the IC is in slave mode and an output when in master mode.
A7	DVDDC	—	Digital Audio Port C Power-Supply Input. Bypass to DGND with a 0.1µF capacitor.
A8	SDINB	DVDDB	Digital Audio Port B Serial-Data Input (DAC Input)
A9	LRCLKB	DVDDB	Digital Audio Port B Left-Right Clock Input/Output. LRCLKB is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLKB is a frame sync pulse. LRCLKB is an input when the IC is in slave mode and an output when in master mode.
A10	DVDDB	—	Digital Audio Port B Power Supply Input. Bypass to DGND with a 0.1µF capacitor.
A11	SPKLP	—	Positive Left-Channel Class D Speaker Amplifier Output
A12	SPKLN	—	Negative Left-Channel Class D Speaker Amplifier Output
B1, D1, D2, G1	DVDD	—	Digital Power Supply. Supply for the digital core. Bypass to DGND with a 1µF capacitor.
B2	DVDDA	—	Digital Audio Port A Power-Supply Input. Bypass to DGND with a 0.1µF capacitor.
B3	SDOUTA	DVDDA	Digital Audio Port A Serial-Data Output (ADC Output)
B4	BCLKA	DVDDA	Digital Audio Port A Bit Clock Input/Output. BCLKA is an input when the IC is in slave mode and an output when in master mode.
B5	SDOUTC	DVDDC	Digital Audio Port C Serial-Data Output (ADC Output)
B6	BCLKC	DVDDC	Digital Audio Port C Bit Clock Input/Output. BCLKC is an input when the IC is in slave mode and an output when in master mode.
B7	GPIO1	DVDDB	General-Purpose Input/Output 1
B8	SDOUTB	DVDDB	Digital Audio Port B Serial-Data Output (ADC Output)
B9	BCLKB	DVDDB	Digital Audio Port B Bit Clock Input/Output. BCLKB is an input when the IC is in slave mode and an output when in master mode.

Bump Description (continued)

BUMP	NAME	LOGIC REFERENCE	FUNCTION
B10	EN	—	Device Enable. Connect high to any supply other than DVDD to enable the device. Connect low to place the entire device in the lowest power mode.
B11	PVDDL	—	Left Speaker Amplifier Power Supply. Bypass to PGNDL with a 1µF and a 10µF capacitor.
B12	PVDDR	—	Right Speaker Amplifier Power Supply. Bypass to PGNDR with a 1µF capacitor.
B13	SPKRP	—	Positive Right-Channel Class D Speaker Amplifier Output
C1, C2, H1	DGND	—	Digital Ground
C3	$\overline{\text{I2CMODE}}$	DVDDA	Active-Low I²C Mode Select. Set low for I²C mode, set high for SPI mode.
C4	MCLK1	DVDDA	Master Clock Input 1. Acceptable input frequency range is 10MHz to 60MHz.
C5	MCLK2/ GPIO3	DVDDB	Master Clock Input 2 or General Purpose Input/Output 3. Acceptable input frequency range is 10MHz to 60MHz when used as a master clock input.
C6	GPIO2	DVDDB	General Purpose Input/Output 2
C8	GPIO0	DVDDB	General Purpose Input/Output 0
C10	TEMPSNSN	—	Negative External Temperature Sensing Diode Input
C11	PGNDL	—	Left Speaker Amplifier Ground
C12	PGNDR	—	Right Speaker Amplifier Ground
C13	SPKRN	—	Negative Right-Channel Class D Speaker Amplifier Output
D3	OUT3	—	Line Output 3. Single-ended output.
D10	TEMPSNSP	—	Positive External Temperature Sensing Diode Input
D12	RCVN	—	Negative Receiver Amplifier Output
D13	RCVP	—	Positive Receiver Amplifier Output
E1, E2	ADDR/ MISO	AVDD/ DVDDA	I²C Bits 1 and 0 of Slave Address or SPI Data Output. Logic referenced to AVDD in I²C mode and to DVDDA in SPI mode.
			$V_{ADDR/MISO}$ / **BINARY SLAVE ADDRESS**
			V_{AGND} / 0010000(R$\overline{W}$)
			V_{DVDDA} / 0010001(R$\overline{W}$)
			$V_{SCL/SCLK}$ / 0010011(R$\overline{W}$)
E3	OUT1	—	Line Output 1
E12	AGND	—	Analog Ground
E13	AVDD	—	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
F1, F2	SDA/MOSI	AVDD/ DVDDA	I²C Serial-Data Input/Output or SPI Data Input. Connect a pullup resistor to DVDDA for full output swing in I²C mode (logic referenced to AVDD in I²C mode and to DVDDA in SPI mode).
F3	OUT2	—	Line Output 2. Single-ended output or negative differential output.

BUMP Description (continued)

BUMP	NAME	LOGIC REFERENCE	FUNCTION
F11	BIAS	—	Common-Mode Voltage Reference. Bypass to AGND with a 1µF capacitor.
F12	REF	—	Converter Reference. Bypass to AGND with a 2.2µF capacitor.
G2	SCL/SCLK	AVDD/ DVDDA	I²C/SPI Serial-Clock Input (logic referenced to AVDD in I²C mode and to DVDDA in SPI mode)
G3	OUT4	—	Line Output 4. Single-ended output.
G4	$\overline{IRQ}$	—	Hardware Interrupt Output. $\overline{IRQ}$ can be programmed to pull low when bits in the status registers change states. Read the corresponding status register to clear $\overline{IRQ}$ once set. Repeated interrupts have no effect on $\overline{IRQ}$ until it is cleared. Connect a pullup resistor (10kΩ recommended) to configure the for full output swing. See the *Interrupt ($\overline{IRQ}$)* section for more information.
G9	JACKSNS	—	Jack Sense. Connect to the microphone terminal of a 4-pole 3.5mm jack to detect microphone presence, insertion, and removal. See the *Headset Detection* section.
G11	CPVSS	—	Inverting Charge-Pump Output. Bypass to HPGND with a 1µF ceramic capacitor.
G12	HPGND	—	Headphone Amplifier and Charge-Pump Ground
G13	HPVDD	—	Headphone Amplifier and Charge-Pump Power Supply. Bypass to HPGND with a 10µF capacitor.
H2	$\overline{CS}$	DVDDA	SPI Chip Select. Connect to DVDDA for I²C mode. The IC latches into SPI mode on the falling edge of $\overline{CS}$.
H3	MIC3N	—	Negative Differential Microphone 3 Input. AC-couple to a microphone with a series capacitor.
H4	MIC2N/ DMICCK2	AVDD	Negative Differential Microphone 2 Input. AC-couple to a microphone with a series capacitor. Can be retasked as a digital microphone clock output.
H5	MIC2P/ DMICDIN2	AVDD	Positive Differential Microphone 2 Input. AC-couple to a microphone with a series capacitor. Can be retasked as a digital microphone data input.
H8	INB2	—	Single-Ended Line Input B2 or Positive Differential Line Input B
H9	INB1	—	Single-Ended Line Input B1 or Negative Differential Line Input B
H10	JACKSW	—	Jack Switch Input. Connects to the mechanical switch on the headset jack if available.
H11	HPSNS	—	Headphone Amplifier Ground Sense. Connect to the headphone jack ground terminal or connect to ground.
H12	C1N	—	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
H13	C1P	—	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
J3	MIC3P	—	Positive Differential Microphone 3 Input. AC-couple to a microphone with a series capacitor.
J4	MICBIAS2	—	Low-Noise Microphone Bias Output. Outputs a 2.2V, 2.4V, 2.6V, or 2.8V microphone bias. Bypass to AGND with a 1µF capacitor. Use to bias the headset microphone.

BUMP Description (continued)

BUMP	NAME	LOGIC REFERENCE	FUNCTION
J5	MICBIAS1	—	Low-Noise Microphone Bias Output. Outputs a 2.2V, 2.4V, 2.6V, or 2.8V microphone bias. Bypass to AGND with a 1µF capacitor. Use to bias the internal microphones.
J6	MIC1N/ DMICCK1	AVDD	Negative Differential Microphone 1 Input. AC-couple to a microphone with a series capacitor. Can be retasked as a digital microphone clock output.
J7	MIC1P/ DMICDIN1	AVDD	Positive Differential Microphone 1 Input. AC-couple to a microphone with a series capacitor. Can be retasked as a digital microphone data input.
J8	INA2	—	Single-Ended Line Input A2 or Positive Differential Line Input A
J9	INA1	—	Single-Ended Line Input A1 or Negative Differential Line Input A
J10	HPR	—	Right-Channel Headphone Amplifier Output
J11	HPL	—	Left-Channel Headphone Amplifier Output
J12	CPVDD	—	Noninverting Charge-Pump Output. Bypass to HPGND with a 1µF ceramic capacitor.

Detailed Description

The MAX98096 is a fully integrated audio hub with FlexSound audio processing and integrated amplifiers.

Two differential microphone amplifiers can accept signals from three analog inputs. Two inputs can be retasked to support up to four digital microphones. A maximum of two analog microphones or four digital microphones can be recorded simultaneously. The analog signals are amplified by up to 50dB and recorded by the stereo ADC or routed to the output amplifiers for playback. The digital record path supports voice filtering with selectable preset highpass filters and high stopband attenuation at $f_S/2$.

The IC includes one analog line input amplifier with an input multiplexer. The input multiplexer selects between line input A and line input B. The line input supports either a stereo single-ended input or a mono differential input. The line inputs are preamplified and then routed either to the ADC for recording or to the output amplifiers for playback.

The IC provides three digital audio interfaces (DAIs) that can transmit and receive up to three different audio signals in a wide range of formats including I^2S, left justified, PCM, and up to four mono slots in TDM. Each interface can be connected to either of three audio ports (A, B and C) for communication with external devices. The interfaces support 8kHz to 96kHz sample rates. DAI1 supports stereo playback data and up to four channels of record data. DAI2 and DAI3 support mono playback and stereo record data.

The playback audio signals from all three DAIs are routed through both a fixed function DSP and the programmable FLEXSOUND DSP. The DAI1 and DAI2 playback paths include selectable highpass filters, a dynamic range controller (DRC), a 5-band parametric equalizer (EQ), and two programmable biquad filters. The DAI3 playback path includes only the selectable highpass filter.

The record audio path includes two channels from the stereo ADC and two channels dedicated to recording digital microphones. The two ADC digital filter channels can alternatively accept digital microphone data to enable a total of four digital microphones. The two ADC channels are routed through both a fixed-function record DSP and the programmable FlexSound DSP or directly to DAIs. The two dedicated digital microphone channels are routed through the FlexSound DSP or directly to DAIs. The fixed-function DSP provides gain control and voice/music filters to optimize voice or music mode.

When recording three or four digital microphones, the recorded audio can only be output on DAI1. When recording one or two analog or digital microphone signals the recorded audio can be output on any DAI. If more advanced signal routing is required, up to three sample rate converters can be enabled to allow each DAI's output data to be a mix of any playback or record audio signal regardless of sample rate.

The programmable FlexSound DSP intercepts all playback and record audio signals and allows advanced signal processing including single and dual microphone noise suppression, acoustic echo cancellation, speaker protection, and ambient noise compensation in the playback paths. If the FlexSound DSP is not required, it can be disabled completely, allowing audio signals to bypass the DSP.

Three sigma delta DACs convert any combination of playback audio signals for output through the analog amplifiers. The stereo DAC routes audio to all outputs. The mono DAC routes audio only to the stereo loudspeaker amplifier.

The IC includes a differential receiver amplifier, a stereo Class D speaker amplifier, a DirectDrive true ground stereo headphone amplifier, and four line outputs.

The stereo Class D amplifier provides efficient amplification for two speakers. The amplifier includes spread-spectrum modulation and active emissions limiting to minimize the radiated emissions (EMI) traditionally associated with Class D amplifiers. In most systems, no output filtering is required to meet standard EMI limits.

The Class H DirectDrive headphone amplifier uses an inverting charge pump to generate a ground referenced output signal. This eliminates the need for DC-blocking capacitors or a midrail bias for the headphone jack ground return. The Class H architecture optimizes the supply voltage output by the charge pump based on audio signal level to increase power efficiency. Ground sense reduces crosstalk and output noise caused by ground return current.

The headphone and speaker amplifier paths include downward expanders that monitor the digital signal level in each DAC and apply progressive attenuation to unwanted low-level audio signals.

The IC integrates jack detection and a keypress ADC to support common accessories that utilize a 3.5mm jack. Jack detection detects insertion, removal, and identifies the type of accessory. Supported accessories are earphones and headsets. A combination of mechanical and electrical detection is used to ensure robust operation. The keypress ADC enables single and multibutton accessories that apply resistive pulldowns on the microphone signal to indicate button presses to the system.

Analog Microphone Inputs

The IC includes three differential microphone inputs. Only two analog microphones can be recorded simultaneously. Analog microphone signals are amplified by two gain stages and then routed to the ADCs and/or bypassed to the output amplifiers (Figure 7). The first stage offers selectable 0dB, 20dB, or 30dB settings. The second stage is a programmable gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps. To maximize signal-to-noise ratio use the gain in the first stage whenever possible. A zero-crossing detection is included on the PGA to minimize zipper noise when making gain changes. MIC1_ and MIC2_ inputs can also be used for digital microphones. See the *Digital Microphone Inputs* section for more details.

Table 1. Microphone Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
LEVEL CONTROL		
0x5F	Microphone 1 Input Level	0
0x60	Microphone 2 Input Level	0
CONFIGURATION		
0x87	Microphone	0

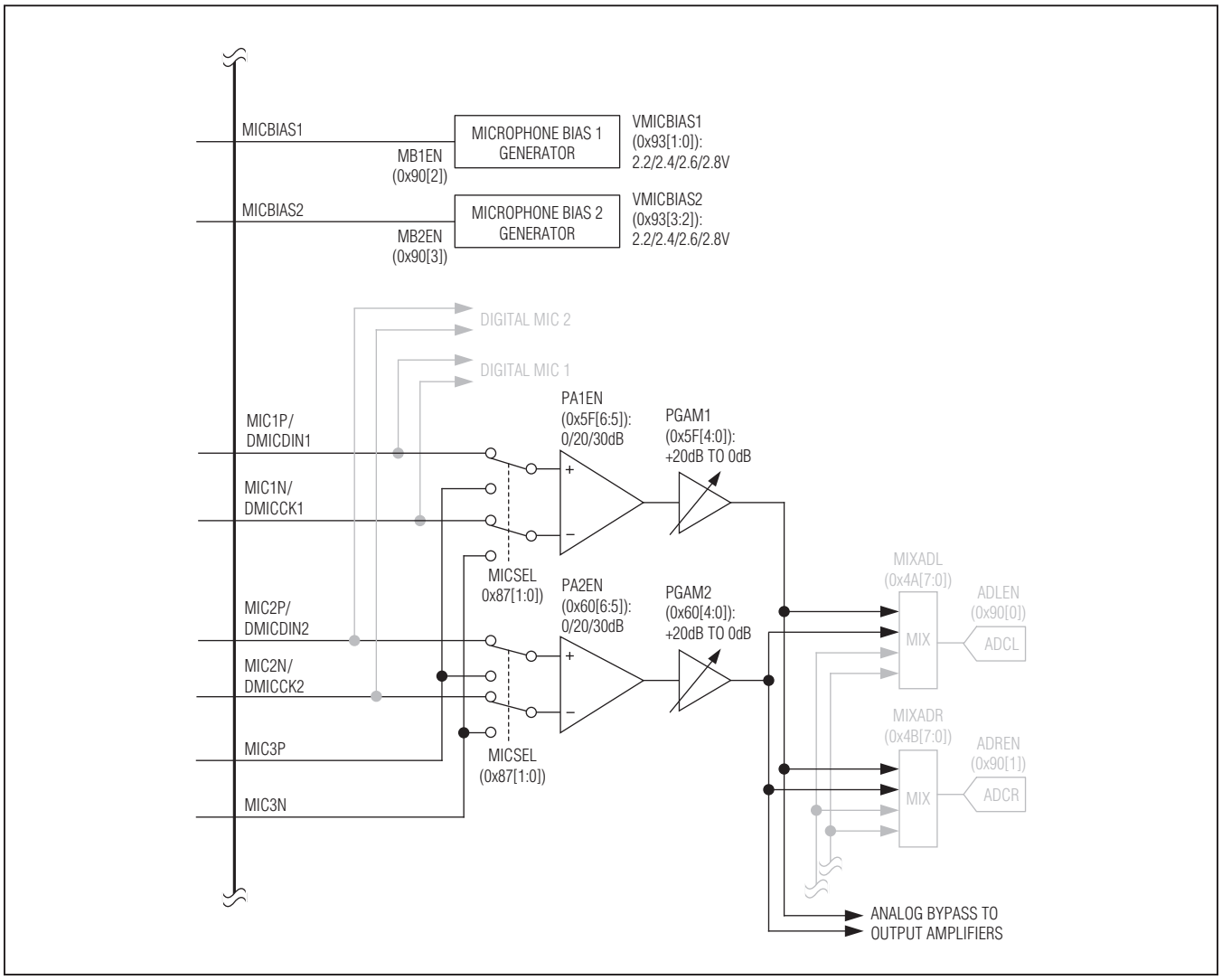


Figure 7. Analog Microphone Block Diagram

Microphone Bias

The IC features two low noise microphone biases for powering the microphones. Each microphone bias can independently be set to 2.2V, 2.4V, 2.6V, or 2.8V.

Table 2. Microphone Bias Register Name and Address

ADDRESS	REGISTER NAME	PAGE
POWER MANAGEMENT		
0x90	Input Enable	0
0x93	Bias Control	0

Digital Microphone Inputs

The IC can input up to four digital microphones. Digital microphone left 1 and digital microphone right 1 are routed through the record path DSP and can be routed to any of the DAIs. The record path DSP is automatically switched to the digital microphones when digital microphone left 1 and/or digital microphone right 1 are enabled. Digital microphone left 2 and digital microphone right 2 are routed directly to the FlexSound DSP for processing or output on DAI1 to an external device in slot 3 and 4 of TDM mode. The ADC must be enabled when using digital microphone 2. DAI1 is automatically selected for TDM mode when digital microphone left 2 and/or digital microphone right 2 is enabled. The analog and digital microphone pins are shared. MIC1 or MIC2 and MIC3 are available when one or two digital microphones are connected, not for simultaneously use. MIC3 is available when three or four digital microphones are connected, not for simultaneously use.

Table 3. Digital Microphone Register Name and Address

ADDRESS	REGISTER NAME	PAGE
CONFIGURATION		
0x87	Microphone	0

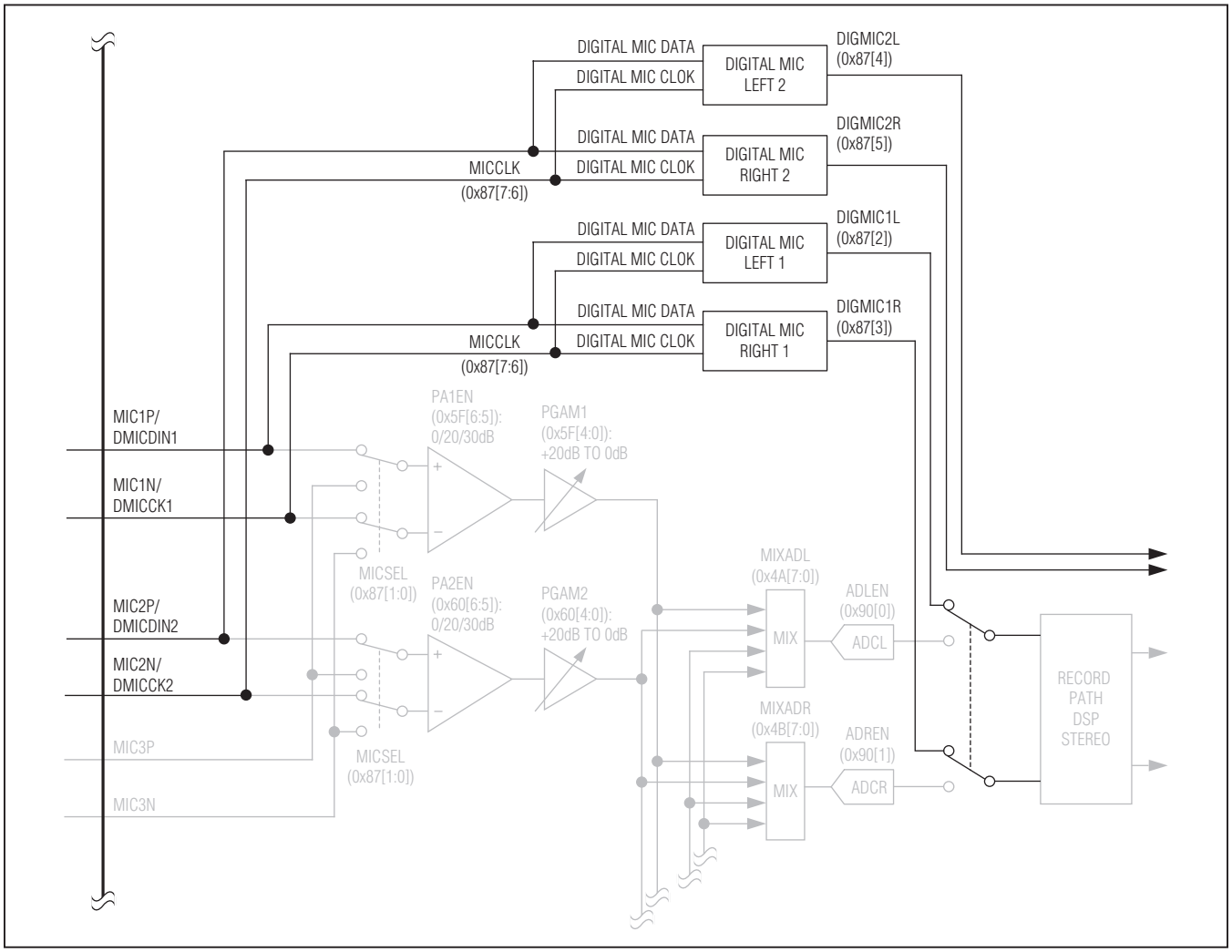


Figure 8. Digital Microphone Block Diagram

Line Inputs

The IC includes stereo single-ended line input amplifier or mono differential line input amplifier (Figure 9). The line input amplifier is multiplexed between two sets of inputs, INA_ and INB_. The line input includes adjustable gain to match a wide range of input signal levels. An external gain mode provides a trimmed feedback resistor for a custom gain. Set the custom gain by choosing the appropriate input resistor and using the following formula:

$$AV_{PGAIN} = 20 \times \log\left(\frac{20k}{R_{IN}}\right)$$

The external gain mode also allows summing multiple signals into a single input, by connecting multiple input resistors as show in Figure 10. The external gain mode also allows input signals larger than $1V_{P-P}$.

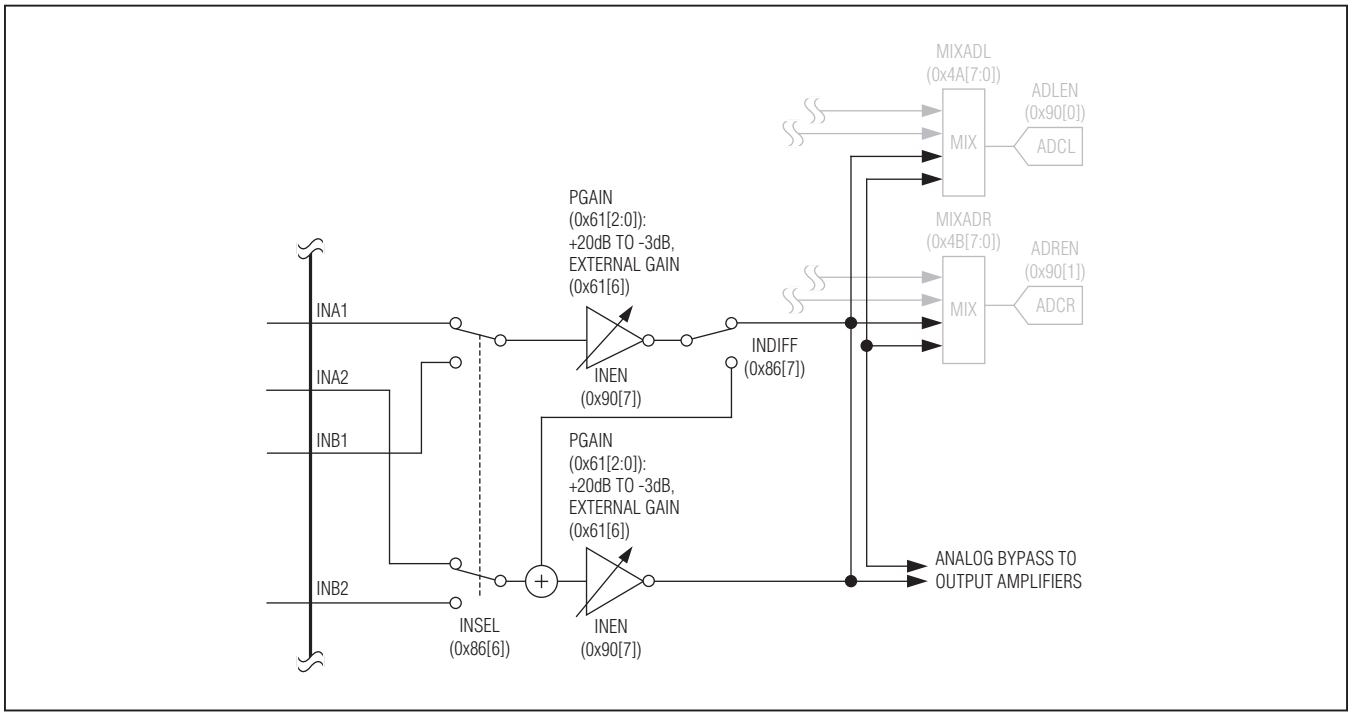


Figure 9. Line Input Block Diagram

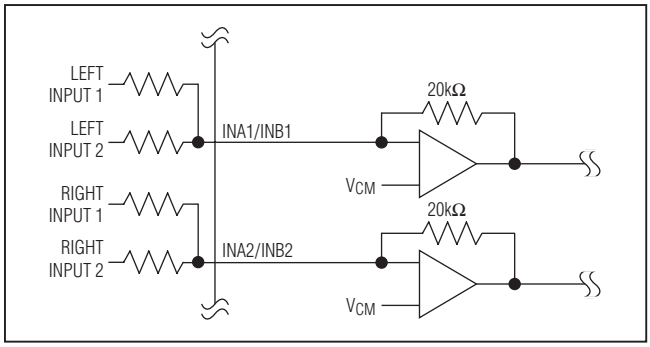


Figure 10. Summing Multiple Signals at the Line Inputs

Table 4. Line Input Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
LEVEL CONTROL		
0x61	Line Input Level	0
CONFIGURATION		
0x86	Line Input/Output	0
POWER MANAGEMENT		
0x90	Input Enable	0

ADC Input Mixers

The IC's stereo ADC accepts input from the microphone amplifiers and line input amplifiers. The ADC mixer routes any combination of the four analog audio inputs to the left and right ADCs.

Record Path Signal Processing (Record DSP)

The IC's record signal path includes two digital gain stages and a selection of voice filters or music filter with an optional DC-blocking filter. Figure 11 shows the detailed signal path. The first stage offers selectable 0dB, 6dB, 12dB or 18dB settings. The second stage is a record level control from -12dB to +3dB in 1dB steps. The option of voice or music filters is set to the same configuration as the filters in the playback DSP that is providing the ADC clock. For an example, when the ADC clock and output is set to DAI1, the filter settings are shared by the settings in the DAI1 playback DSP. See the *Selectable Highpass Filtering* section for more information. DAI3 only has voice filters.

Table 5. ADC Input Mixers Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
MIXERS		
0x4A	Left ADC	0
0x4B	Right ADC	0

Table 6. Record DSP Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
ADC CLOCK CONTROL		
0x45	ADC Clock Mode	0
LEVEL CONTROL		
0x5D	Left ADC Level	0
0x5E	Right ADC Level	0

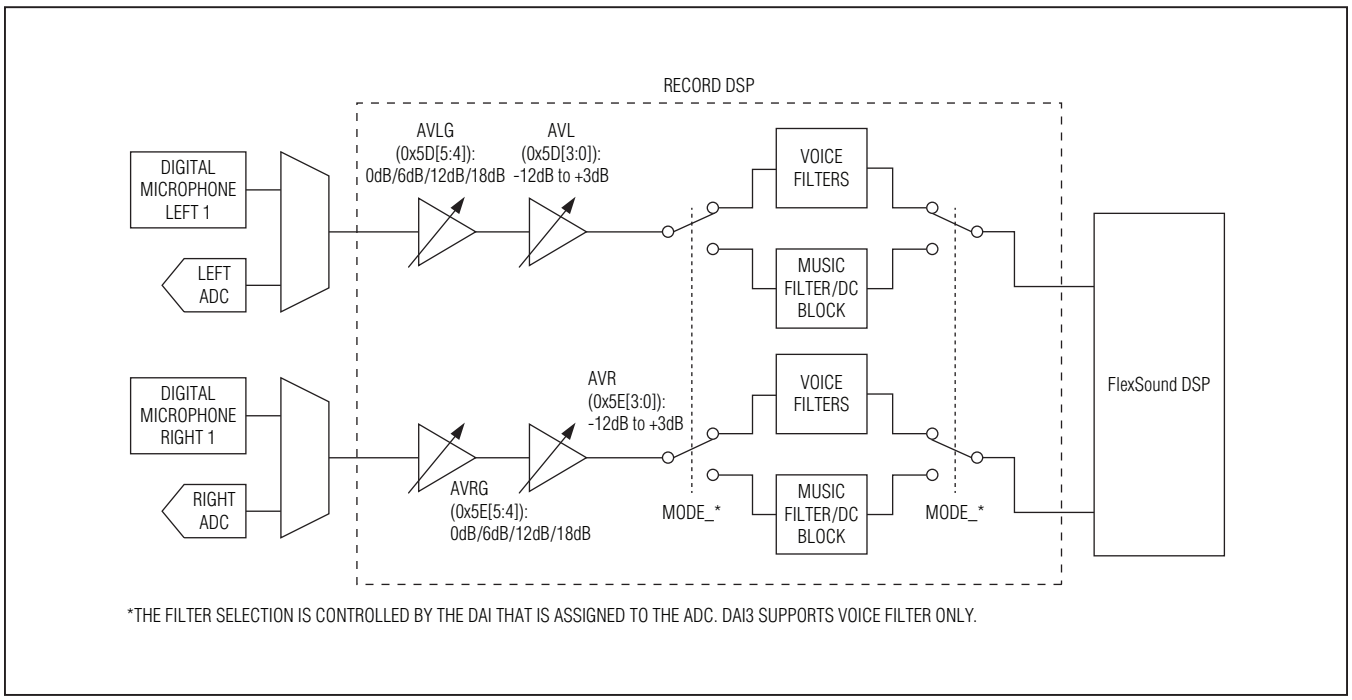


Figure 11. Record Path Signal Processing

Sidetone

Enable sidetone during full-duplex operation to add a low-level copy of the recorded audio signal to the playback audio signal (Figure 12). Sidetone is commonly used in telephony to allow the speaker to hear himself/herself speak, providing a more natural user experience. Sidetone only works in voice mode. The IC implements sidetone digitally to help prevent unwanted feedback into the playback signal path and better matches the playback audio signal. DAI1 and DAI2 sidetone are controlled by the same register bits. DAI3 sidetone is controlled by its own register bits.

Table 7. Sidetone Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
LEVEL CONTROL		
0x56	Sidetone DAI1/2	0
0x57	Sidetone DAI3	0

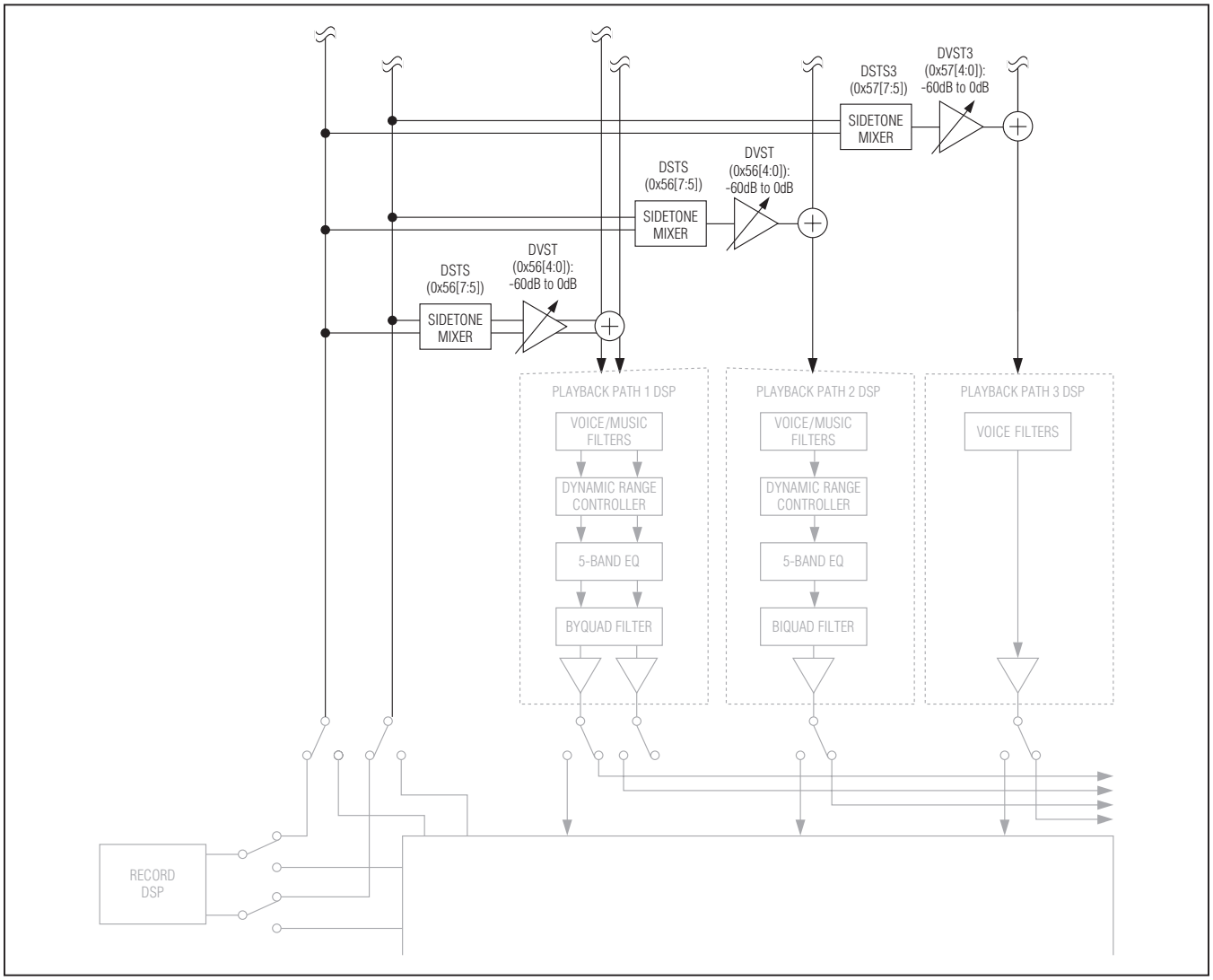


Figure 12. Sidetone Block Diagram

Digital Audio Interfaces

The IC features three DAIs that can be configured in a variety of formats including left justified, I²S, PCM, and time division multiplexed (TDM). When in TDM mode the IC supports up to 4 mono audio slots in each frame. The IC can use up to 2 mono slots per interface, leaving the remaining two slots available for another device. DAI1 can output on all 4 mono slots when using 4 digital microphones. DAI 1 is automatically selected for TDM mode when digital microphone left 2 and/or right 2 are enabled. Table 8 shows how to configure the device for common digital audio formats. Figure 14 and Figure 15 show examples of common audio formats. By default, SDOUTA/SDOUTB/SDOUTC are set high impedance when the IC is not outputting data to facilitate sharing the bus. Configure the interface in TDM mode using only slot 1 to transmit and receive mono PCM voice data. Any of the DAIs can be routed to any of the ports (PORT A, PORTB, or PORTA).

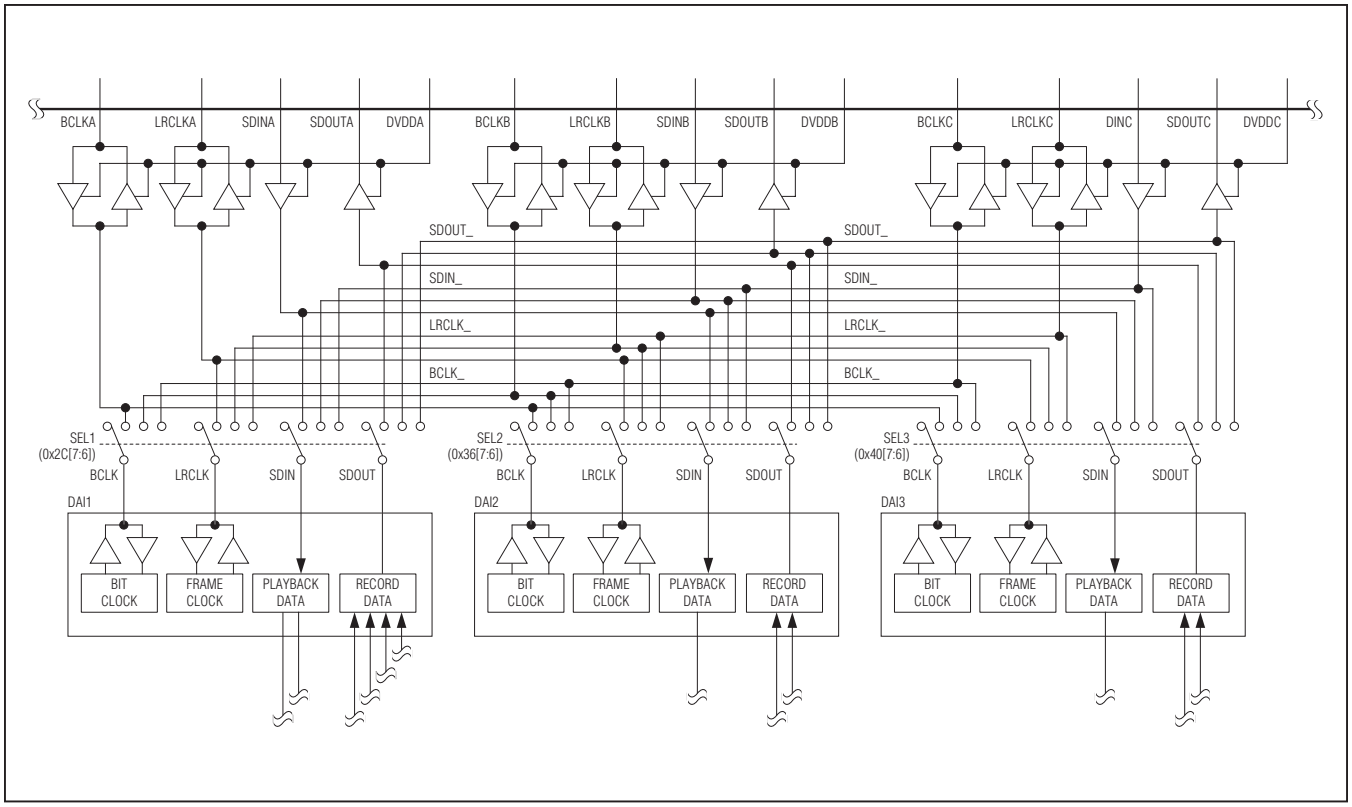


Figure 13. Digital Audio Interfaces Block Diagram

Table 8. Common Digital Audio Formats

MODE	WCI_	BCI_	DLY_	TDM_	SLOTL_	SLOTR_
Left Justified	1	0	0	0	X	X
I²S	0	0	1	0	X	X
TDM	X	1	X	1	Set as desired	

X = Don't care.

Table 9. Digital Audio Interface Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
DAI1 CONFIGURATION		
0x2A	DAI1 Format	0
0x2C	DAI1 I/O Configuration	0
0x2D	DAI1 Time-Division Multiplex	0
DAI2 CONFIGURATION		
0x34	DAI2 Format	0
0x36	DAI2 I/O Configuration	0
0x37	DAI2 Time-Division Multiplex	0
DAI3 CONFIGURATION		
0x3E	DAI3 Format	0
0x40	DAI3 I/O Configuration	0
0x41	DAI3 Time-Division Multiplex	0

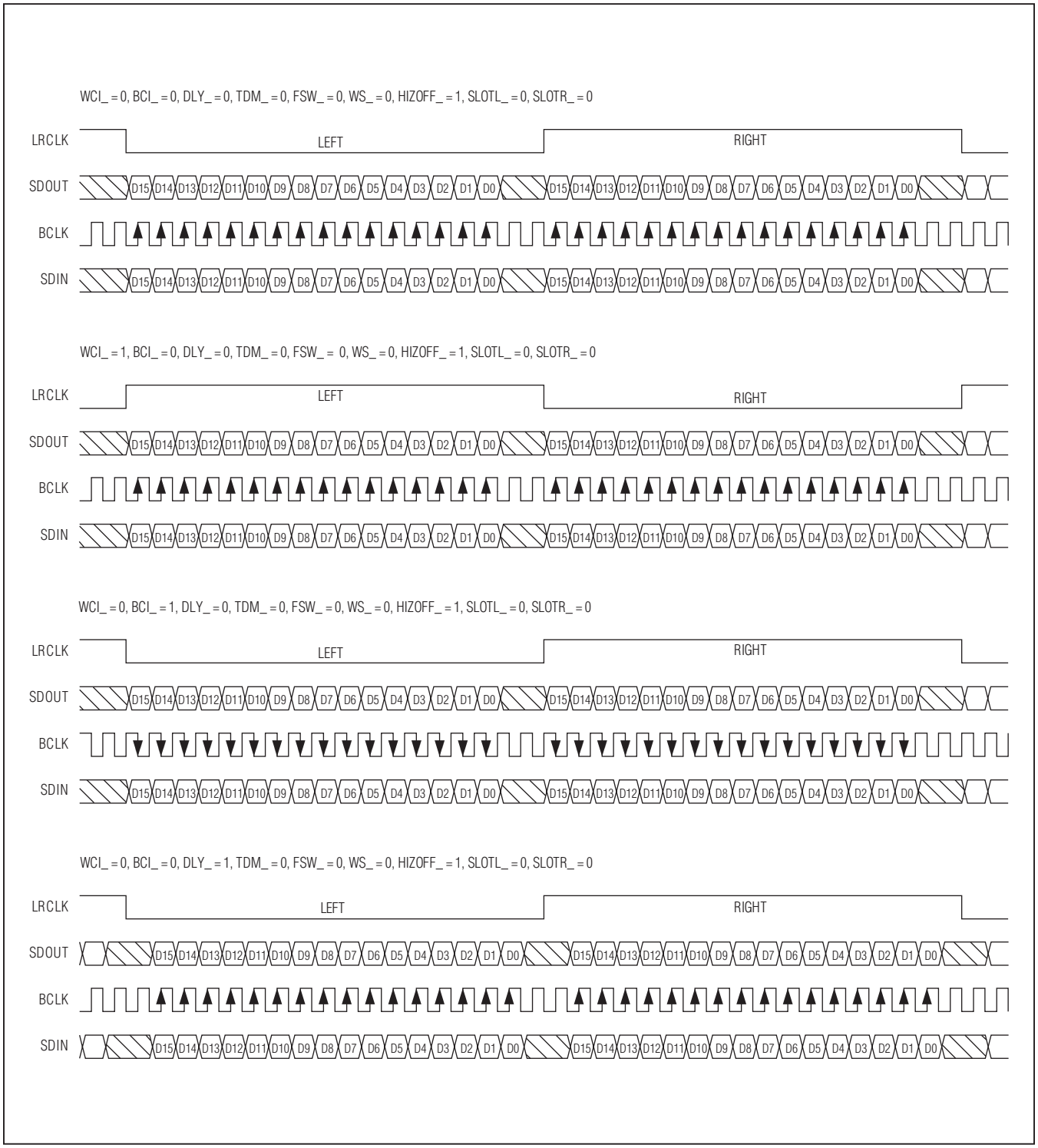


Figure 14. Non-TDM Data Format Examples

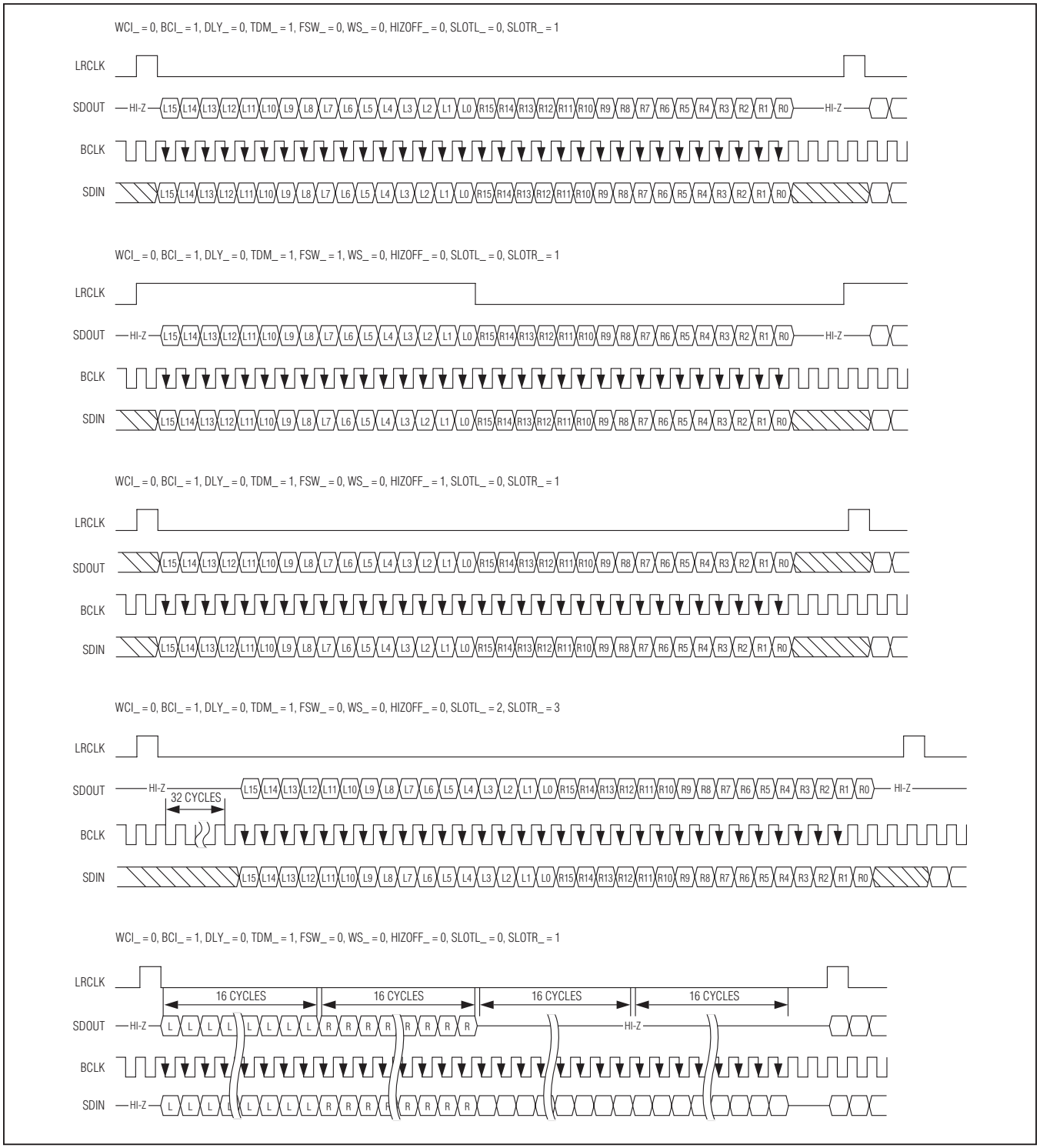


Figure 15. TDM Mode Data Format Examples

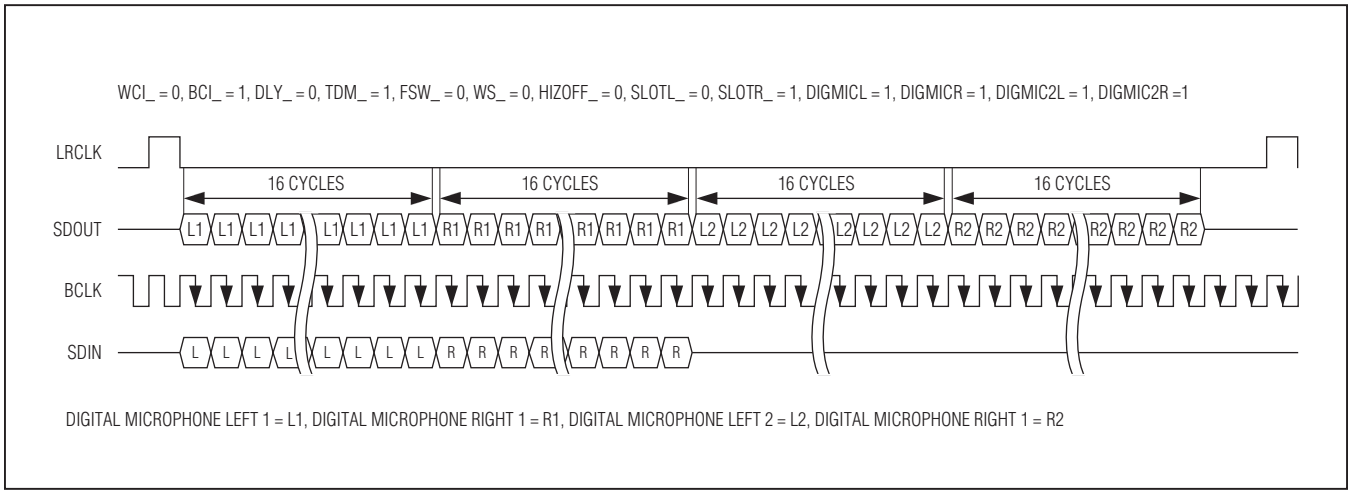


Figure 16. TDM Mode Data Format Examples (Cont.)

Clock Control

The digital signal paths in the IC require a master clock (MCLK) between 10MHz and 60MHz to function. Internally, the IC requires a clock between 10MHz and 20MHz. A prescaler divides MCLK by 1, 2, or 4 to create the internal clock called PCLK. PCLK is used as a reference clock for all portions of the IC.

The IC includes three playback digital audio signal paths and a record signal path, all capable of supporting any sample rate from 8kHz to 96kHz. Each path is independently configured to allow different sample rates. To accommodate a wide range of system architectures, four main clocking modes are supported:

- **PLL Mode:** When operating in slave mode, enable the PLL to lock onto any LRCLK input. This mode requires the least configuration, but provides the lowest performance. Use this mode to simplify initial startup or when normal mode and exact integer mode cannot be used.
- **Normal Mode:** This mode uses a 15-bit clock divider to set the sample rate relative to PCLK. This allows high flexibility in both the PCLK and LRCLK frequencies and can be used in either master or slave mode (Table 10).

Table 10. Common NI1/2 Values

PCLK (MHz)	LRCLK (kHz)											
	DHF1/2 = 0									DHF1/2 = 1		
	8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**	**64**	**88.2**	**96**
10	13A9	1B18	1D7E	2752	3631	3AFB	4EA5	6C61	75F7	4EA5	6C61	75F7
11	11E0	18A2	1ACF	23BF	3144	359F	477E	6287	6B3E	477E	6287	6B3E
11.2896	116A	**1800**	1A1F	22D4	**3000**	343F	45A9	**6000**	687D	45A9	**6000**	687D
12	1062	1694	1893	20C5	2D29	3127	4189	5A51	624E	4189	5A51	624E
12.288	**1000**	160D	**1800**	**2000**	2C1A	**3000**	**4000**	5833	**6000**	**4000**	5833	**6000**
13	F20	14D8	16AF	1E3F	29AF	2D5F	3C7F	535F	5ABE	3C7F	535F	5ABE
16	C4A	10EF	126F	1893	21DE	24DD	3127	43BD	49BA	3127	43BD	49BA
16.9344	B9C	**1000**	116A	1738	**2000**	22D4	2E71	**4000**	45A9	2E71	**4000**	45A9
18.432	AAB	EB3	**1000**	1555	1D66	**2000**	2AAB	3ACD	**4000**	2AAB	3ACD	**4000**
20	9D5	D8C	EBF	13A9	1B18	1D7E	2752	3631	3AFB	2752	3631	3AFB

***Note: Bold** values are exact integers that provide maximum full-scale performance.*

- **Exact Integer Mode (DAI1 only):** In both master and slave mode, common MCLK frequencies (12MHz, 13MHz, 16MHz, and 19.2MHz) can be programmed to operate in exact integer mode for both 8kHz and 16kHz sample rates. In these modes, the MCLK and LRCLK rates are selected by using the FREQ1 bits instead of the NI and PLL control bits.
- **DAC Low Power Mode:** This mode bypasses the PLL for reduced power consumption and uses fixed counters to generate the clocks. The DAI_DAC_LP bits override the other clock settings.

Digital Signal Routing

The IC provides for a wide range of signal routing options. Three sample rate conversion filters allow any of the playback digital audio signals to mix with any other DAI regardless of sample rate. The sample rate converters filter out the higher frequency content for down conversion. The ADC output must be routed through a playback DSP before it can be sample rate converted. The ADC can be configured to operate at any one of the three playback sample rates. The left ADC is routed to the SRC mixers for DAI2 and DAI3, while the right ADC is connected directly to DAI2 and DAI3, as shown in Figure 17. DAI1 data get mixed to mono for DAI2 and DAI3. Sidetone is available in all configurations; see the *Sidetone* section for more information. Figure 17 shows the digital signal path between the DSPs and the DAIs.

Sample Rate Converter

The IC feature a sample rate converter (SRC) filter for each of the playback DAI paths to filter out the higher frequency content before converting to a lower sample rate. Any of the playback data can be routed any of the three DAI outputs regardless of the sample rate of the output DAI. The SRC mixer can mix any of the DAI playback data and the record data. The record data from the ADC does not go through the SRC filter. The record data must go through sidetone before converting the sample rate for given DAI other than the one assigned to the ADC.

Table 11. Clock Control Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
CODEC CLOCK CONTROL		
0x26	CODEC Clock Configuration	0
DAI1 CLOCK CONTROL		
0x27	DAI1 Clock Mode	0
0x28	DAI1 Any Clock Control	0
0x29	DAI1 Any Clock Control	0
DAI1 CONFIGURATION		
0x2B	DAI1 Clock	0
DAI2 CLOCK CONTROL		
0x31	DAI2 Clock Mode	0
0x32	DAI2 Any Clock Control	0
0x33	DAI2 Any Clock Control	0
DAI2 CONFIGURATION		
0x35	DAI1 Clock	0
DAI3 CLOCK CONTROL		
0x3B	DAI3 Clock Mode	0
0x3C	DAI3 Any Clock Control	0
0x3D	DAI3 Any Clock Control	0
DAI3 CONFIGURATION		
0x3F	DAI3 Clock	0
DAC CONTROL		
0x46	DAC Control 1	0

Table 12. Digital Signal Routing Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
DAI1 CONFIGURATION		
0x2E	DAI1 Filter	0
DAI1 SDOUT		
0x2F	DAI1 Level Control	0
0x30	DAI1 Level Control	0
DAI2 CONFIGURATION		
0x38	DAI2 Filter	0
DAI2 SDOUT		
0x39	DAI2 Level Control	0
0x3A	DAI2 Level Control	0
DAI3 CONFIGURATION		
0x42	DAI3 Filter	0
DAI3 SDOUT		
0x43	DAI3 Level Control	0
0x44	DAI3 Level Control	0

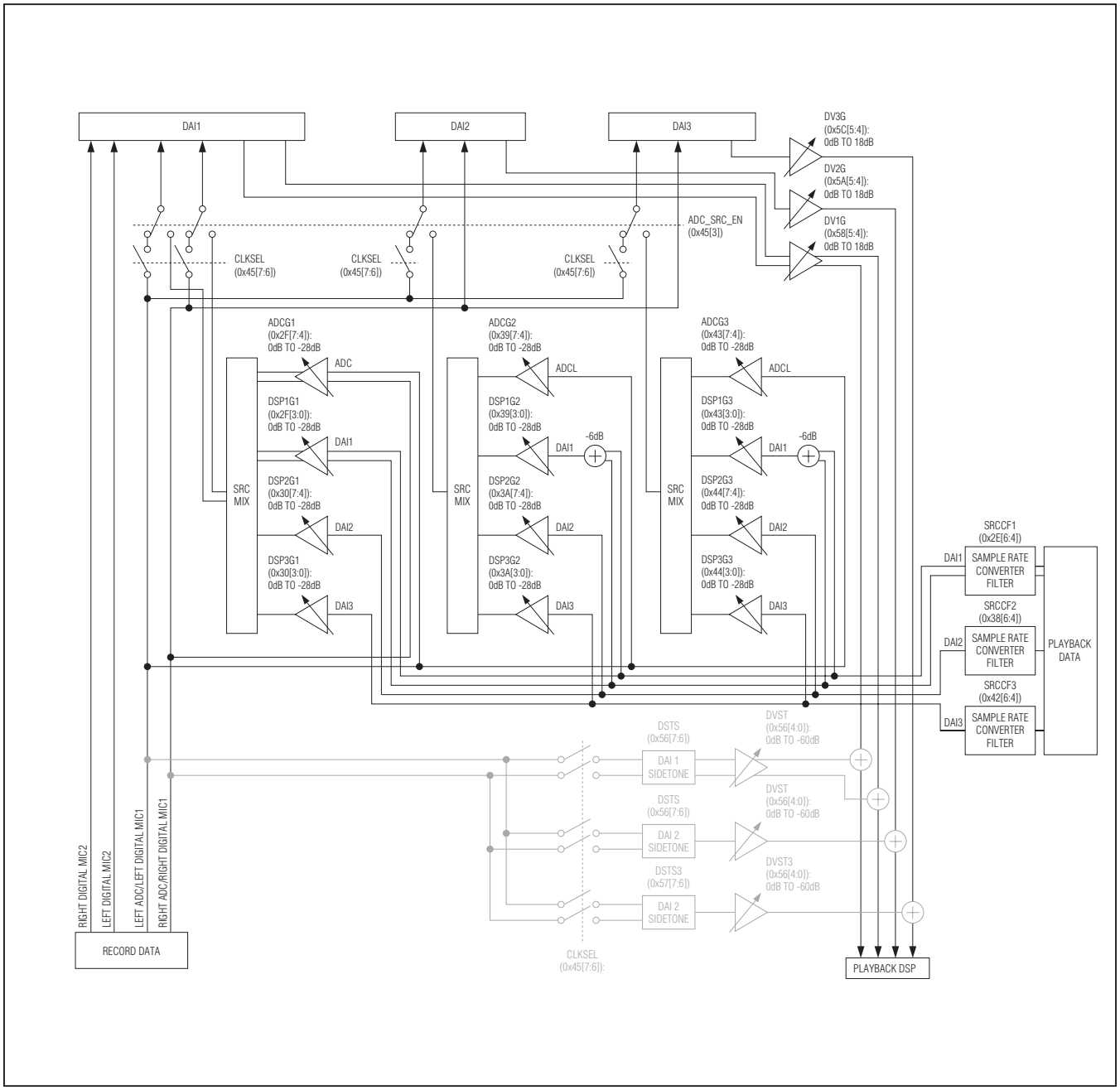


Figure 17. Detailed Digital Signal Routing Diagram

Playback Path Signal Processing (Playback DSP)

The playback signal path includes separate processing for each of the three paths. Signal processing features include voiceband filters, dynamic range controller (DRC), a five-band parametric equalizer (EQ), two biquad filers, and programmable attenuation. Figure 18 shows the complete signal path.

Selectable Highpass Filtering

Each digital signal path in the IC includes options for defining the path bandwidth. Use voice mode when the sample rate is 24kHz or less. The voice IIR filters provide greater than 70dB stopband attenuation at frequencies above $f_S/2$ to reduce aliasing. Three selectable highpass filters eliminate unwanted low-frequency signals.

Use music mode when processing high fidelity audio content. Music mode is only available for DAI1 and DAI2. The music FIR filters reduce power consumption and are linear phase to maintain stereo imaging. An optional DC-blocking filter is available to eliminate unwanted DC offset. For sample rates greater than 50kHz, a second set of FIR filters are available. Table 13 and Table 14 show the available filter responses.

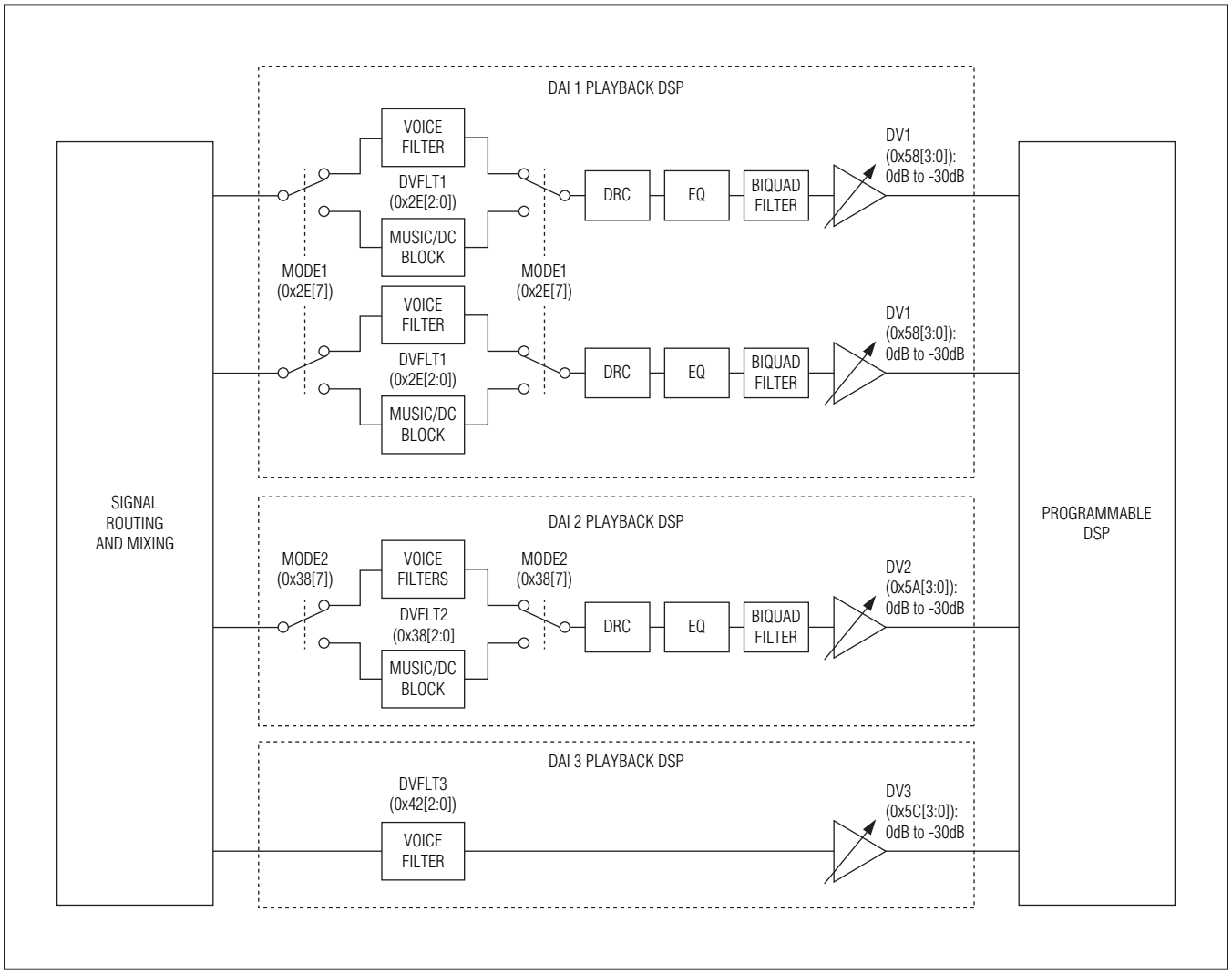


Figure 18. Fixed Function Playback Signal Processing

Table 13. Voice/Music Lowpass Filters

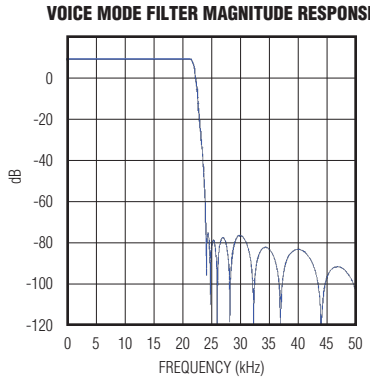
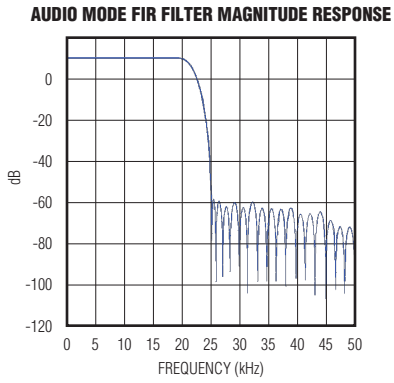
MODE_	FILTER RESPONSE
0	
1	

Table 14. Voice Highpass Filters

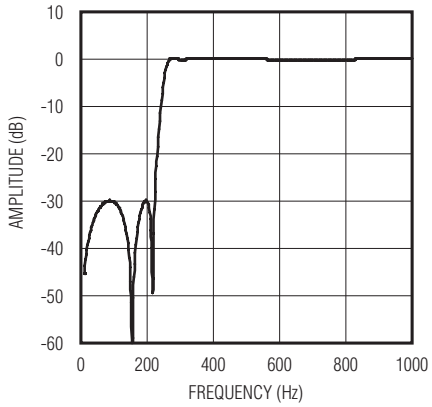
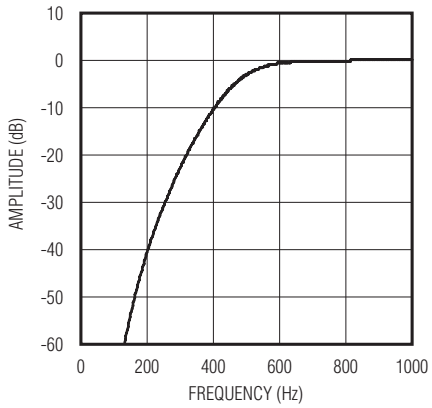
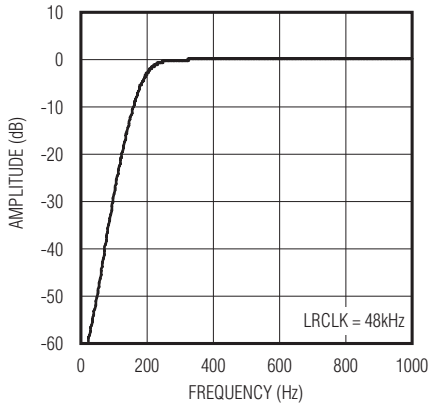
AVPTL/DVFLT VALUE	INTENDED SAMPLE RATE	FILTER RESPONSE
000	N/A	Disabled
001/011	16kHz/8kHz	
010/100	16kHz/8kHz	
101	8kHz to 48kHz	
110, 111	N/A	Reserved

Table 15. Selectable Highpass Filter Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
DAI1 CONFIGURATION		
0x2E	DAI1 Filter	0
DAI2 CONFIGURATION		
0x38	DAI2 Filter	0
DAI3 CONFIGURATION		
0x42	DAI3 Filter	0

Dynamic Range Control (DRC)

The DRC provides multiband programmable compression and expansion to both the DAI1 and DAI2 playback paths. Figure 19 shows the DRC gain response. The DRC can process the audio spectrum in up to three bands (Figure 20). Figure 21 shows the structure of the DRC 3-band crossover filter. Band 1 is a low-pass filter. Band 3 is a high-pass filter. Band 2 is the middle band that is created by subtracting Band 1 and Band 3 with the input data. Use BAND 2 for single band operation and BAND 1 and BAND 2 for two band operation.

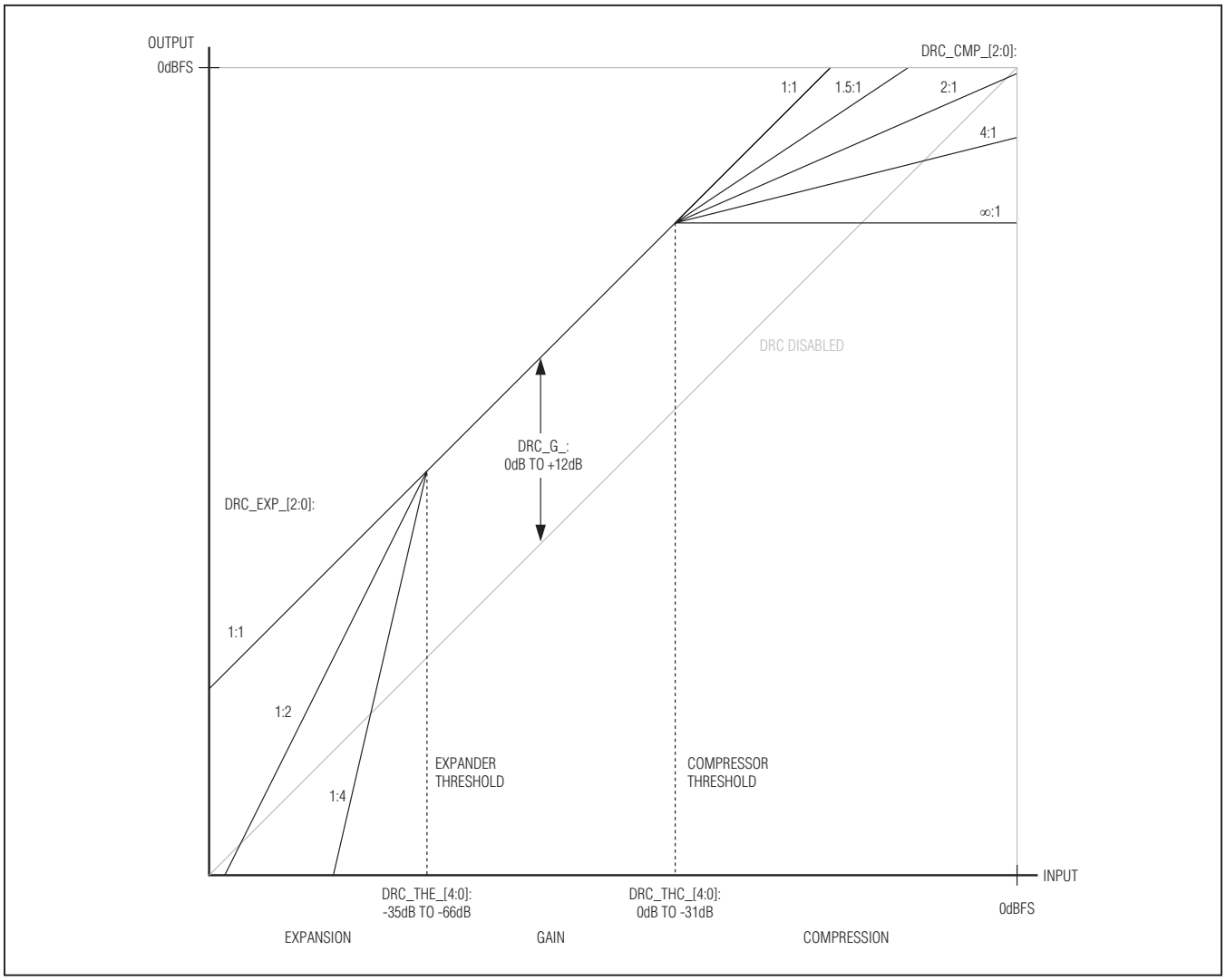


Figure 19. DRC Gain Response

The compressor attenuates high-amplitude signals and allows for a higher gain setting to be selected without clipping the output signal. This increases the perceived loudness of the audio signal and maintains a stable output amplitude despite changes in input amplitude.

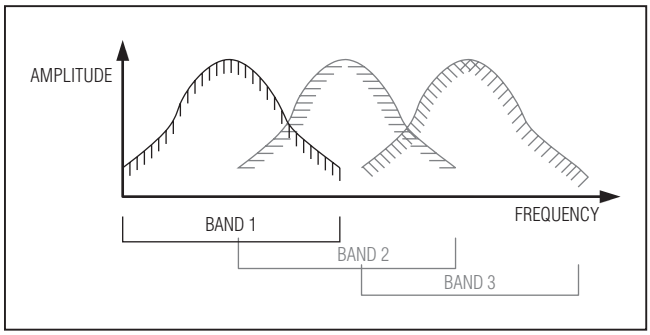


Figure 20. DRC Three Bands

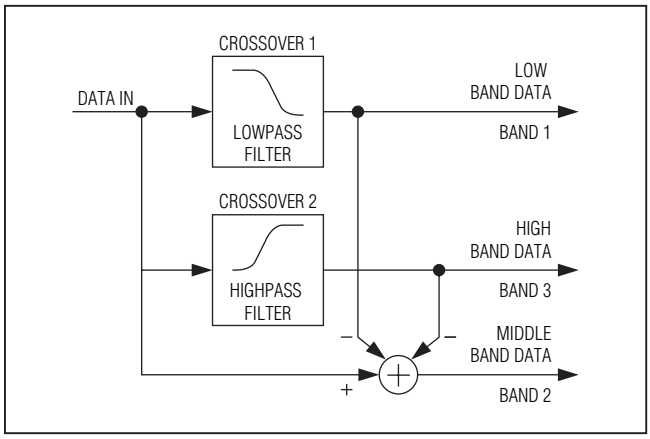


Figure 21. DRC 3-Band Crossover Filter

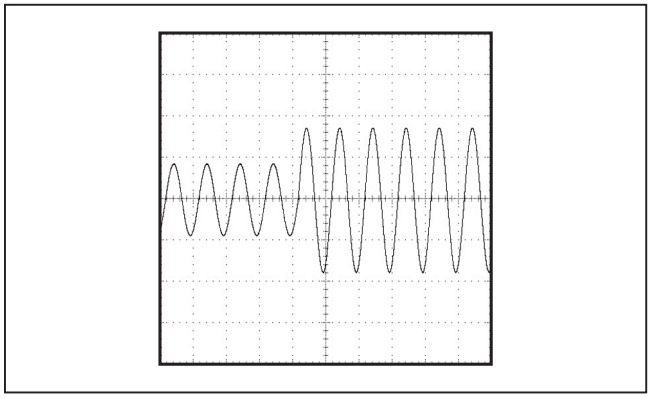


Figure 22. Low-Signal to High-Signal Transition, No Clipping, Compressor Disabled

Figure 22 through Figure 24 demonstrates the benefits of using the compressor. Each of these figures uses the same input signal.

To operate the compressor, select a threshold level, compression ratio, attack time-constant, and release time through control registers. When enabled, RMS signal levels that cross above the selected DRC threshold level are attenuated based on the selected compression ratio (Figure 19). The user-selected gain setting is automatically restored when the RMS signal level falls below the compressor threshold. The attack time-constant determines the time-constant used when the compressor engages. The release time determines the time-per-step used when the compressor disengages.

The expander reduces the noise floor when there is no desired input signal by attenuating peak signals that are below the selected expander threshold (Figure 19).

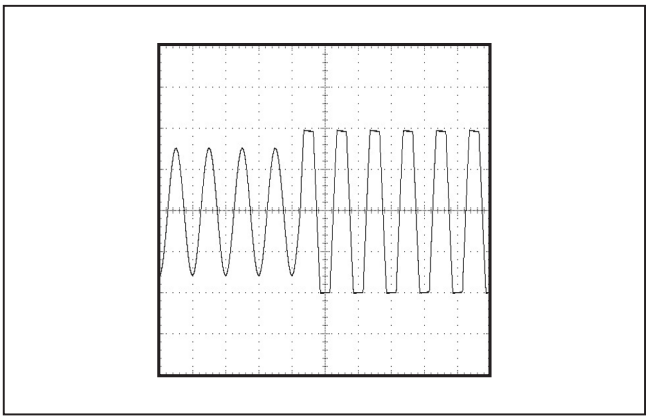


Figure 23. Low-Signal to High-Signal Transition, Increased Gain, Compressor Disabled

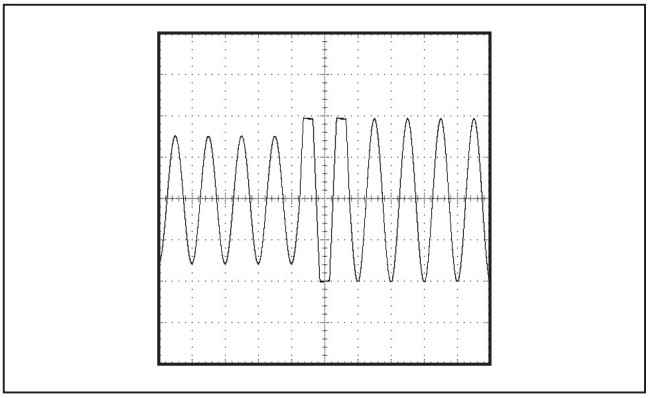


Figure 24. Low-Signal to High-Signal Transition, Increased Gain, DRC Enabled

Expansion ratio and attack time settings are configured by control registers. The expansion ratio determines the input: output relationship used when the input signal is below the selected threshold. The expansion attack time determines the time-per-step used when the expander engages. Figure 25 and Figure 26 show the benefits of the expander by comparing the output with the expander disabled against the output with the expander enabled.

DAI1 and DAI2 playback paths can be independently configured. See Figure 19 for the range of possible input to output responses possible with the DRC. In addition, both attack time and release time are programmable.

Parametric Equalizer

The parametric EQ contains five independent biquad filters with programmable gain, center frequency, and bandwidth for playback path 1 (stereo) and 2 (mono). Each biquad filter has a gain range of ±12dB, a center frequency range from 20Hz to 20kHz. Use a filter Q less than that shown in Figure 27 to achieve ideal frequency responses. Setting a higher Q results in nonideal frequency response. The biquad filters are series connected allowing a total gain of ±60dB. The path needs to be disabled by setting SDIEN_ low when changing the filter values.

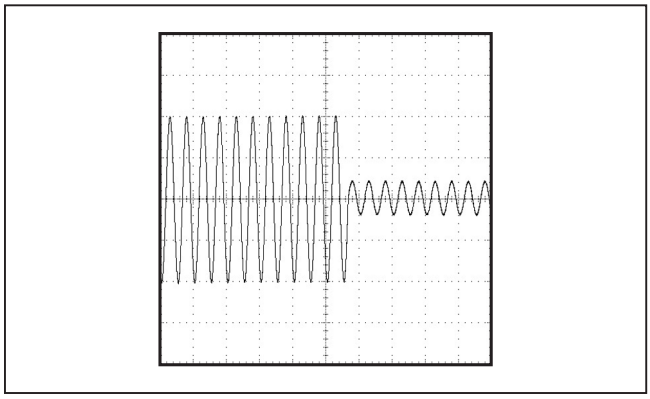


Figure 25. High-Signal to Low-Signal Transition, Expander Disabled

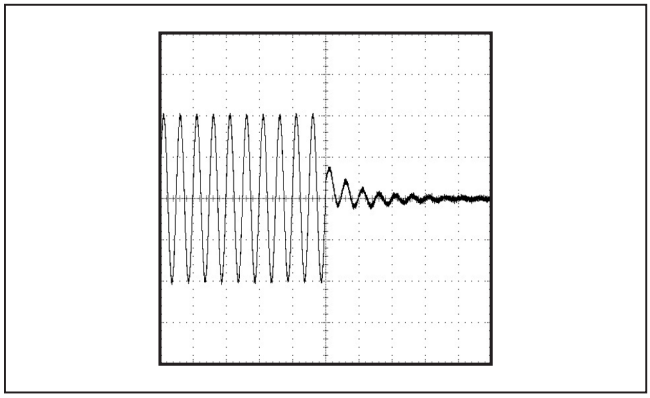


Figure 26. High-Signal to Low-Signal Transition, Expander Enabled

Table 16. Dynamic Range Control Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
DRC DAI1		
0x6C	DAI1 DRC 1 Timing	0
0x6D	DAI1 DRC 1 Compressor	0
0x6E	DAI1 DRC 1 Expander	0
0x6F	DAI1 DRC 1 Gain	0
0x70	DAI1 DRC 2 Timing	0
0x71	DAI1 DRC 2 Compressor	0
0x72	DAI1 DRC 2 Expander	0
0x73	DAI1 DRC 2 Gain	0
0x74	DAI1 DRC 3 Timing	0
0x75	DAI1 DRC 3 Compressor	0
0x76	DAI1 DRC 3 Expander	0
0x77	DAI1 DRC 3 Gain	0
DRC DAI2		
0x78	DAI2 DRC 1 Timing	0
0x79	DAI2 DRC 1 Compressor	0
0x7A	DAI2 DRC 1 Expander	0
0x7B	DAI2 DRC 1 Gain	0
0x7C	DAI2 DRC 2 Timing	0
0x7D	DAI2 DRC 2 Compressor	0
0x7E	DAI2 DRC 2 Expander	0
0x7F	DAI2 DRC 2 Gain	0
0x80	DAI2 DRC 3 Timing	0
0x81	DAI2 DRC 3 Compressor	0
0x82	DAI2 DRC 3 Expander	0
0x83	DAI2 DRC 3 Gain	0
FILTER COEFFICIENTS		
0x9C–0xA5	DAI1 Crossover Filter 1	1
0xA6–0xAF	DAI1 Crossover Filter 2	1
0xB0–0xB9	DAI2 Crossover Filter 1	1
0xBA–0xC3	DAI2 Crossover Filter 2	1

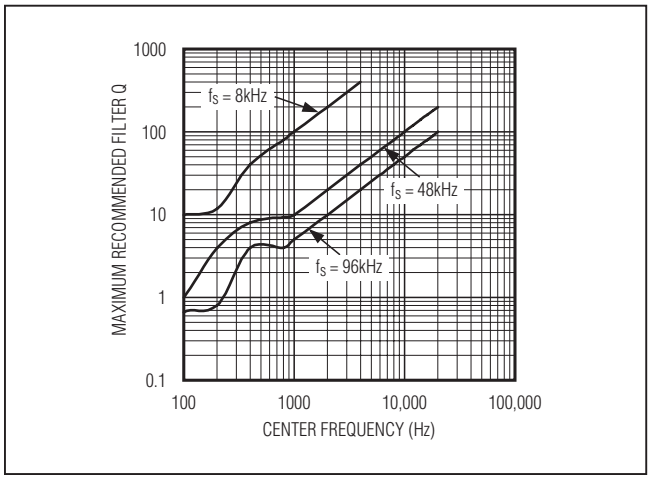


Figure 27. Maximum Recommended Filter Q vs. Frequency

Use the attenuator at the EQ's input to avoid clipping the signal. The attenuator can be programmed for fixed attenuation or dynamic attenuation based on signal level. If the dynamic EQ clip detection is enabled, the signal level from the EQ is fed back to the attenuator circuit to determine the amount of gain reduction necessary to avoid clipping.

The MAX98096 Evaluation Kit software includes a graphic interface for generating the EQ coefficients.

Biquad Filters

Two programmable biquad filters provide highly configurable filtering for both playback path 1 and 2. These filters allow for highly customizable frequency response in addition to the 5-band EQ. The two programmable biquad filters can be configured as any one or two combinations of the following filters:

- Lowpass
- Highpass
- Band pass 1
- Band pass 2
- Notch
- EQ
- Low shelf
- High shelf
- Gain

Use the evaluation kit software to calculate the proper coefficients for the desired filter response. The gain, frequency, and Q factor are programmable through the evaluation kit software. The path needs to be disabled by setting SDIEN_ low when changing the filter values.

Table 17. Parametric Equalizer Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
LEVEL CONTROL		
0x59	DAI1 EQ Level	0
0x5B	DAI2 EQ Level	0
CONFIGURATION		
0x88	Level Control	0
FILTER COEFFICIENTS		
0x10–0x19	DAI1 EQ Band 1	1
0x1A–0x23	DAI1 EQ Band 2	1
0x24–0x2D	DAI1 EQ Band 3	1
0x2E–0x37	DAI1 EQ Band 4	1
0x38–0x41	DAI1 EQ Band 5	1
0x42–0x4B	DAI2 EQ Band 1	1
0x4C–0x55	DAI2 EQ Band 2	1
0x56–0x5F	DAI2 EQ Band 3	1
0x60–0x69	DAI2 EQ Band 4	1
0x6A–0x73	DAI2 EQ Band 5	1

Table 18. Biquad Filter Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
CONFIGURATION		
0x88	Level Control	0
FILTER COEFFICIENTS		
0x74–0x7D	Biquad Filter 1 (DAI1)	1
0x7D–0x87	Biquad Filter 1 (DAI2)	1
0x88–0x91	Biquad Filter 2 (DAI1)	1
0x92–0x9B	Biquad Filter 2 (DAI2)	1

Table 19. Headphone and Speaker Expander Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
SPEAKER SIGNAL PROCESSING		
0x6B	Speaker Noise Gate	0
HEADPHONE SIGNAL PROCESSING		
0x84	Headphone Noise Gate	0

Headphone and Speaker Expander

To minimize audible noise at the output when there is no audio signal, noise quieting circuits monitor the digital signal level just before each DAC. If the signal level is below the programmed threshold either the speaker or headphone analog volume level can be reduced to attenuate any noise being output. Doing so helps to reduce noise from noisy sources. Noise quieting is not supported on analog inputs unless the audio signal is first routed through the ADC path.

FlexSound System

The IC integrates a FlexSound processor in combination with a FlexSound software stack to provide a complete digital signal processing solution. The FlexSound processor provides advanced programmable signal processing for both the playback and record signal path. It consists of a processor core based on the Tensilica HiFi2, memory for the processor, hardware to get audio data in and out of the processor and support communication with a host, GPIOs, hardware decryption for downloaded code, and a software stack that ties everything together and facilitates performing signal processing.

FlexSound Processor Usage Models

There are three primary usage models for the FlexSound processor listed in order of increasing complexity:

- Use Maxim provided preconfigured use cases.
- Configure existing signal processing modules to create custom use cases.
- Write DSP plug-ins for the FlexSound processor that can be combined with existing signal processing modules to create custom use cases.

Preconfigured use cases provide the most straight forward path to using the FlexSound processor. These use cases are available to users in both the evaluation kit software and the ALSA driver. The use cases generally require only tuning prior to production release. Supported preconfigured use cases include:

- Noise reduction and echo cancelation (NREC) for portable devices
- Speaker protection and distortion limiting

The use cases are accessable in both the evaluation kit software and the ALSA driver provided by Maxim for Linux-based system. Refer to the [EVKIT Software user's guide] and [ALSA driver application notes] for details.

Link together exiting FlexSound plug-ins to create customized use cases. The included signal processing plug-ins are:

- One and two microphone noise suppression
- Echo cancellation
- Wind noise suppression
- Ambient aware outputs (receive voice clarity)
- Distortion limiter
- Power and excursion limiters
- Equalizers
- Dynamic range control

These signal processing plug-ins are made available through the evaluation kit software and can imported into the ALSA driver. For more information see the [EVKIT Software user's guide] and [ALSA driver application notes].

To create custom plug-ins for the FlexSound knowledge of the FlexSound audio engine (a proprietary real-time operating system) and the architecture of the underlying FlexSound processor is required. Refer to the [FlexSound Plug-in Developer's Guide] for details. Plug-in development includes developing algorithms that run on the FlexSound processor and real-time control modules for use in the evaluation kit software. The development process takes advantage of a mature set of development tools provided by Tensilica for the HiFi2.

FlexSound Processor

The FlexSound processor is a custom configured Tensilica HiFi2. Detailed information on the HiFi2 is available from Tensilica (www.tensilica.com).

The HiFI2 consists of a base general purpose 32-bit RISC processor combined with additional instructions and hardware to efficiently handle 16/24 fixed point data with particular attention to audio signal processing needs. Programming is done in C/C++, including inner loops of DSP algorithms where C/C++ intrinsics play a key role. Tensilica provides a mature set of tools for programming the HiFi2 including an IDE based on Eclipse.

The FlexSound processor configuration of the HiFi2 has the following salient features:

- Core architecture
  - ✧ Dual 24 x 24-bit MAC unit
  - ✧ Zero-overhead looping
  - ✧ Efficient handling of 16/24-bit integer and s1.15/s1.23 fixed point data
  - ✧ 5-stage pipeline with 64/24/16-bit ISA
  - ✧ 2-issue VLIW
  - ✧ Integrated timer with 2 timers
  - ✧ Integrated interrupt controller with 17 interrupts on 4 levels
- Processor speed
  - ✧ 40MHz at 1.4V
  - ✧ Up to 100MHz at 1.8V
- Memory (all single cycle access)
  - ✧ 24KB local instruction RAM
  - ✧ 40KB local data RAM
  - ✧ 56KB local instruction ROM (contains FlexSound RTOS and DSP library functions)
  - ✧ 8KB local data ROM (contains RTOS and FFT twiddle tables)
- Interfaces
  - ✧ GPIO (4 direct pins)
  - ✧ On-chip-debug with JTAG interface
  - ✧ Input FIFOs
    - ▪ 6 input FIFOs for audio data (20-bit wide)
    - ▪ 1 input FIFO for communication from a host processor (8-bit wide)
    - ▪ 1 input FIFO (32 bit) for speaker ADC data
  - ✧ Output FIFOs
    - ▪ 6 output FIFOs for audio data (20-bit wide)
    - ▪ 1 output FIFO for communication to a host processor (8-bit wide)
  - ✧ Ports
    - ▪ 1 output port for controlling audio interfaces
    - ▪ 1 output port (9 bit) for register map writes
    - ▪ 1 input port (9 bit) register map reads
    - ▪ 1 input port for battery data

Table 20. FlexSound Processor Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
FlexSound PROCESSOR I/O		
0x00	FlexSound Processor Host Data I/O	0/1
STATUS		
0x01	Host Interrupt Status	0/1
0x02	Host Read Status	0/1
0x03	Host Write Status	0/1
SEGMENT POINTER		
0x0F	Segment Pointer	0
INTERRUPT CONTROL		
0x10	Host Interrupt Config	0/1
0x11	Host Interrupt Enable	0/1
HOST CONTROL		
0x15	Decrypt	0
0x18	Keycode1	0
0x19	Keycode2	0
0x1A	Keycode3	0
0x1B	Keycode4	0
0x1C	OEMCcode1	0
0x1D	OEMCcode2	0
FlexSound PROCESSOR CONTROL		
0x1E	FlexSound Processor Data FIFO Configuration 1	0
0x1F	FlexSound Processor Data FIFO Configuration 2	0
0x20	FlexSound Processor Data FIFO Configuration 3	0
0x21	FlexSound Processor Data FIFO Configuration 4	0
0x22	FlexSound Processor Data FIFO Configuration 5	0
0x23	FlexSound Processor Data FIFO Configuration 6	0
0x24	GPIO	0
FlexSound PROCESSOR CLOCK CONTROL		
0x25	FlexSound Processor Clock Configuration	0

Control Interface

The FlexSound processor is controlled through register 0x00 in the IC's register map. This register serves as a data tunnel between the host and the DSP, allowing arbitrary data lengths to be exchanged. The data tunnel can be accessed through the I²C or SPI or JTAG interface.

Register Access

The FlexSound DSP can access registers 0x10 to 0x97 on segment page 0 of the IC if the system allows it. This allows the DSP to self-configure the hardware and provide dynamic adjustments of settings.

Analog Feedback

To enable speaker protection and distortion limiting and optimize echo cancellation, the IC provides feedback to the DSP of the receiver and speaker output signals and battery voltage. This information allows DSP algorithms to react to the exact output audio signal without requiring prediction. The speaker amplifiers must be disabled when monitoring the receiver output with the DSP. This information allows DSP algorithms to react to the exact output audio signal without requiring prediction.

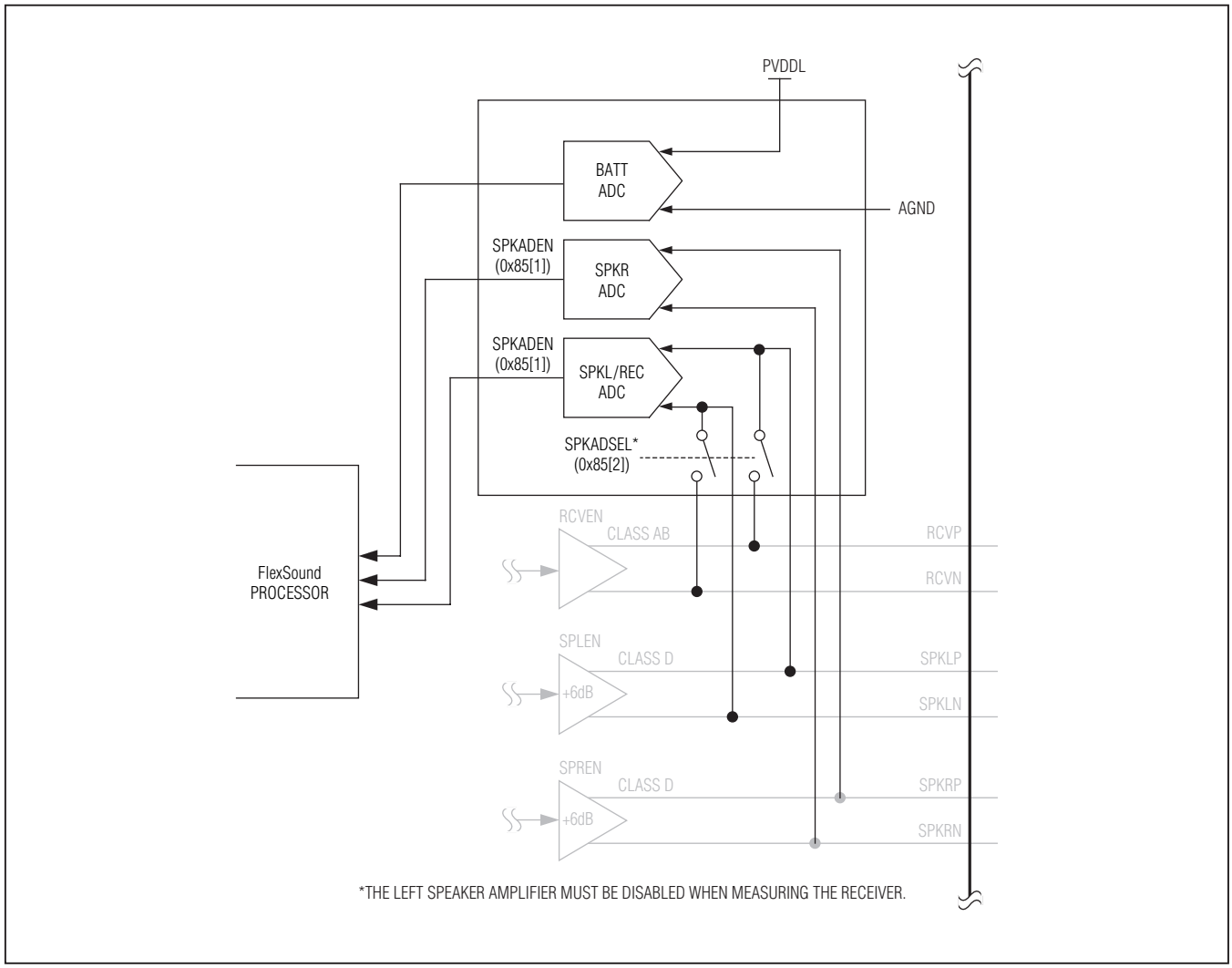


Figure 28. FlexSound Analog Feedback Block Diagram

Code Protection

The FlexSound processor supports data decryption during the loading process. Algorithms can be stored on the system host in an encrypted format and decrypted on the fly while being loaded into the DSP memory.

FlexSound Processor Clock

The FlexSound processor operates over a range of clock frequencies depending on processor loading, 40MHz (min) for 1.4V operation and 100MHz (min) for 1.8V operation. To minimize power consumption the processor always operates at the lowest clock speed possible. To generate the range of clock frequencies required, a multiplying delay-locked loop (MDLL) is integrated to convert MCLK to the frequency required by the FlexSound processor.

Receiver Amplifier

The IC includes a single differential receiver amplifier that is designed to drive 16Ω to 32Ω earpiece speakers (Figure 30). The receiver amplifier output can be fed back to the FlexSound processor to give real-time monitoring for different algorithms. The speaker amplifier outputs need to be disabled when the receiver output is fed back to the FlexSound processor.

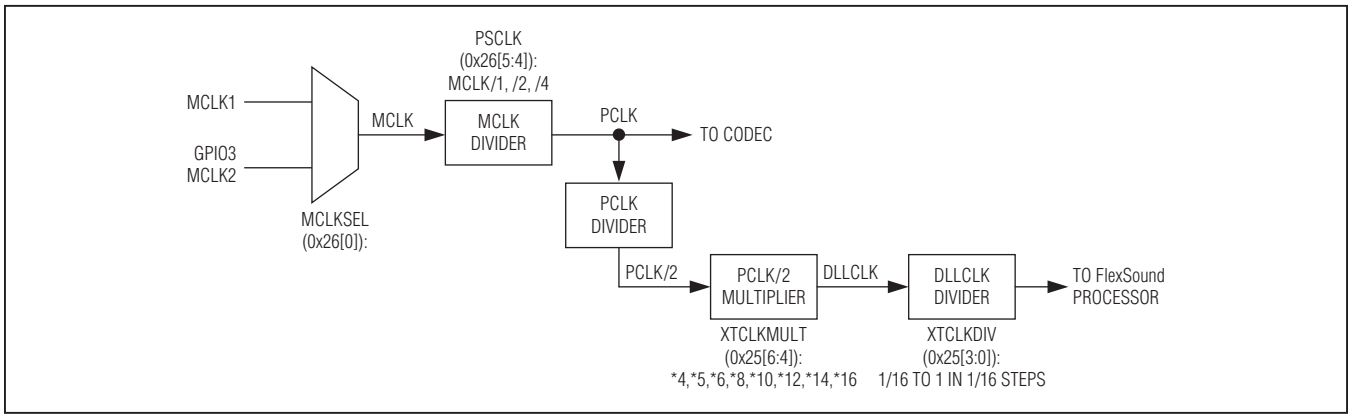


Figure 29. FlexSound Processor Clock Detail Block Diagram

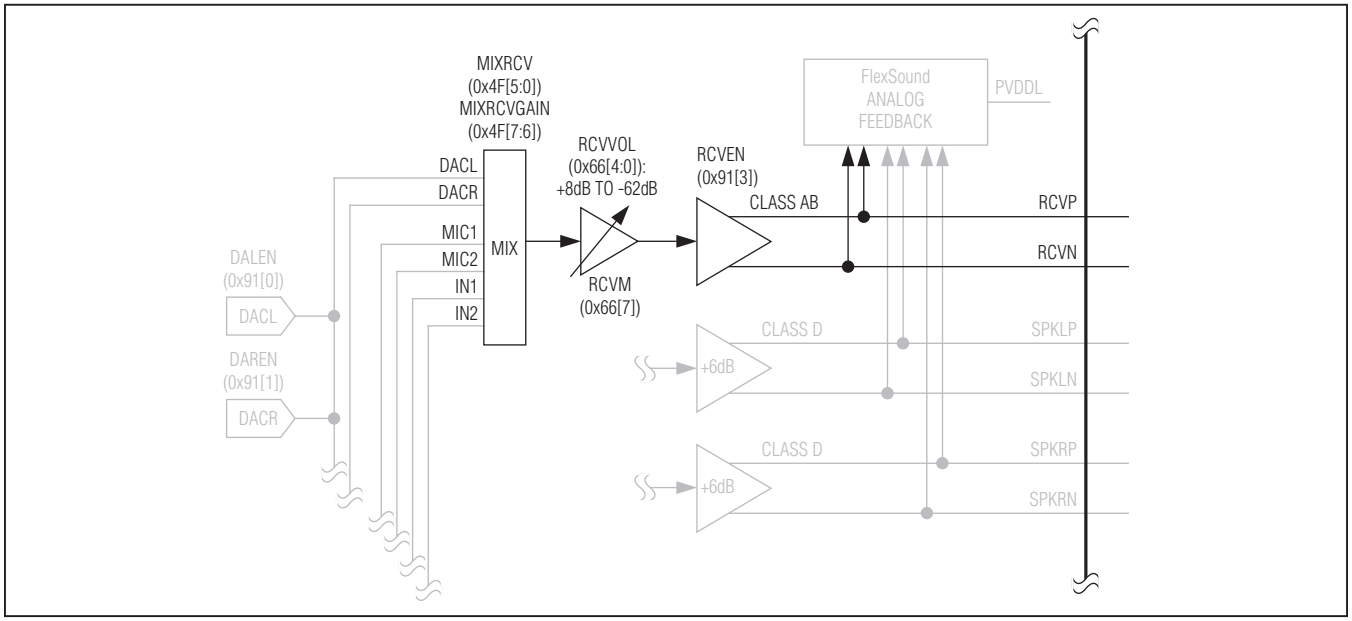


Figure 30. Receiver Amplifier Block Diagram

Table 21. Receiver Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
MIXERS		
0x4F	Receiver	0
LEVEL CONTROL		
0x66	Receiver Volume Control	0
POWER MANAGEMENT		
0x91	Output Enable	0

Table 22. Receiver Mixer Attenuation Levels

MIXRCVGAIN	DAC_ GAIN (dB)	IN_ GAIN (dB)	MIC_ GAIN (dB)
00	0	+9	+9
01	-6	+3	+3
10	-9	0	0
11	-12	-3	-3

Receiver Output Mixer

The IC receiver amplifier accepts inputs from the stereo DAC, the line inputs, and the MIC inputs. Configure the mixer to mix any combination of the available sources. The mixer features different attenuation levels for when more than one inputs to the mixer are selected (Table 22).

Speaker Amplifiers

The IC integrates a stereo filterless Class D amplifier that offers much higher efficiency than Class AB without the typical disadvantages. The speaker output utilizes active emissions limiting and spread-spectrum modulation to minimize the EMI radiated by the amplifier. The

Table 23. Speaker Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
MIXERS		
0x50	Left Speaker	0
0x51	Right Speaker	0
LEVEL CONTROL		
0x67	Left Speaker Volume Control	0
0x68	Right Speaker Volume Control	0
POWER MANAGEMENT		
0x91	Output Enable	0
0x92	Output Enable	0

right channel features a slave mode where the switching scheme is in sync with the left channel to eliminate the beat tone that occurs with asynchronous stereo Class D switching.

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78%, however, that efficiency is only exhibited at peak output power. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the IC's Class D amplifier still exhibits 85% efficiency under the same conditions.

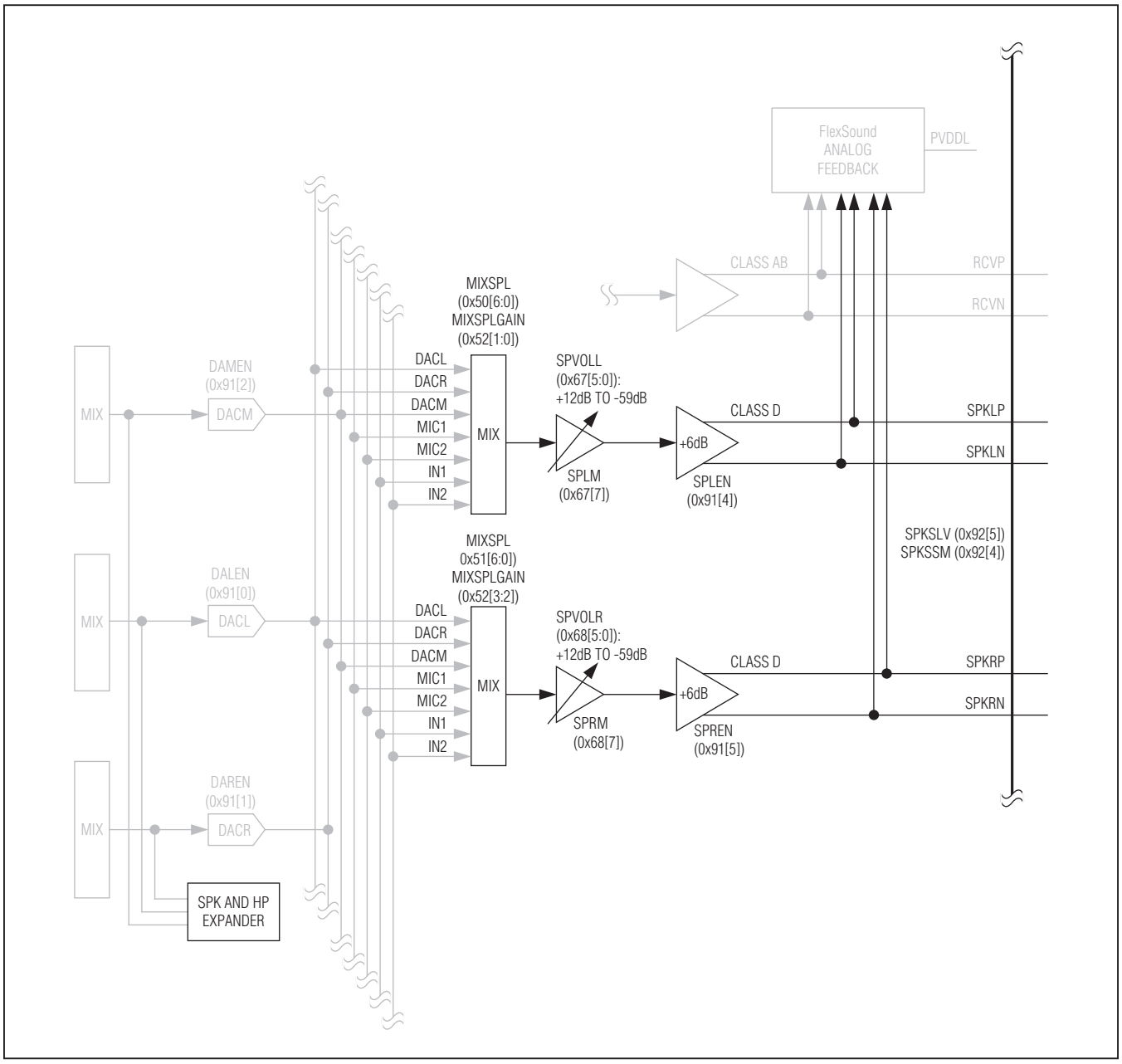


Figure 31. Speaker Amplifier Block Diagram

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters or shielding in order to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions, while maintaining up to 92% efficiency. Maxim's patented spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The IC's spread-spectrum modulator randomly varies the switching frequency by ±10kHz around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 32).

Speaker Output Mixers

The IC's speaker amplifiers accept inputs from the stereo DAC, mono DAC, the line inputs (single-ended or differential), and the MIC inputs. Configure the mixer to mix any combination of the available sources. The mixer features different attenuation levels for when more than one inputs to the mixer are selected (Table 24).

Table 24. Speaker Mixer Attenuation Levels

MIXSPLGAIN MIXSPRGAIN	DAC_ GAIN (dB)	IN_ GAIN (dB)	MIC_ GAIN (dB)
00	0	+9	+9
01	-6	+3	+3
10	-9	0	0
11	-12	-3	-3

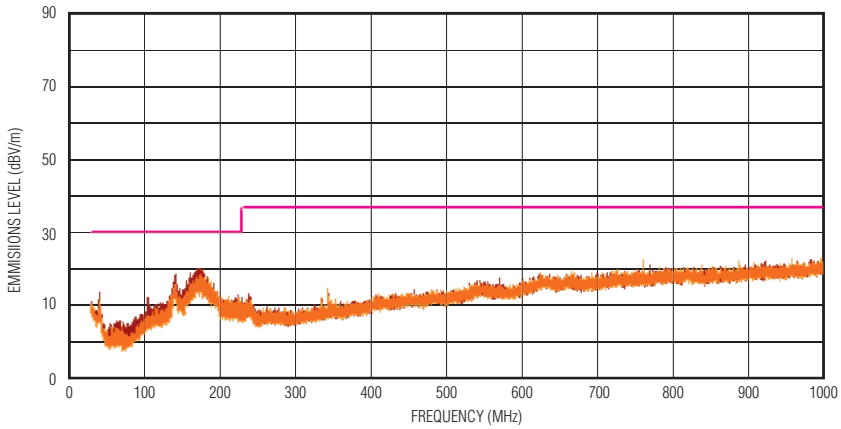


Figure 32. EMI with 30.2cm of Speaker Cable

Headphone Amplifier

DirectDrive Headphone Amplifier

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply). Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's second-generation DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the ICs to be biased at GND while operating from a single supply (Figure 33). Without a DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF typ) capacitors, the IC's charge pump requires 3 small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier.

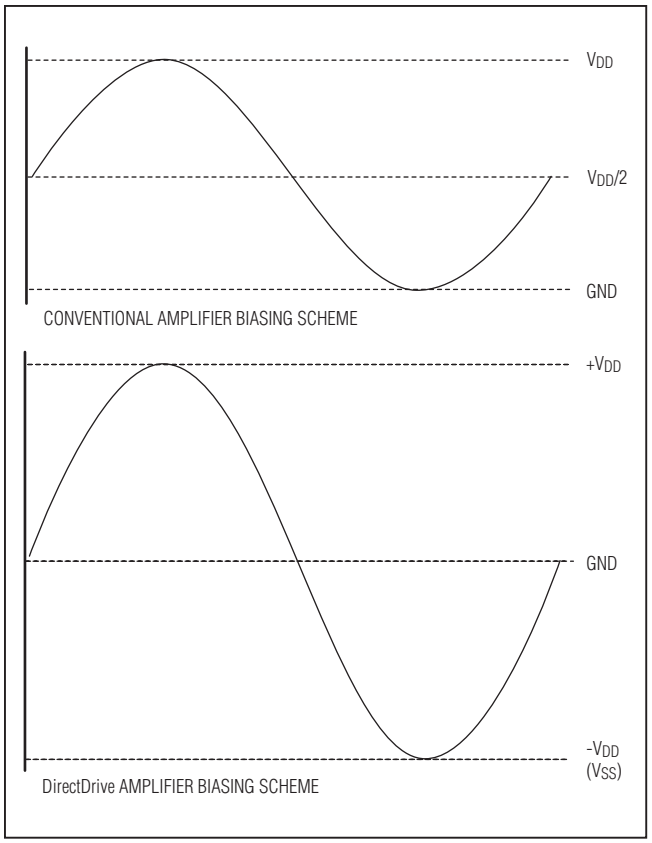


Figure 33. Traditional Amplifier Output vs. DirectDrive Output

Class H Operation

A Class H amplifier uses a Class AB output stage with power supplies that are modulated by the output signal. In the case of the IC, two nominal power-supply differentials of 1.8V (+0.9V to -0.9V) and 3.6V (+1.8V to -1.8V) are available from the charge pump. Figure 34 shows the operation of the output-voltage-dependent power supply.

Charge Pump

The dual-mode charge pump generates both the positive and negative power supplies for the headphone amplifier. To maximize efficiency, both the charge pump's switching frequency and output voltage change based on signal level.

When the output signal level is less than 10% of HPVDD, the switching frequency is reduced to a low rate. This minimizes switching losses in the charge pump. When the output signal exceeds 10% of HPVDD, the switching frequency increases to support the load current.

For output signals below 25% of HPVDD, the charge pump generates ±(HPVDD/2) to minimize the voltage drop across the amplifier's power stage and thus improve efficiency. Output signals that exceed 25% of HPVDD cause the charge pump to output ±HPVDD. The higher output voltage allows for full output swing from the headphone amplifier.

To prevent clipping when transitioning from the ±(HPVDD/2) output mode to the ±HPVDD output mode, the charge pump transitions very quickly. This quick change draws significant current from HPVDD for the duration of the transition. The bypass capacitor on HPVDD supplies the required current and prevents droop on HPVDD. See the *Supply Bypassing, Layout, and Grounding* section for more information.

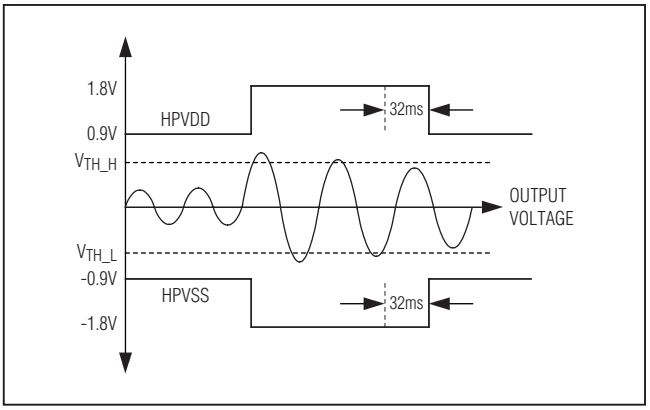


Figure 34. Class H Operation

Headphone Ground Sense (HPSNS)

HPSNS senses the ground return for the headphone load. For optimal performance, connect HPSNS to the ground pole of the jack through an isolated trace, as shown in Figure 30. If HPSNS is not used, connect to the analog ground plane.

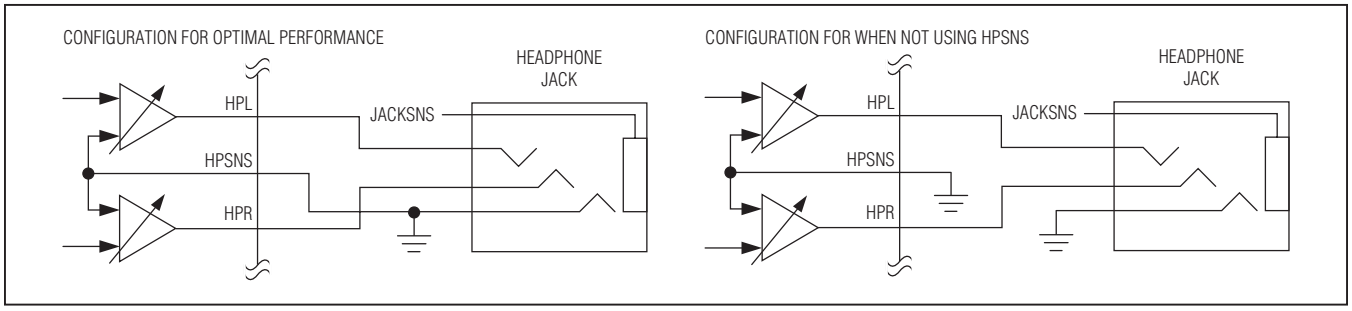


Figure 35. HPSNS Configuration

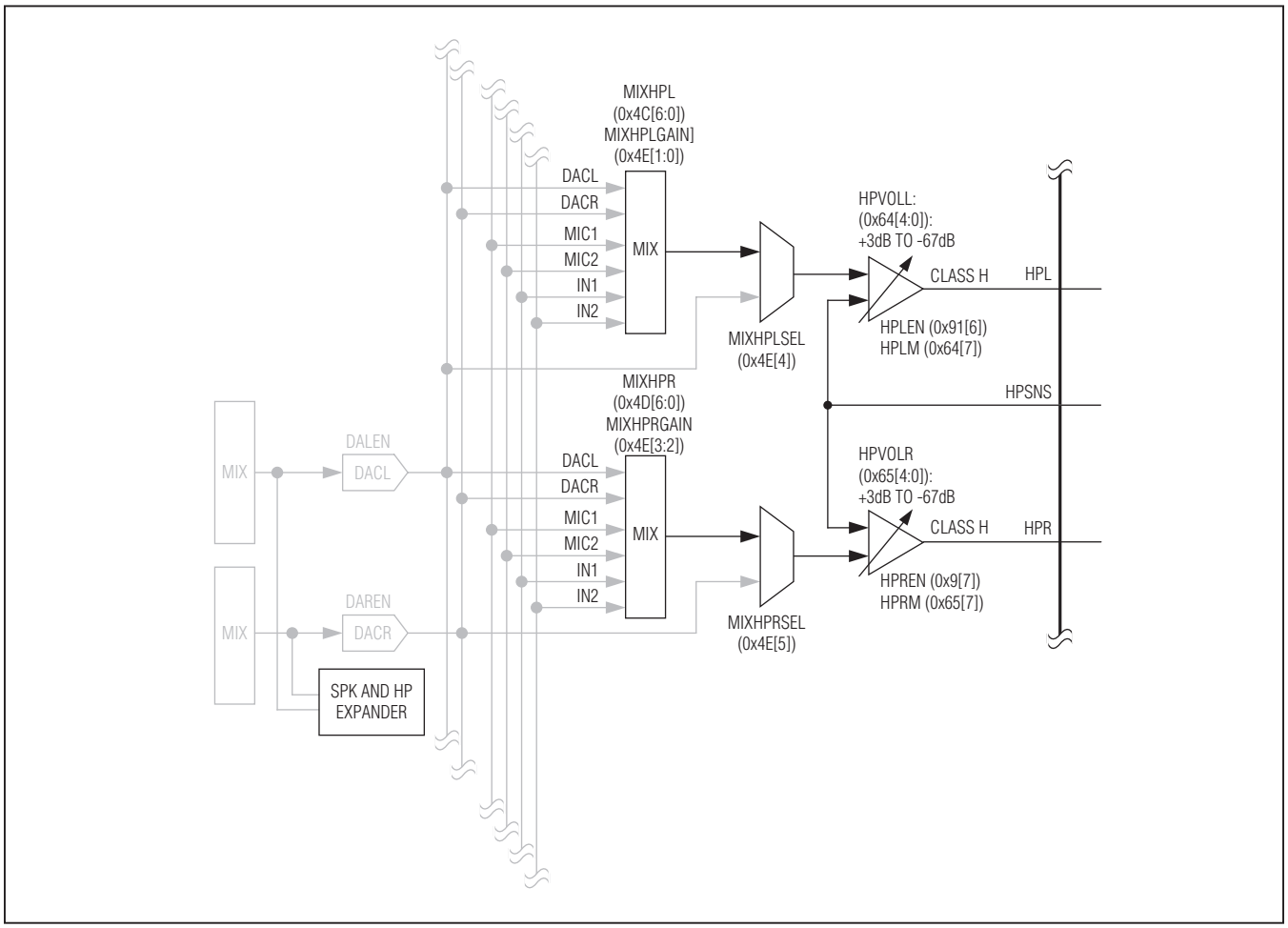


Figure 36. Headphone Amplifier Block Diagram

Table 25. Headphone Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
MIXERS		
0x4C	Left Headphone	0
0x4D	Right Headphone	0
0x4E	Headphone Mixer Gain	0
LEVEL CONTROL		
0x64	Left Headphone Volume Control	0
0x65	Right Headphone Volume Control	0
POWER MANAGEMENT		
0x91	Output Enable	0

Table 26. Headphone Mixer Attenuation Levels

MIXHPLGAIN MIXHPRGAIN	DAC_ GAIN (dB)	IN_ GAIN (dB)	MIC_ GAIN (dB)
00	0	+9	+9
01	-6	+3	+3
10	-9	0	0
11	-12	-3	-3

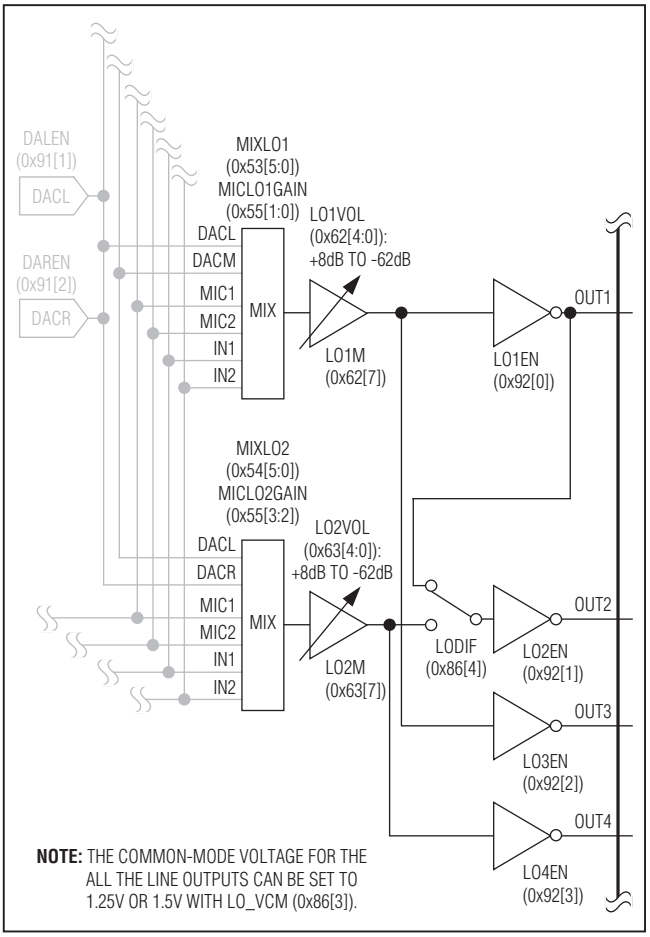


Figure 37. Line Output Block Diagram

Headphone Output Mixers

The headphone amplifier mixer accepts inputs from the stereo DAC, the line inputs (single-ended or differential), and the MIC inputs. Configure the mixer to mix any combination of the available sources. The mixer features different attenuation levels for when more than one inputs to the mixer are selected (Table 26). The stereo DAC can bypass the headphone mixers and be connected directly to the headphone amplifiers to provide lower power consumption and lower noise.

Line Output Amplifier

The IC includes two stereo single-ended line output amplifiers (Figure 37). OUT1 and OUT2 can be configured as a mono differential output, where the input signal is supplied from line output mixer 1. OUT1 and OUT3 share the same volume control and mixer. OUT2 and OUT4 share the same volume control and mixer. The common-mode voltage on the line output amplifiers can be lowered from 1.5V to 1.25V for lower supply levels (PVDDR), through the control register.

Line Output Mixer

The IC line output amplifier accepts inputs from the stereo DAC, the line inputs and the MIC inputs. Configure the mixer to mix any combination of the available sources. The mixer features different attenuation levels for when more than one input to the mixer is selected (Table 27).

Click-and-Pop Reduction

The IC includes extensive click-and-pop reduction circuitry. The circuitry minimizes clicks-and-pops at turn-on, turn-off, and during volume changes.

Zero-crossing detection is implemented on all analog PGAs and volume controls to prevent large glitches when volume changes are made. Instead of making a volume change immediately, the change is made when the audio signal crosses the midpoint. If no zero-crossing occurs within the timeout window of 100ms, then the change occurs at that time. Figure 38 and Figure 39 show the turn on response with zero-crossing detection enabled and disabled, respectively.

Table 27. Line Output Mixer Attenuation Levels

MIXLO1GAIN MIXLO2GAIN	DAC_ GAIN (dB)	IN_ GAIN (dB)	MIC_ GAIN (dB)
00	0	+9	+9
01	-6	+3	+3
10	-9	0	0
11	-12	-3	-3

Table 28. Line Output Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
LEVEL CONTROL		
0x62	Line Output Level 1	0
0x63	Line Output Level 2	0
CONFIGURATION		
0x86	Line Input/Output	0
POWER MANAGENEMT		
0x92	Output Enable	0

Volume slewing breaks up large volume changes into the smallest available step size and the steps through each step between the initial and final volume setting. When enabled, volume slewing also occurs at device turn-on and turn-off. During turn-on, the volume is set to mute before the output is enabled. Once the output is on, the volume ramps to the desired level. At turn-off, the volume is ramped to mute before the outputs are disabled. Figure 40 and Figure 41 show the turn on/off response with volume slewing enabled and disabled, respectively.

When there is no audio signal zero-crossing detection can prevent volume slewing from occurring. Enable enhanced volume slewing to prevent the volume controller from requesting another volume level until the previous one has been set. Each step in the volume ramp then occurs after a zero-crossing has occurred in the audio signal or the timeout window has expired. During turn-off enhanced volume slewing is always disabled.

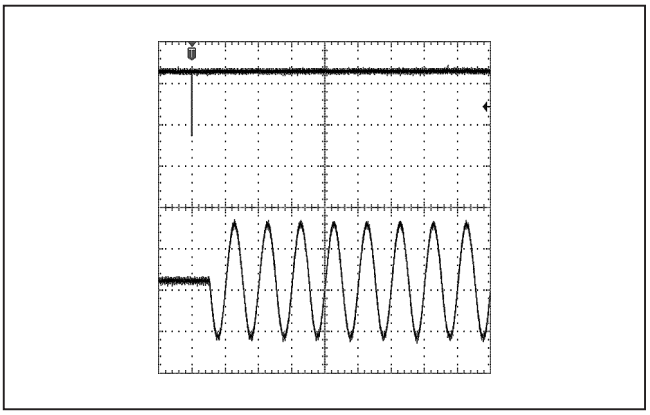


Figure 38. Zero-Crossing Detection Enabled

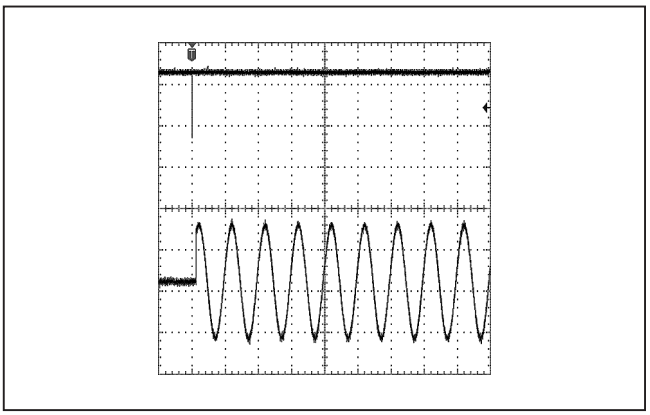


Figure 39. Zero-Crossing Detection Disabled

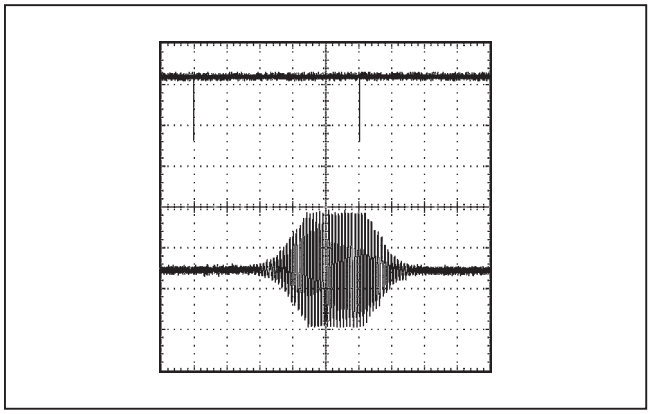


Figure 40. Volume Slewing Enabled

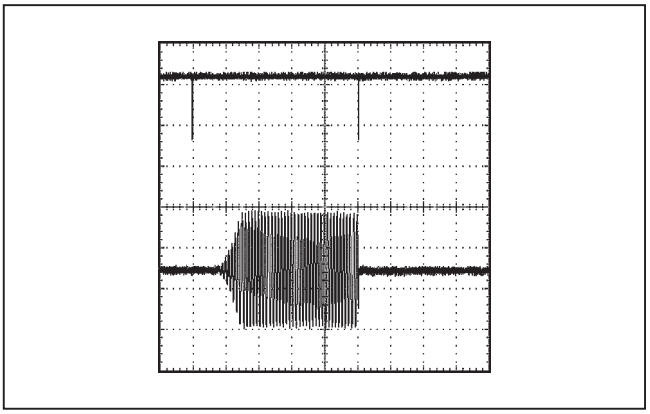


Figure 41. Volume Slewing Disabled

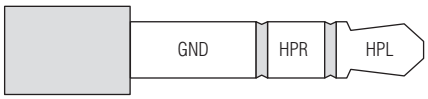
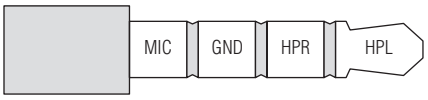
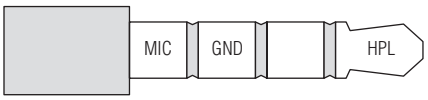
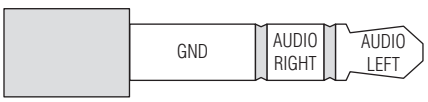
Table 29. Click-and-Pop Reduction Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
CONFIGURATION		
0x88	Level Control	0

Accessory Detection

The IC features a detection scheme that senses when a 3.5mm plug is inserted into the system jack. After sensing insertion, a configuration detection algorithm takes over and reads the makeup of the installed plug. Information regarding the makeup of the plug is reported back through the status registers. Table 30 shows the types of accessories that can be detected individually.

Table 30. Accessories Identified by the IC

ACCESSORIES	ELECTRICAL CONFIGURATION	RESULTS (Register 0x07)
Stereo headphones		HP_IN (0xC0)
Stereo headset		HP_IN, MIC_IN (0xC8)
Mono headset		HP_IN, MIC_IN (0xC8)
Line output cable		LO_IN (0xA0)

Jack Insertion Testing

Jack insertion detection uses an inaudible AC signal to HPL to sense when a load is plugged in. The headphone amplifiers must be disabled when polling for insertion to prevent false detection. The AC test signal is constantly poling until a load is detected. Enable the JACKSW by setting PIN5EN in register 0x89 to reduce the frequency of the polling for lower power consumption. The IC is programmable to work with both types of mechanical switches (Table 31). Disable JACKSW to speed up polling in systems where no jack switch is available. Faster polling decreases response time at the expense of power consumption.

Detecting Jack Removal

Jack removal detection monitors JACKSNS after an insertion has been detected and the accessory type been reported. A removal is detected when JACKSNS flys up to $V_{MICBIAS2}$. When a removal is detected, immediately disable the headphone amplifiers so that subsequent jack insertions can be detected.

Power Modes

The power modes of the IC are controlled by the JDEN bits. The three power modes include disabled mode, normal operating mode, and button detection mode.

- **Disabled:** All jack detection circuitry is disabled.
- **Normal detection/operating:** The jack detection circuitry waits for an insertion or removal event to occur either polling for insertion or waiting for removal.
- **Button detection:** The IC can be operated in a low power configuration waiting for a button press on the accessory. Disable MICBIAS_ and enable the internal pullup resistor on JACKSNS (V_{DDUP}) and enabling only the keypress detection circuit to detect a button press with the minimum power consumption.

Key-Switch Encoder

The IC key-switch encoder supports two types of passive keypads:

- A single button hookswitch or MIC switch that grounds out JACKSNS when pressed.
- A passive multibutton headset with a resistor/switch array between JACKSNS and ground.

Table 31. Programming Polarity of Jack Switch (Register 0x45)

JKSWTYP	JACK SWITCH TYPE
0	Open when a jack is inserted
1	Closed when a jack is inserted

Table 32. Jack Detection Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
STATUS (Read Only)		
0x07	Auto Jack Detection	0/1
0x08	Jack Detection	0/1
INTERRUPT CONTROL		
0x13	Jack Detect Interrupt Enabled 1	0
0x14	Jack Detect Interrupt Enabled 2	0
ADC CLOCK CONTROL		
0x45	ADC Clock Mode	0
JACK DETECTION		
0x89	Automatic Jack Detection	0
0x8A	Manual jack Detection	0
0x8E	DC Test Slew Rate	0
0x8F	Test Configuration	0

Key-Switch Encoder Timing

Two registers control the key-switch delay times t_{DEB} and t_{DELAY}. The debounce time is the time from when the switch stops bouncing and when the ADC converts. The delay time is set long to ensure that an unplug event is not encoded as a keypress. See Figure 48.

An interrupt flags provided the appropriate mask bit is set, after the delay time elapses.

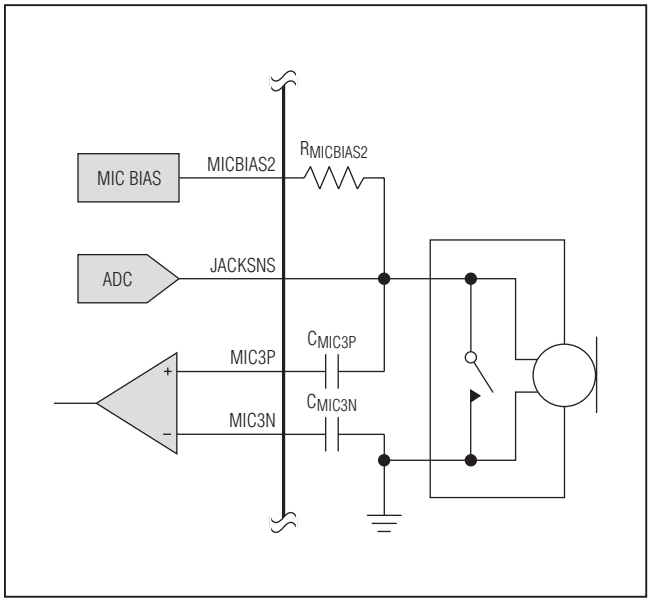


Figure 42. Passive Single Button Hookswitch

Single Button, Hook-Switch/MIC Switch

Figure 42 shows a single button hookswitch.

Figure 43 and Figure 44 show the timing involved when pressing a hookswitch for single button keypress < t_{DELAY} or > t_{DELAY}.

Passive Multibutton Headset (MBH)

A passive MBH consists of a microphone with numerous switches that connect different value resistors to ground. The switched resistor and the mic bias resistor set up a voltage divider that creates a unique voltage. The on-chip ADC then encodes the voltage and reports to the system.

Figure 45 shows the circuit diagram of a passive MBH.

Figure 46 and Figure 47 show the timing for < t_{DELAY} or > t_{DELAY} keypress on a passive MBH. The buttons create voltage divider off of MICBIAS by the combination of the MICBIAS resistor and the switch's load resistor. The ADC reads the resulting voltage to determine which button was pressed. The switch that shorts the MICBIAS to ground is handled like the hookswitch in the previous section.

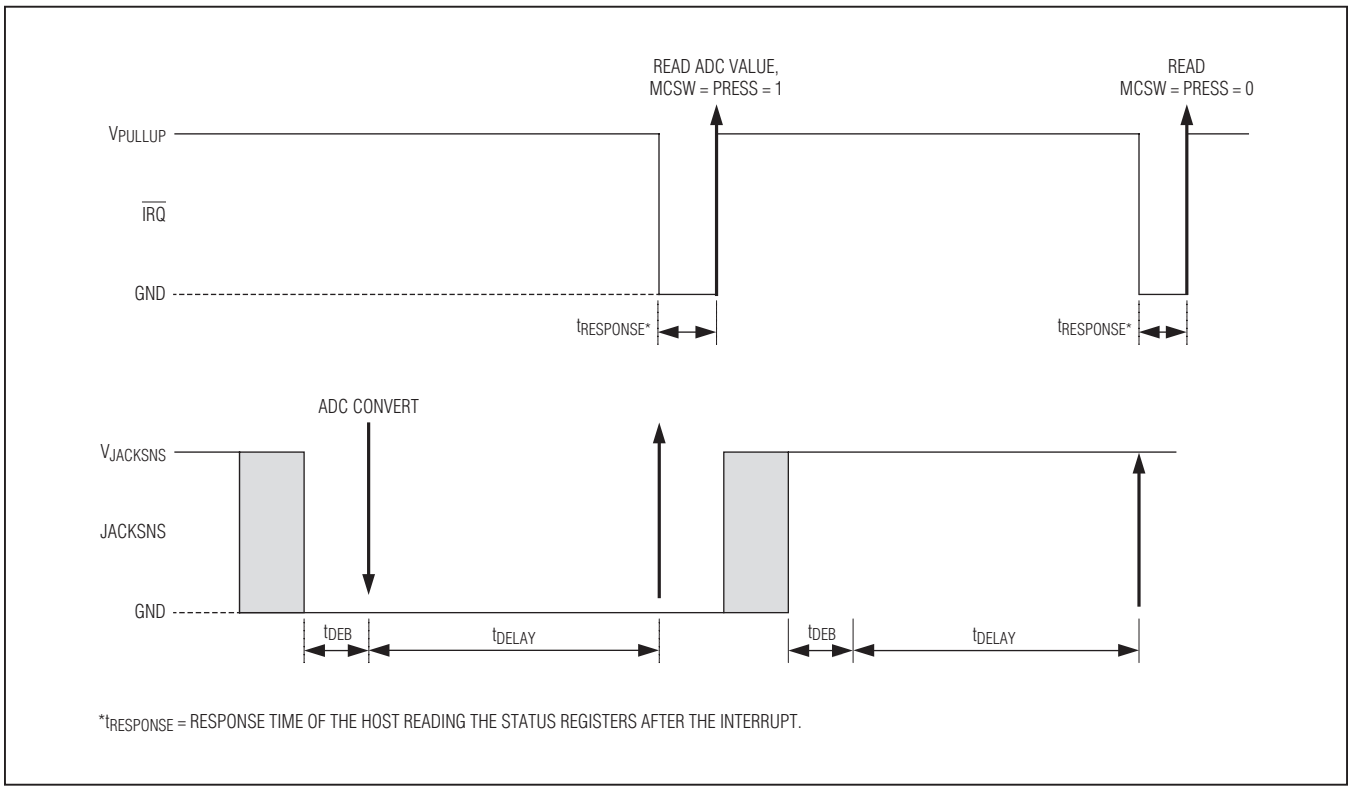


Figure 43. Single Hook Switch/Mic Switch Timing t_{DELAY}

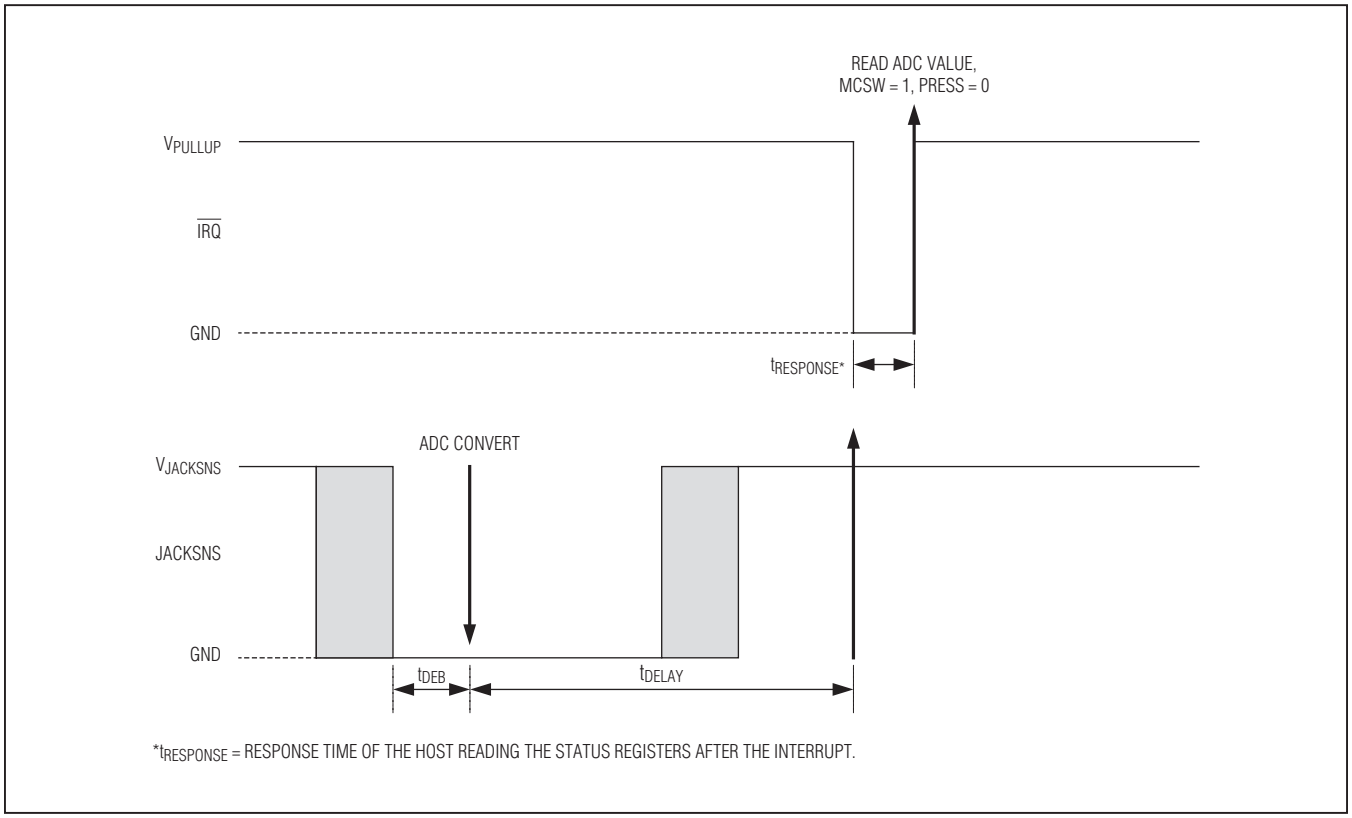


Figure 44. Single Hook Switch/Mic Switch Timing t_{DELAY}

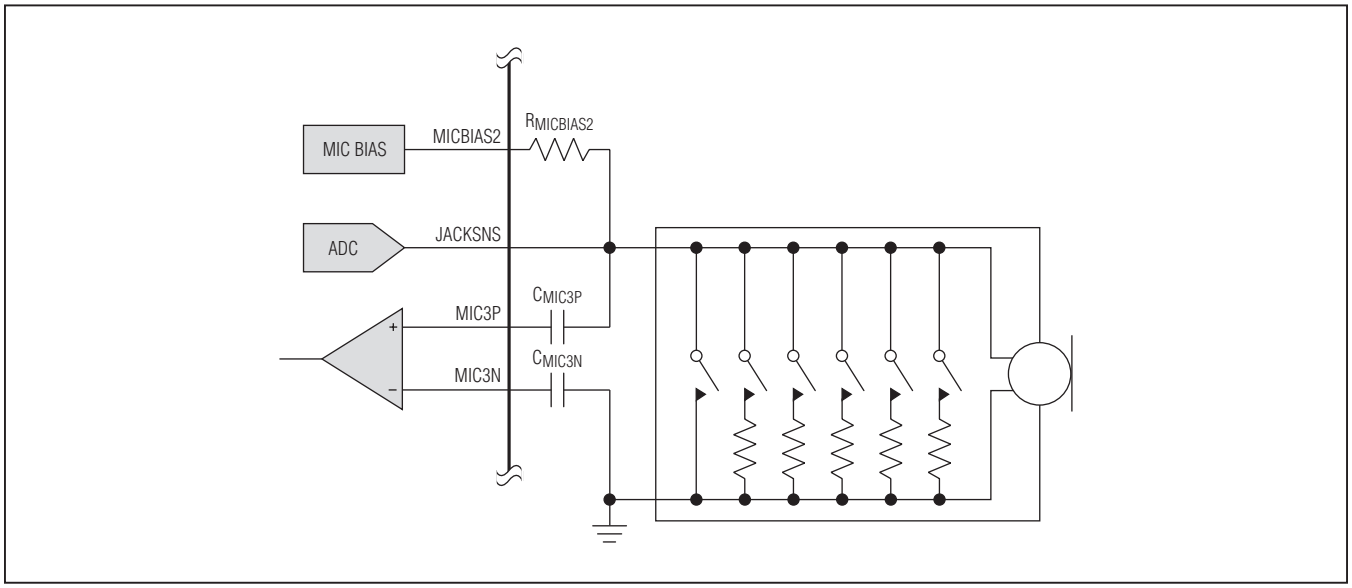


Figure 45. Passive MBH

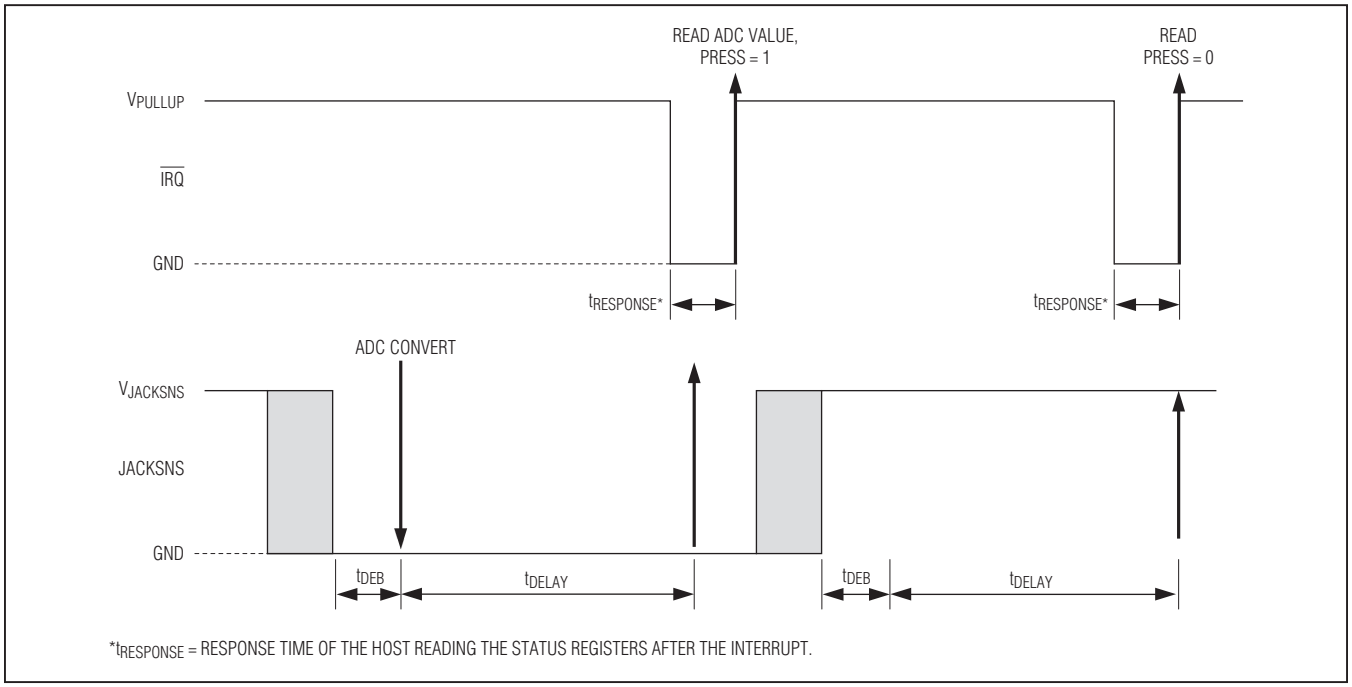


Figure 46. MBH Timing t_{DELAY}

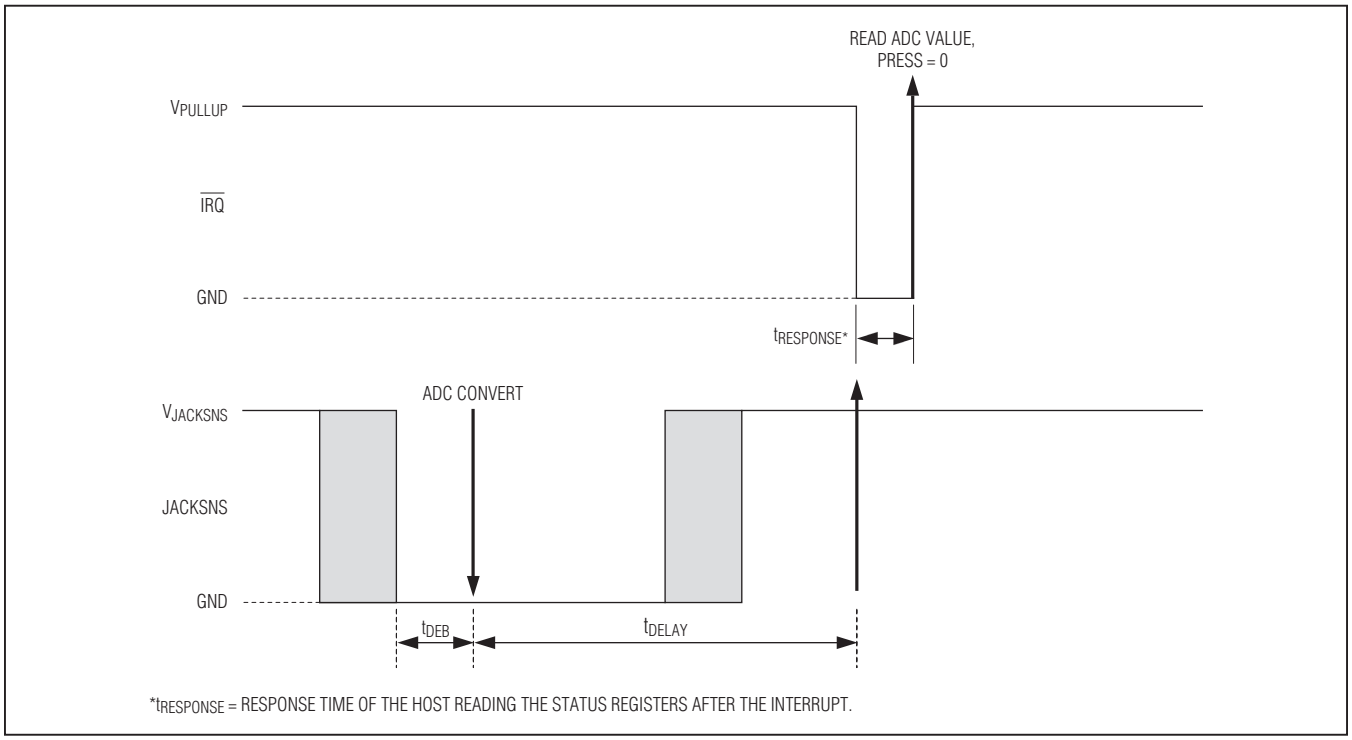


Figure 47. MBH Timing t_{DELAY}

Table 33. Key Switch Encoder Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
STATUS (Read Only)		
0x07	Auto Jack Detection	0/1
0x0A	ACC ADC	0/1
INTERRUPT CONTROL		
0x13	Jack Detect Interrupt Enabled 1	0
JACK DETECTION		
0x8B	Keyscan Debounce	0
0x8C	Keyscan Delay	0
0x8D	Key Threshold	0

Slow Jack Removal

Removing the headphone jack slowly can cause a false trigger of the key switch encoder because the right headphone shorts between mic bias and gnd. The programmable delay time must be set by the system to mask out this slow removal so that an interrupt doesn't flag until the JKIN status bit tells the system the jack is unplugged. Figure 48 shows the timing and interrupt reporting for a slow jack removal event.

A mic removal event is triggered when JACKSNS transitions from a lower voltage to MICBIAS2.

Interrupt ($\overline{IRQ}$)

The IC features an interrupt signal through the open drain $\overline{IRQ}$ output. The Interrupt Control register allows the user to select which status bits pull $\overline{IRQ}$ low to flag the host. The $\overline{IRQ}$ is pull low when a status bit is high. Table 34 shows the codec interrupt controls and their associated status bits.

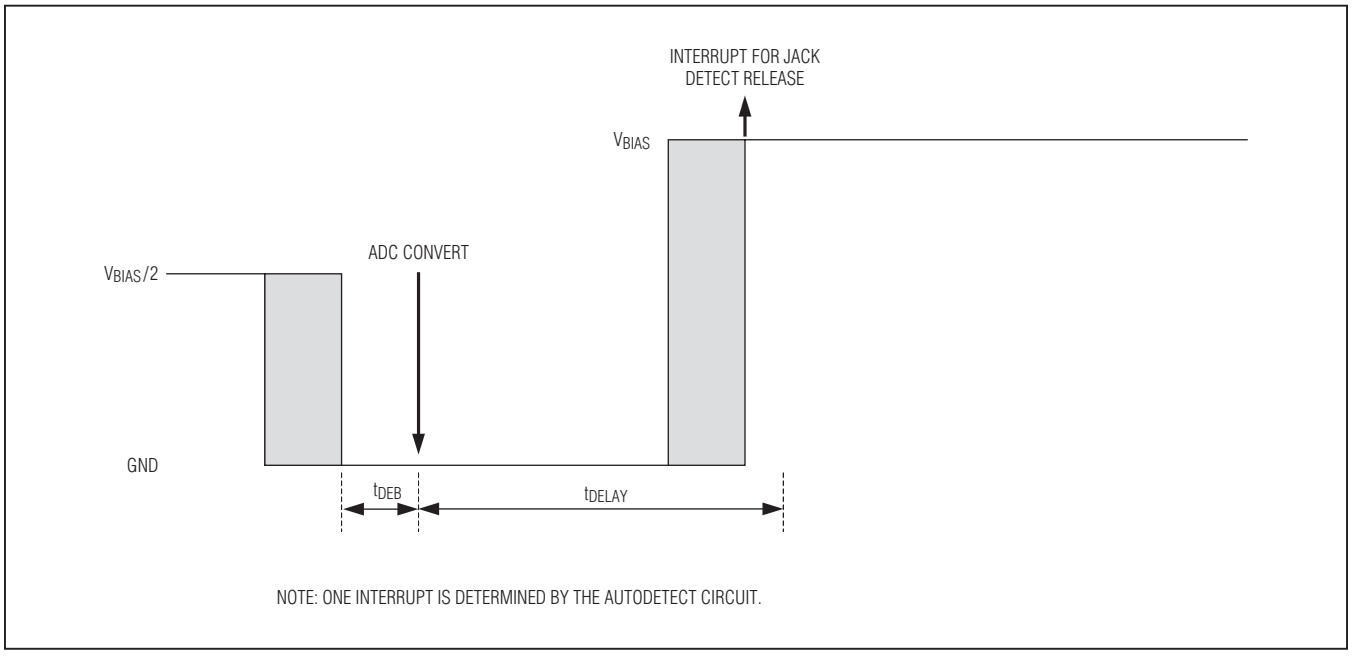


Figure 48. Slow Jack Removal Timing

Table 34. Codec Interrupt Control Bits and Their Associated Status Bits

INTERRUPT CONTROL		STATUS		INTERRUPT CONTROL		STATUS	
REGISTER	BIT NAME	REGISTER	BIT NAME	REGISTER	BIT NAME	REGISTER	BIT NAME
0x12	ICLD	0x04	CLD	0x13	IDDONE	0x07	DDONE
0x12	ISLD	0x04	SLD	0x13	IIHP_IN	0x07	IHP_IN
0x12	IULK3	0x04	ULK3	0x13	ILO_IN	0x07	LO_IN
0x12	IULK2	0x04	ULK2	0x13	IMIC_IN	0x07	MIC_IN
0x12	IULK3	0x04	ULK1	0x13	ITTY_IN	0x07	TTY_IN
0x12	IALCACT	0x05, 0x06	ALC_ACT_	0x13	IMCSW	0x07	MCSW
0x12	IALCCLP	0x05, 0x06	ALCCLP_	0x13	IKEYDET	0x07	KEYDET
0x12	IDCRYPT	0x04	DCRPTOK	0x14	IJKDET	0x08	JKDET
			DCPTDN				

Table 35. Interrupt/Status Register Names and Addresses

ADDRESS	REGISTER NAME	PAGE
STATUS (Read Only)		
0x01	Host Interrupt Status	0/1
0x02	Host Read Status	0/1
0x03	Host Write Status	0/1
0x04	Codec Status	0/1
0x05	ALC Status DAI 1	0/1
0x06	ALC Status DAI 2	0/1
0x07	Auto Jack Detection	0/1
0x08	Jack Detection	0/1
0x09	Batt ADC	0/1
0x0A	ACC ADC	0/1
0x0C	Left Speaker Voltage	0/1
0x0D	Right Speaker Voltage	0/1
0x0E	Batt ADC	0/1
INTERRUPT CONTROL		
0x10	Host Interrupt Config	0
0x11	Host Interrupt Enable	0
0x12	Codec Interrupt Enable	0
0x13	Jack Detect Interrupt Enable 1	0
0x14	Jack Detect Interrupt Enable 2	0

Control Interface

The IC can be controlled by either I²C or SPI. Set I2CMODE low to select I²C or set it high to select SPI. Both interface protocols allow access to the register map and the FlexSound processor host interface. The IC features two segments of registers. Set the segment pointer low to write/read from the registers in segment 0, and set the segment pointer high to write/read from the registers in segment 1. Refer to the *IC Register Map and Descriptions* document for details on programming the IC.

I²C Serial Interface

The IC features an I²C/SMBus-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. Figure 5 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP

(P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low-to-high transition on SDA while SCL is high (Figure 49). A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the IC the seven most significant bits are defined by ADDR as shown in Table 36. Setting the read/write bit to 1 configures the IC for read mode. Setting the read/write bit to 0 configures the IC for write mode. The address is the first byte of information sent to the IC after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt each byte of data when in write mode (Figure 50). The IC pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

Table 36. I²C Slave Address

V_{ADDR}	HEX SLAVE ADDRESS		BINARY SLAVE ADDRESS	
	READ	WRITE	READ	WRITE
V_{AGND}	0x21	0x20	00100001	00100000
V_{DVDDA}	0x23	0x22	00100011	00100010
$V_{SCL/SCLK}$	0x27	0x26	00100111	00100110

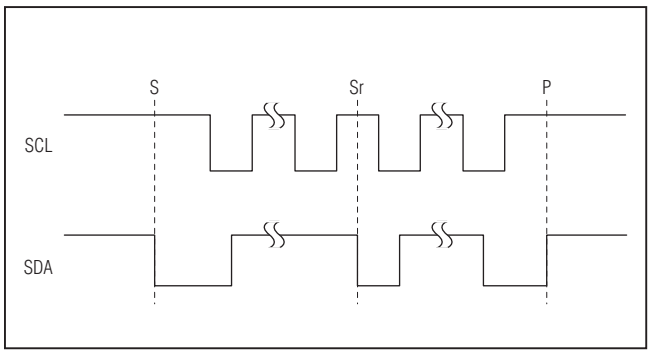


Figure 49. START, STOP, and REPEATED START Conditions

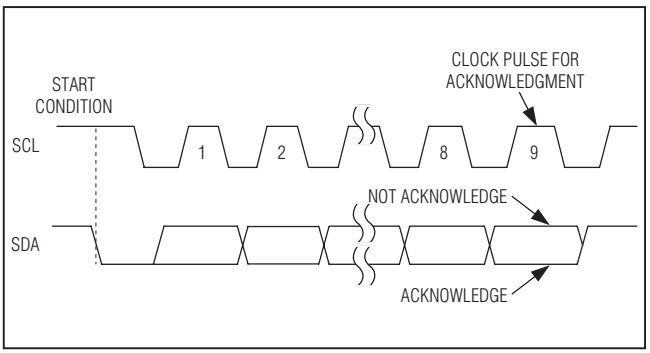


Figure 50. Acknowledge

Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 51 illustrates the proper frame format for writing one byte of data to the IC. Figure 52 illustrates the frame format for writing n-bytes of data to the IC.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that are written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte except for register 0x00. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. The autoincrement does not rollover to the next page.

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the IC is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. The autoincrement does not rollover to the next page. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the IC's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The

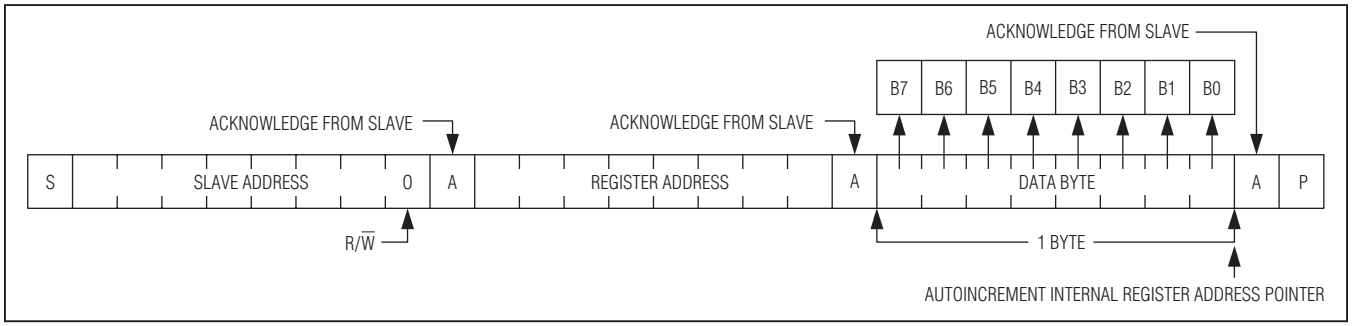


Figure 51. Writing One Byte of Data to the IC

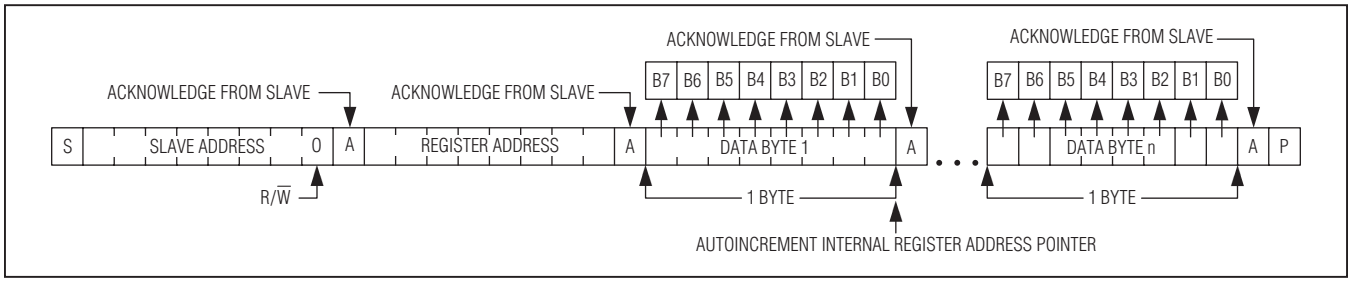


Figure 52. Writing n-Bytes of Data to the IC

IC then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 53 illustrates the frame format for reading one byte from the IC. Figure 54 illustrates the frame format for reading multiple bytes from the IC.

Serial Peripheral Interface (SPI)

For applications where an I²C master is not available or clock speeds higher than 400kHz are needed use the IC's SPI interface. The SPI interface supports clock speeds up to 26MHz using SCLK, MOSI, MISO, and $\overline{CS}$.

Serial Clock (SCLK)

The external SPI master provides the SCLK signal to clock the SPI interface. The IC samples the MOSI input data on the rising edge of SCLK and changes the output data (MISO) on the falling edge of SCLK. The IC ignores SCLK transitions when $\overline{CS}$ is high.

Chip Select ($\overline{CS}$)

The SPI interface is active only when $\overline{CS}$ is low. When $\overline{CS}$ is high, the IC set the MISO output high impedance and resets the internal SPI logic. If $\overline{CS}$ goes high in the middle of an SPI transfer, all the data is discarded. When $\overline{CS}$ is low, unless the register address is correctly decoded by the IC, the MISO output set high impedance.

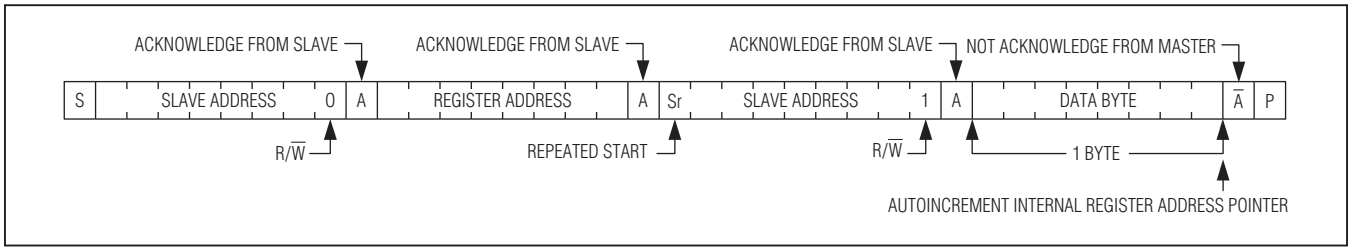


Figure 53. Reading One Byte of Data from the IC

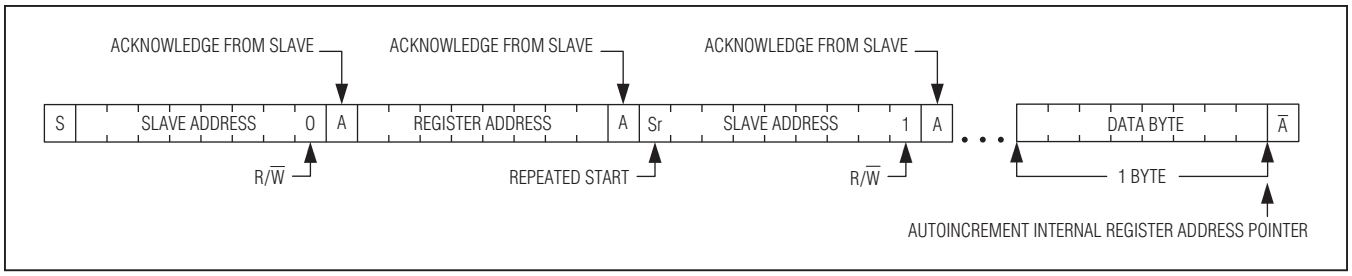


Figure 54. Reading n-Bytes of Data from the IC

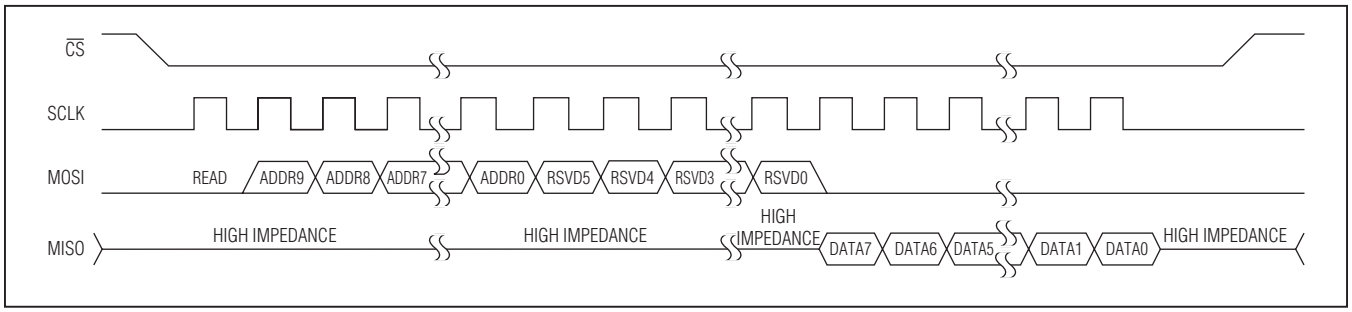


Figure 55. SPI Byte Write

Write Format

For an SPI write transfer, write a 1, followed by the 10-bit address MSB first, 5 reserved bits, and finally the 8 data bits on MOSI (Figure 55). For multiple write repeat, write a 1, followed by the 10-bit address MSB first, 5 reserved bits, and finally the 8 data bits on MOSI for up to the maximum of eight times (Figure 56).

Read Format

For an SPI read transfer, write a 0, followed by the 10-bit address MSB first, and 5 reserved bits on MOSI. During the next 8 clock cycles read back the 8 data bits on MISO (Figure 57). The SPI autoincrement for multiple bytes reads for a maximum of eight bytes (Figure 58).

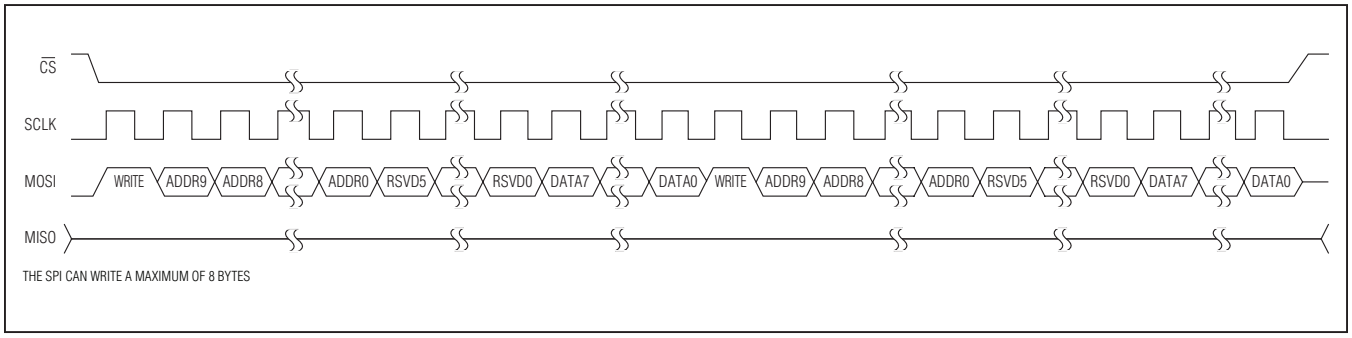


Figure 56. SPI Multiple Byte Write

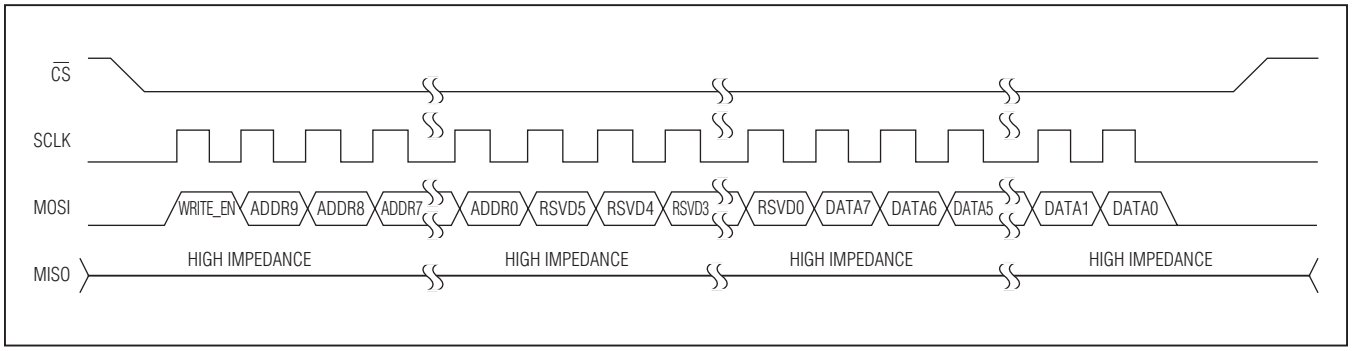


Figure 57. SPI Read Format

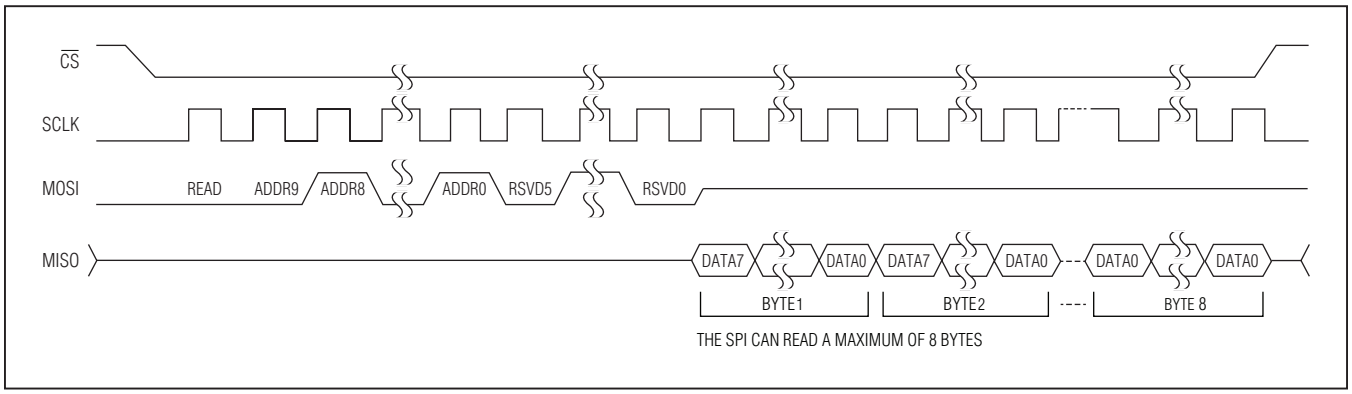


Figure 58. SPI Read Format

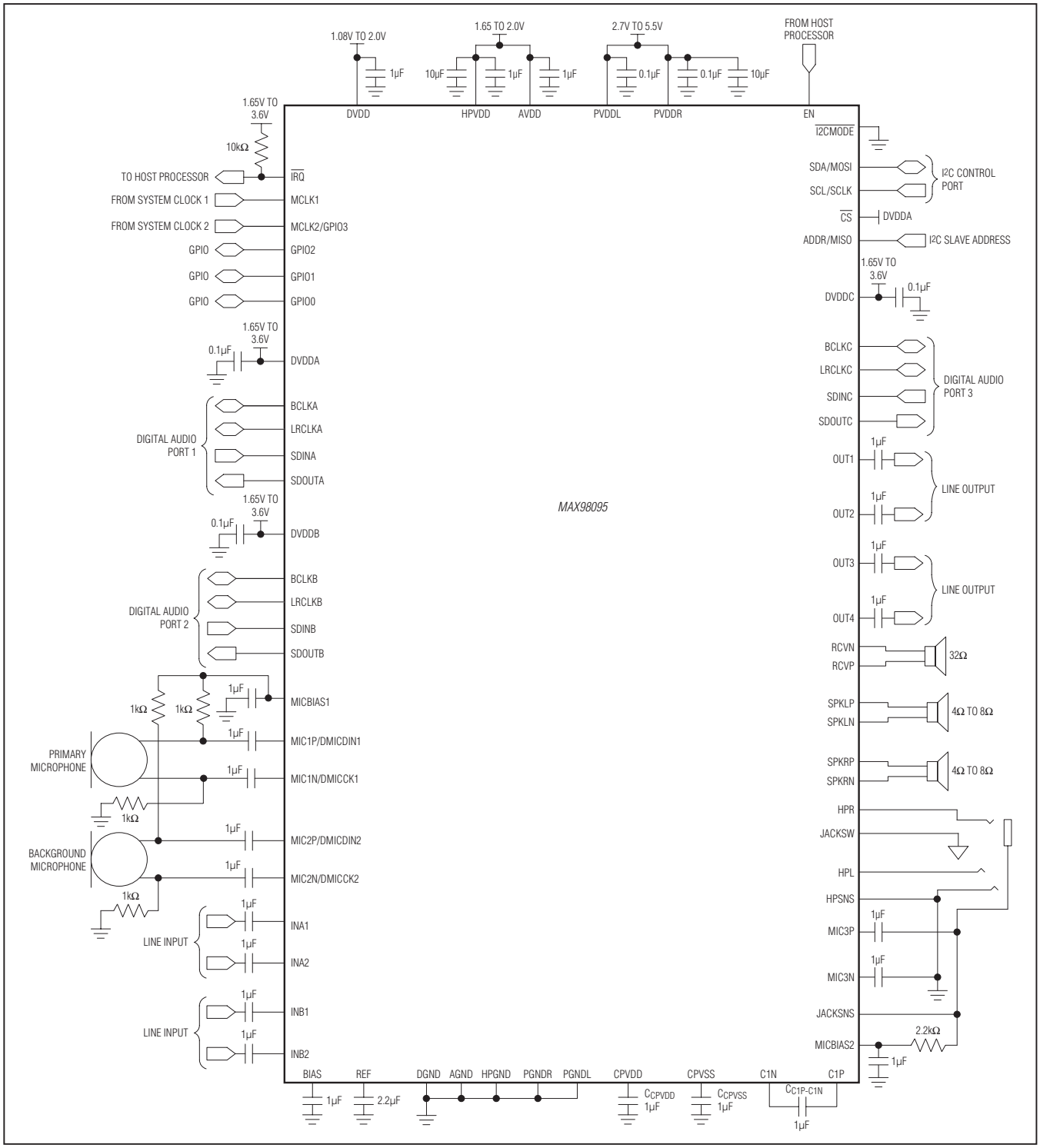


Figure 59. Typical Operating Circuit with Analog Microphones and I2C Host Interface

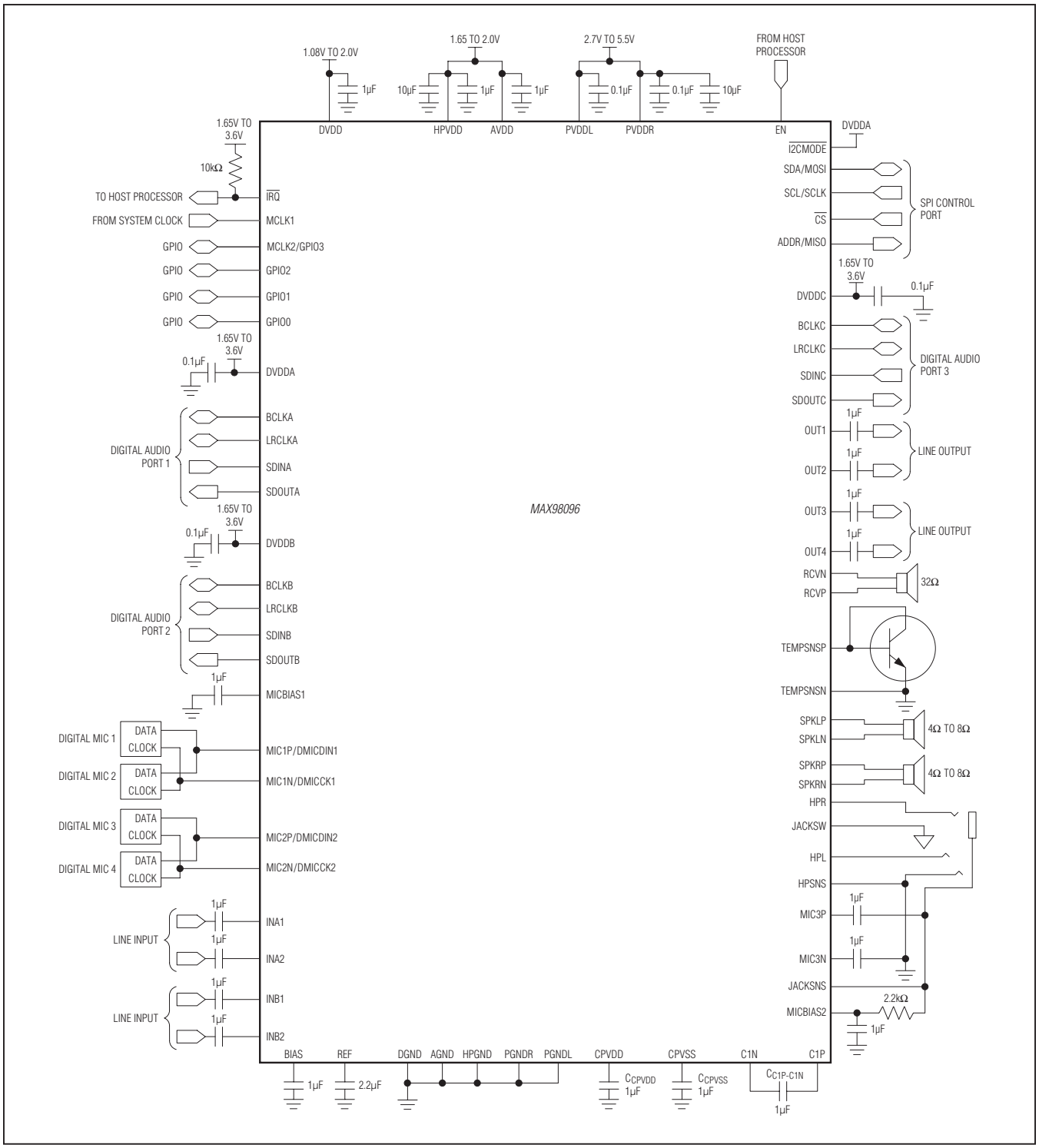


Figure 60. Typical Operating Circuit with Digital Microphones and SPI Host Interface

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (2 x V_{DD} peak-to-peak) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The IC's Class D amplifier does not require an output filter. The IC uses a special modulation method that relies on the inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

Because the Class D modulation frequency of the IC output is well beyond the bandwidth of most speakers, the voice coil movement due to the switching frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance >10µH. Typical 4Ω speakers exhibit series inductances in the 20µH to 100µH range.

Power Sequence

When first applying power to the IC, ensure that PVDD_ is applied first followed by the AVDD, HPVDD, DVDD and DVDD_.

Startup/Shutdown Sequencing

To ensure proper device initialization and minimal click-and-pop, program the IC's control registers in the correct order. The IC features two levels of software shutdown. The $\overline{SHDN}$ is an active-low shutdown that places everything, but the control interface in shutdown. The CODEC_SHDN is an active-high shutdown that places the codec in shutdown, but allows the FlexSound processor continue to run and maintain the contents in memory. Use CODEC_SHDN when you want to change the paths without disturbing the FlexSound processor. Table 37 lists the correct startup sequence for the device.

While many configuration options in the IC can be made while the device is operating, some registers should only be adjusted with CODEC_SHDN = 1.

Table 38 lists the registers that should not be adjusted during operation.

Table 37. Startup Sequence

SEQUENCE	DESCRIPTION	SEQUENCE	DESCRIPTION
1	Ensure $\overline{SHDN}$ = 0	6	Configure mixers
2	Configure clocks	7	Configure gain and volume controls
3	Configure digital audio interface	8	Configure miscellaneous functions
4	Configure digital signal processing	9	Enable desired functions
5	Load coefficients	10	Set $\overline{SHDN}$ = 1

Table 38. Register Changes that Require CODEC_SHDN = 1

DESCRIPTION	REGISTER		
	ADDRESS	REGISTER NAME	PAGE
Clock Control Registers	**CODEC CLOCK CONTROL**		
	0x26	Codec Clock Configuration	0
	DAI1 CLOCK CONTROL		
	0x27	DAI1 Clock Mode	0
	0x28	DAI1 AnyClock Control	0
	0x29	DAI1 AnyClock Control	0
	0x2B	DAI1 AnyClock Control	0

Table 38. Register Changes that Require CODEC_SHDN = 1 (continued)

DESCRIPTION	REGISTER		
	ADDRESS	REGISTER NAME	PAGE
Clock Control Registers	**DAI2 CLOCK CONTROL**		
	0x31	DAI2 Clock Mode	0
	0x32	DAI2 AnyClock Control	0
	0x33	DAI2 AnyClock Control	0
	0x35	DAI2 AnyClock Control	0
	DAI3 CLOCK CONTROL		
	0x3B	DAI3 Clock Mode	0
	0x3C	DAI3 AnyClock Control	0
	0x3D	DAI3 AnyClock Control	0
	0x3F	DAI3 AnyClock Control	0
Digital Audio Interface Configuration	**DAI1 CONFIGURATION**		
	0x2A	DAI1 Format	0
	0x2B	DAI1 Clock	0
	0x2C	DAI1 I/O Configuration	0
	0x2D	DAI1 Time-Division Multiplex	0
	DAI2 CONFIGURATION		
	0x34	DAI2 Format	0
	0x35	DAI2 Clock	0
	0x36	DAI2 I/O Configuration	0
	0x37	DAI2 Time-Division Multiplex	0
	DAI3 CONFIGURATION		
	0x3E	DAI3 Format	0
	0x3F	DAI3 Clock	0
	0x40	DAI3 I/O Configuration	0
	0x41	DAI3 Time-Division Multiplex	0
Digital Passband Filters	**DAI1 CONFIGURATION**		
	0x2E	DAI1 Filters	0
	DAI1 SDOUT MIXER LEVEL CONTROL		
	0x2F	DAI1 Level Control	0
	0x30	DAI1 Level Control	0
	DAI2 CONFIGURATION		
	0x38	DAI2 Filters	0
	DAI2 SDOUT MIXER LEVEL CONTROL		
	0x39	DAI2 Level Control	0x39
	0x3A	DAI2 Level Control	0x3A
	DAI3 CONFIGURATION		
	0x42	DAI3 Filters	0
	DAI3 SDOUT MIXER LEVEL CONTROL		
	0x43	DAI3 Level control	0
	0x44	DAI3 Level control	0

Table 38. Register Changes that Require CODEC_SHDN = 1 (continued)

DESCRIPTION	REGISTER		
	ADDRESS	REGISTER NAME	PAGE
ANALOG MIXER*	**MIXER**		
	0x48	Stereo DAC	0
	0x49	Mono DAC	0
	0x4A	Left ADC	0
	0x4B	Right ADC	0
	0x4C	Left Headphone	0
	0x4D	Right Headphone	0
	0x4E	Headphone Gain	0
	0x4F	Earpiece	0
	0x50	Left Speaker	0
	0x51	Right Speaker	0
	0x52	Speaker Gain	0
	0x53	Line Output Mixer 1	0
	0x54	Line Output Mixer 2	0
	0x55	Line Output Control	0
Digital Signal Processing Coefficients	**FILTER COEFFICIENTS**		
	0x10 - 0x19	EQ Band 1 (DAI1)	1
	0x1A - 0x23	EQ Band 2 (DAI1)	1
	0x24 - 0x2D	EQ Band 3 (DAI1)	1
	0x2E - 0x37	EQ Band 4 (DAI1)	1
	0x38 - 0x41	EQ Band 5 (DAI1)	1
	0x42 - 0x4B	EQ Band 1 (DAI2)	1
	0x4C - 0x55	EQ Band 2 (DAI2)	1
	0x56 - 0x5F	EQ Band 3 (DAI2)	1
	0x60 - 0x69	EQ Band 4 (DAI2)	1
	0x6A - 0x73	EQ Band 5 (DAI2)	1
	0x74 - 0x7D	Biquad Filter 1 (DAI1)	1
	0x7E - 0x87	Biquad Filter 1 (DAI2)	1
	0x88 - 0x91	Biquad Filter 2 (DAI1)	1
	0x92 - 0x9B	Biquad Filter 2 (DAI2)	1
	0xA6 - 0xAF	Crossover Filter 1 (DAI1)	1
	0xB0 - 0xB9	Crossover Filter 2 (DAI1)	1
	0xBA - 0xC3	Crossover Filter 1 (DAI2)	1

**To help reduce click and pop.*

Component Selection

Optional Ferrite Bead Filter

In applications where Class D speaker leads exceed 20mm, additional EMI suppression can be achieved by using a filter constructed from a ferrite bead and a capacitor to ground (Figure 61). Use a ferrite bead with low DC resistance, high frequency (> 600MHz) impedance between 100Ω and 600Ω, and rated for at least 1A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select a capacitor less than 1nF based on EMI performance.

Input Capacitor

An input capacitor, C_{IN}, in conjunction with the input impedance of the IC line inputs forms a highpass filter that removes the DC bias from an incoming analog signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface mount ceramic capacitors satisfy the ESR requirement.

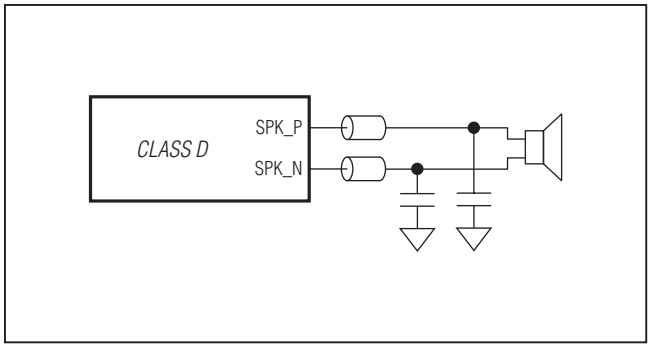


Figure 61. Optional Class D Ferrite Bead Filter

For best performance over the extended temperature range, select capacitors with an X7R dielectric.

Charge-Pump Flying Capacitor ($C_{C1P-C1N}$)

The value of the flying capacitor (connected between C1N and C1P) affects the output resistance of the charge pump. A value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of the flying capacitor reduces the charge-pump output resistance to an extent. Above 1µF, the on-resistance of the internal switches and the ESR of external charge-pump capacitors dominate.

Charge-Pump Holding Capacitor (C_{CPVDD}, C_{CPVSS})

The holding capacitor (bypassing CPVDD and CPVSS to ground) value and ESR directly affect the ripple at CPVDD and CPVSS. Increasing the capacitor's value reduces output ripple. Likewise, decreasing the ESR reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* section for more information.

Ambient Temperature Sensor

The IC uses an external NPN transistor to sense the ambient temperature of the system. The transistor should be placed as close as possible to the speaker. The emitter of the transistor should be connected to ground at the location of the transistor and TEMPSNSN should be used to sense the ground voltage at that location. See Figure 59 or Figure 60 for how to connect the transistor to the MAX98096. Table 39 lists the recommended components to use for the sense transistor.

Table 39. Recommended Ambient Temperature Transistors

MANUFACTURER	PART NO.
Central Semiconductor	CMPT3904
Rohm Semiconductor	SST3904
Samsung Semiconductor	KST3904-TF
Seimens	SMBT3904
Zetex	FMMT3904CT-ND

Table 40. Recommended Connections for Unused Pins

NAME	CONNECTION	NAME	CONNECTION	NAME	CONNECTION
SDOUTA	Unconnected	MCLK1	Always connect	JACKSNS	Unconnected
SDINA	DGND	MCLK2/GPIO3	Unconnected	CPVSS	Unconnected
LRCLKA	Unconnected	GPIO2	Unconnected	HPGND	Always connect
SDINC/TDI	DGND	N.C.	Unconnected	HPVDD	Always connect
LRCLKC/TCK	Unconnected	GPIO0	Unconnected	$\overline{CS}$	DVDDA
DVDDC	DVDD	TEMPSNSN	AGND	MIC3N	Unconnected
SDINB/TRST	DGND	PGNDL	Always connect	MIC2N/DMICCK2	Unconnected
LRCLKB	Unconnected	PGNDR	Always connect	MIC2P/DMICDIN2	Unconnected
DVDDB	DVDD	SPKRN	Unconnected	INB2	Unconnected
SPKLP	Unconnected	DVDD	Always connect	INB1	Unconnected
SPKLN	Unconnected	OUT3	Unconnected	JACKSW	Unconnected
PVDDR	Always connect	TEMPSNSP	AGND	HPSNS	AGND
DVDDA	DVDD	RCVN	Unconnected	C1N	Unconnected
BCLKA	Unconnected	RCVP	Unconnected	C1P	Unconnected
SDOUTC/ TDO	Unconnected	ADDR/MISO	Always connect	MIC3P	Unconnected
BCLKC	Unconnected	AGND	Always connect	MICBIAS2	Unconnected
GPIO1	Unconnected	AVDD	Always connect	MICBIAS1	Unconnected
SDOUTB	Unconnected	SDA/MOSI	Always connect	MIC1N/DMICCK1	Unconnected
BCLKB	Unconnected	OUT2	Unconnected	MIC1P/DMICDIN1	Unconnected
EN	Always connect	BIAS	Always connect	INA2	Unconnected
PVDDL	Always connect	REF	Always connect	INA1	Unconnected
SPKRP	Unconnected	SCL/SCLK	Always connect	HPR	Unconnected
DGND	Always connect	OUT4	Unconnected	HPL	Unconnected
$\overline{I2CMODE}$	Always connect	$\overline{IRQ}$	Unconnected	CPVDD	Unconnected

Unused Pins

Table 40 shows how to connect the IC pins when circuit blocks are unused.

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. When designing a PCB for the ICs, partition the circuitry so that the analog sections of the IC are separated from the digital sections. This ensures that the analog audio traces are not routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND, DGND, HPGND, SPKLGND, and SPKRGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signals.

Ground the bypass capacitors on MICBIAS1, MICBIAS2, BIAS, and REF directly to the ground plane with minimum trace length. Also, be sure to minimize the path length to AGND. Bypass AVDD directly to AGND.

Connect all digital I/O termination to the ground plane with minimum path length to DGND. Bypass DVDD, DVDDA, DVDDB, and DVDDC directly to DGND.

Place the capacitor between C1P and C1N as close as possible to the IC to minimize trace length from C1P to C1N. Inductance and resistance added between C1P and

C1N reduce the output power of the headphone amplifier. Bypass CPVDD and CPVSS with a capacitor located close to CPVSS with a short trace length to HPGND. Close decoupling of CPVSS minimizes supply ripple and maximizes output power from the headphone amplifier.

HPSNS senses ground noise on the headphone jack and adds the same noise to the output audio signal, thereby making the output (headphone output minus ground) noise free. Connect HPSNS to the headphone jack shield to ensure accurate pickup of headphone ground noise.

Bypass PVDDL and PVDDR to PGNDL and PGNDL, respectively, with as little trace length as possible. Connect SPKLP, SPKLN, SPKRP, and SPKRN to the stereo speakers using the shortest traces possible. Reducing trace length minimizes radiated EMI. Route SPKLP/SPKLN and SPKRP/SPKRN as differential pairs on the PCB to minimize loop area, thereby the inductance of the circuit. If filter components are used on the speaker outputs, be sure to locate them as close as possible to the IC to ensure maximum effectiveness. Minimize the trace length from any ground-connected passive components to PGNDL and PGNDL to further minimize radiated EMI.

Use Cases

The IC includes three digital audio interfaces capable of operating a completely separate sample rates simultaneously. In addition, a number of mixers and three sample rate converters are provided to support a wide range of use cases. Figure 62 and Figure 63 show two example use cases to demonstrate the what is possible.

Recording a Voice Call with Music

Figure 63 illustrates a phone call through a Bluetooth device with music from the application processor mixed into the transmit and receive voice paths. The music, transmit voice, and receive voice are sent back to the application processor to be recorded.

Recording a Bluetooth Call with Music

The IC is capable of mixing signal from up to three different sample rates. Figure 63 illustrates a phone call through a Bluetooth® device with music playing from the application processor for the up link and mixed in the down link. The music, uplink and down link can be sent back to the application processor to be recorded.

Recommended PCB Routing

The IC uses a 108-bump WLP package. Figure 64 provides an example of how to connect to all active bumps using 3 layers of the PCB. To ensure uninterrupted ground returns, use layer 2 as a connecting layer between layer 1 and layer 2 and flood the remaining area with ground.

RF Susceptibility

GSM radios transmit using time-division multiple access (TDMA) with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers. The IC is designed specifically to reject RF signals, however, PCB layout has a large impact on the susceptibility of the end product.

Improvements to both layout and component selection decreases the IC's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Keep PCB trace lengths shorter than 1/4 of the wavelength of the RF frequency of interest. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the IC. The wavelength (λ) in meters is given by: $\lambda = c/f$ where $c = 3 \times 10^8$ m/s, and f = the RF frequency of interest.

Route audio signals on middle layers of the PCB to allow ground planes above and below to shield them from RF interference. Ideally the top and bottom layers of the PCB should primarily be ground planes to create effective shielding, in Hertz.

Additional RF immunity can also be obtained by relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self-resonance at RF frequencies. These capacitors when placed at the input pins can effectively shunt the RF noise at the inputs of the IC. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane. Avoid using microvias to connect to the ground plane whenever possible as these vias do not conduct well at RF frequencies.

WLP Applications Information

Refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications* for the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results. Figure 65 shows the dimensions of the WLP balls used on the IC.

Bluetooth is a registered trademark owned by Bluetooth SIG, Inc.

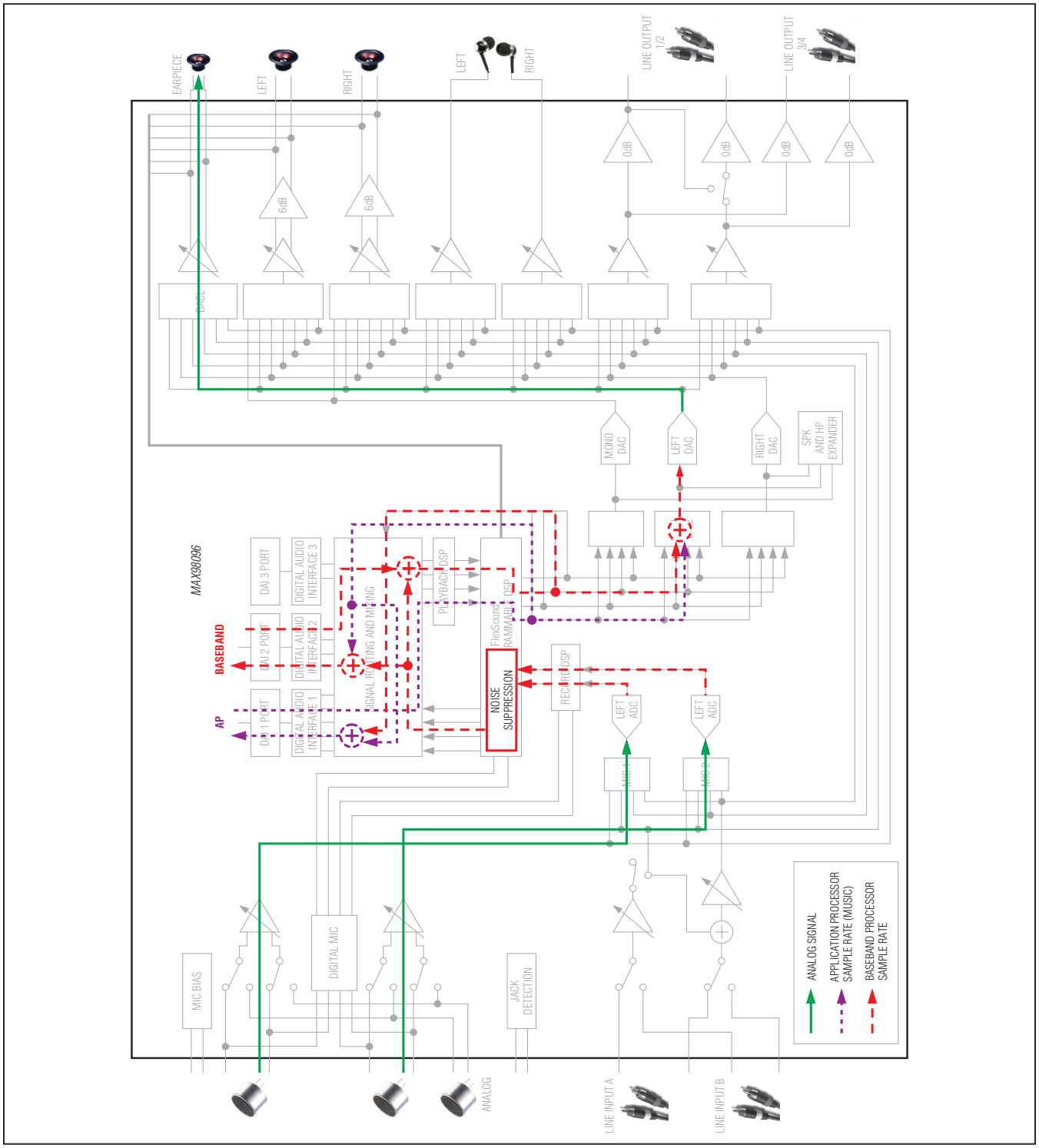


Figure 62. Recording a Phone Call with Music

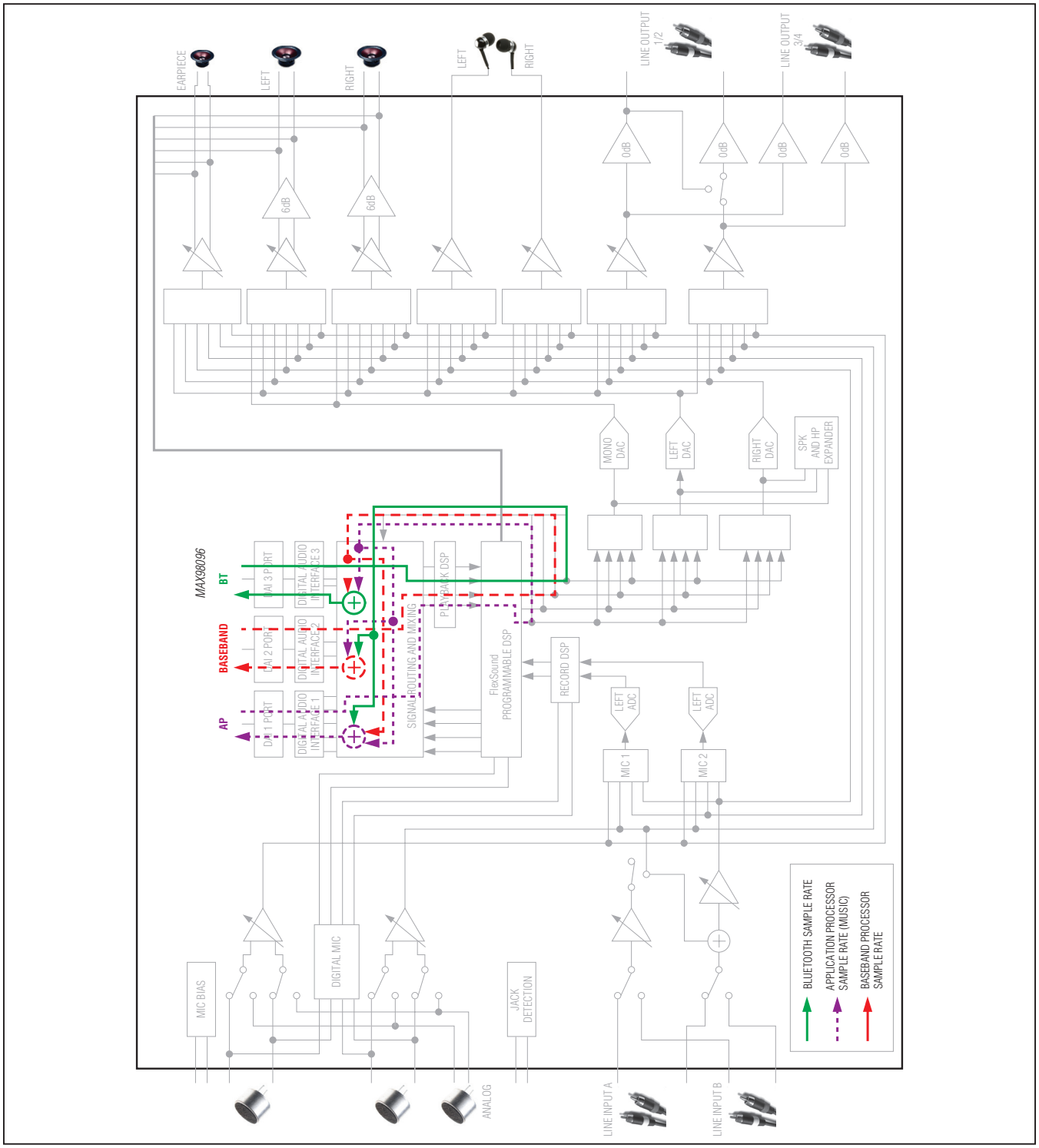


Figure 63. Recording a Blue Tooth Phone Call with Music

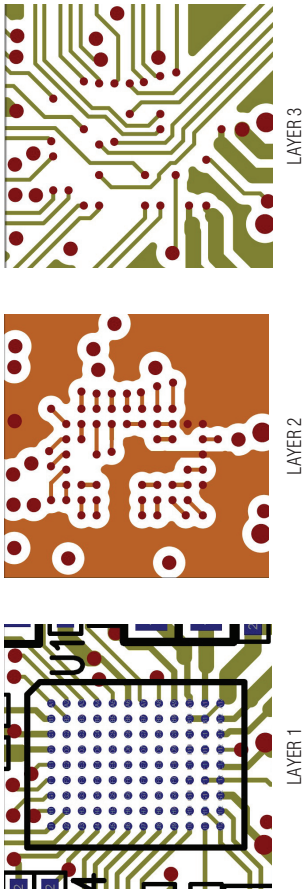


Figure 64. Suggested Routing

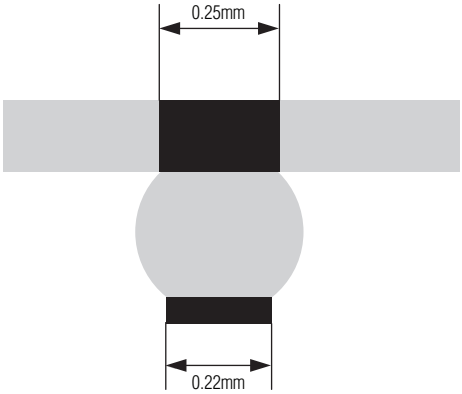


Figure 65. WLP Ball Dimensions

Ordering Information

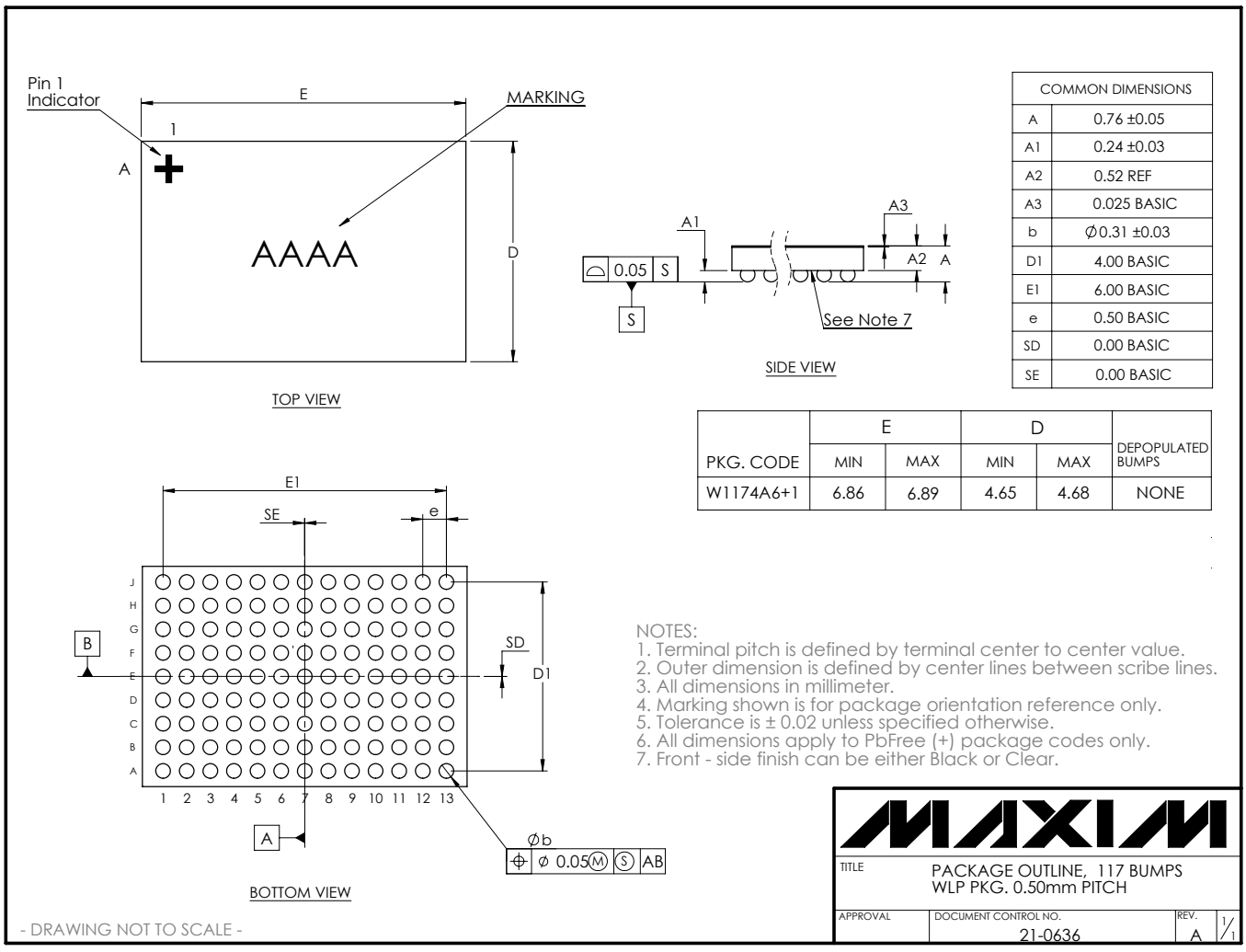
PART	TEMP RANGE	PIN-PACKAGE
MAX98096EWF+T	-40°C to +85°C	117 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
117 WLP	W1174A6+1	21-0636	Refer to Application Note 1891



COMMON DIMENSIONS	
A	0.76 ±0.05
A1	0.24 ±0.03
A2	0.52 REF
A3	0.025 BASIC
b	∅0.31 ±0.03
D1	4.00 BASIC
E1	6.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W1174A6+1	6.86	6.89	4.65	4.68	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

MAXIM

TITLE	PACKAGE OUTLINE, 117 BUMPS WLP PKG. 0.50mm PITCH		
APPROVAL	DOCUMENT CONTROL NO. 21-0636	REV. A	1/1

Audio Hub with Wideband FlexSound Processor

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—