

Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM
CMOS

16M (×8/×16) FLASH MEMORY & 4M (×8/×16) STATIC RAM

MB84VD2118XEM-70/MB84VD2119XEM-70

■ FEATURES

- Power Supply Voltage of 2.7 V to 3.3 V
- High Performance
70 ns maximum access time (Flash)
70 ns maximum access time (SRAM)
- Operating Temperature
−40°C to +85°C
- Package 56-ball BGA

(Continued)

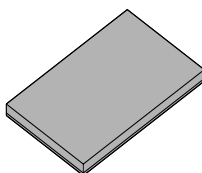
■ PRODUCT LINE UP

Part No.	MB84VD2118XEM/MB84VD2119XEM	
Supply Voltage(V)	V _{ccf} = 3.0V ^{+0.3V} _{−0.3V}	V _{ccs} = 3.0V ^{+0.3V} _{−0.3V}
Max. Address Access Time (ns)	70	70
Max. $\overline{\text{CE}}$ Access Time (ns)	70	70
Max. $\overline{\text{OE}}$ Access Time (ns)	30	35

Note: Both V_{ccf} and V_{ccs} must be in recommended operation range when either part is being accessed.

■ PACKAGE

56-ball plastic BGA



(BGA-56P-M02)

(Continued)

— FLASH MEMORY

- **Simultaneous Read/Write Operations (Dual Bank)**

Multiple devices available with different bank sizes (Please refer to ORDERING INFORMATION)

Host system can program or erase in one bank, then immediately and simultaneously read from the other bank

Zero latency between read and write operations

Read-while-erase

Read-while-program

- **Minimum 100,000 Write/Erase Cycles**

- **Sector Erase Architecture**

Eight 4 K words and thirty one 32 K words.

Any combination of sectors can be concurrently erased. Also supports full chip erase.

- **Boot Code Sector Architecture**

MB84VD2118XEM: Top sector

MB84VD2119XEM: Bottom sector

- **Embedded Erase™ Algorithms**

Automatically pre-programs and erases the chip or any sector

- **Embedded Program™ Algorithms**

Automatically writes and verifies data at specified address

- **Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**

- **Ready-Busy Output (RY/BY)**

Hardware method for detection of program or erase cycle completion

- **Automatic Sleep Mode**

When addresses remain stable, automatically switch themselves to low power mode.

- **Low V_{CC} Write Inhibit ≤ 2.5 V**

- **Hidden ROM (Hi-ROM) Region**

64K byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence

Factory serialized and protected to provide a secure electronic serial number (ESN)

- **WP/ACC Input Pin**

At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status

(MB84VD2118XEM:SA37,SA38 MB84VD2119XEM:SA0,SA1)

At V_{IH}, allows removal of boot sector protection

At V_{ACC}, program time will reduce by 40%.

- **Erase Suspend/Resume**

Suspends the erase operation to allow a read in another sector within the same device

- **Please refer to “MBM29DL16XTE/BE” Datasheet in Detailed Function**

— SRAM

- **Power Dissipation**

Operating : 40 mA max.

Standby : 15 μA max.

- **Power Down Features using $\overline{\text{CE1s}}$ and $\overline{\text{CE2s}}$**

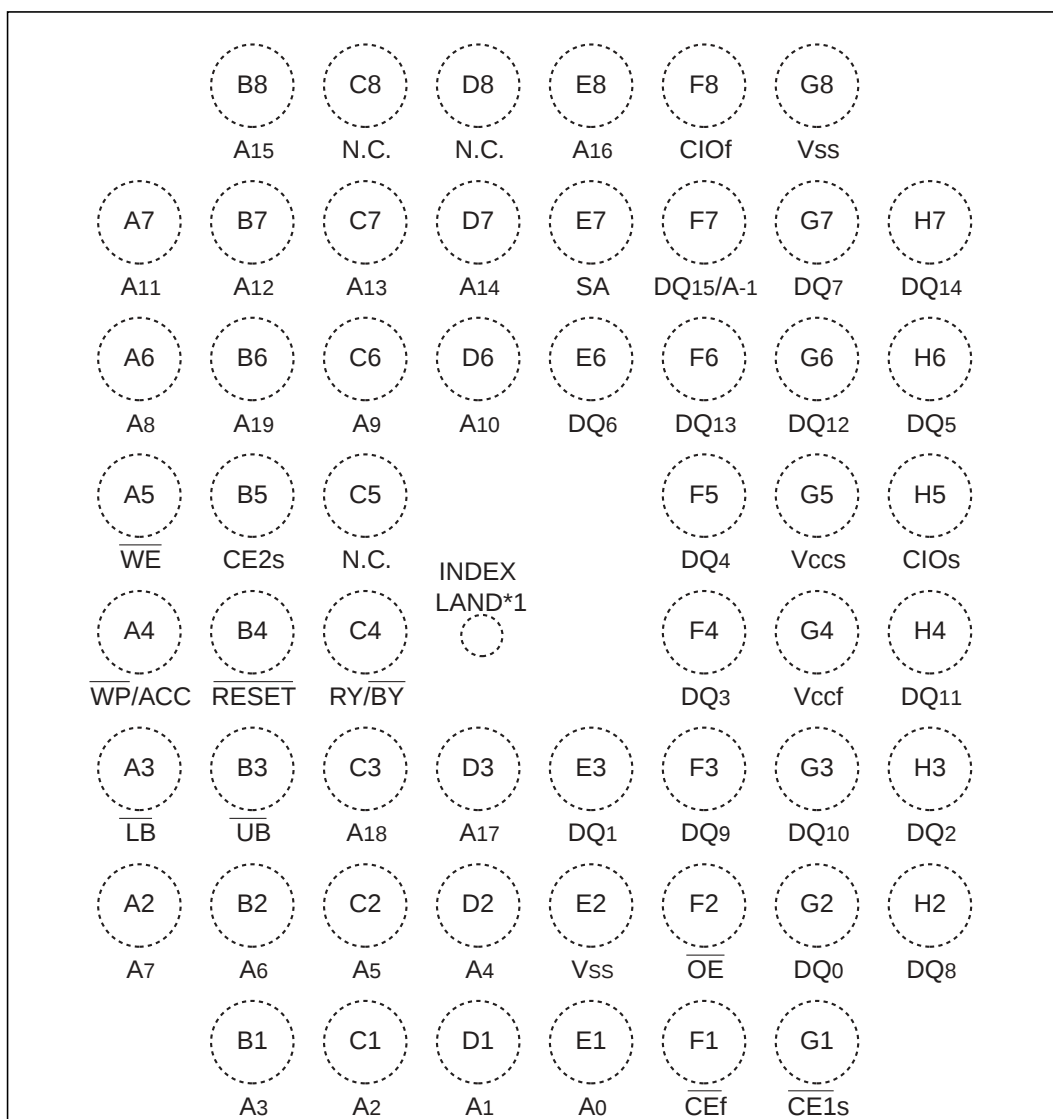
- **Data Retention Supply Voltage: 1.5 V to 3.3 V**

- **$\overline{\text{CE1s}}$ and $\overline{\text{CE2s}}$ Chip Select**

- **Byte Data Control: $\overline{\text{LB}}$ (DQ₀ to DQ₇), $\overline{\text{UB}}$ (DQ₈ to DQ₁₅)**

PIN ASSIGNMENT

(Top View)
Marking side



*1) There is no solder ball. This land should be open electrically.

(BGA-56P-M02)

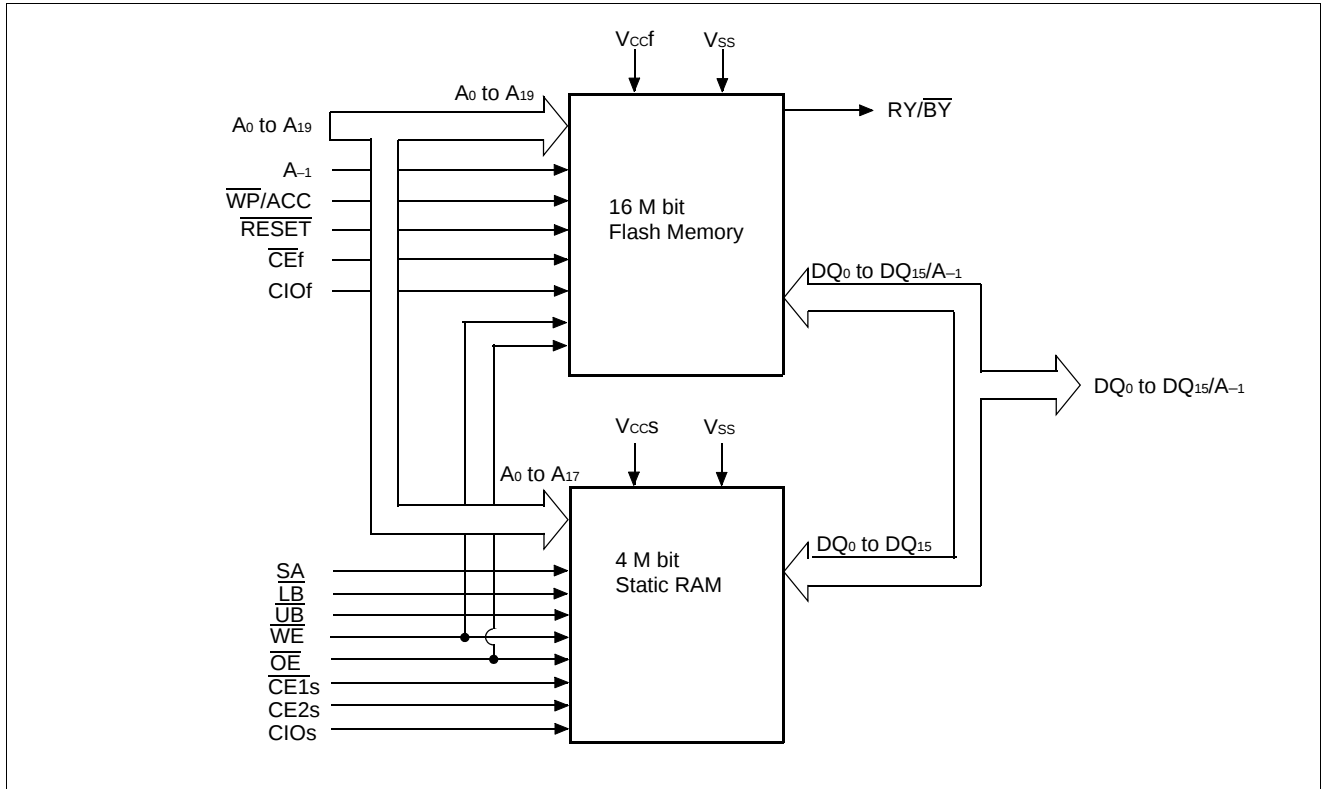
MB84VD2118XEM/MB84VD2119XEM-70

■ PIN DESCRIPTION

Pin Name	Function	Input/Output
A ₁₇ to A ₀	Address Inputs (Common)	I
A ₁₉ to A ₁₈ , A ₋₁	Address Input (Flash)	I
SA	Address Input (SRAM)	I
DQ ₁₅ to DQ ₀	Data Inputs / Outputs (Common)	I/O
$\overline{\text{CE}}_{\text{f}}$	Chip Enable (Flash)	I
$\overline{\text{CE}}_{1\text{s}}$	Chip Enable (SRAM)	I
CE _{2s}	Chip Enable (SRAM)	I
$\overline{\text{OE}}$	Output Enable (Common)	I
$\overline{\text{WE}}$	Write Enable (Common)	I
RY/ $\overline{\text{BY}}$	Ready/Busy Outputs (Flash) Open Drain Output	O
$\overline{\text{UB}}$	Upper Byte Control (SRAM)	I
$\overline{\text{LB}}$	Lower Byte Control (SRAM)	I
CIO _f	I/O Configuration (Flash) CIO _f =V _{ccf} is Word mode (× 16), CIO _f =V _{ss} is Byte mode (× 8)	I
CIO _s	I/O Configuration (SRAM) CIO _s =V _{ccs} is Word mode (× 16), CIO _s =V _{ss} is Byte mode (× 8)	I
$\overline{\text{RESET}}$	Hardware Reset Pin / Sector Protection Unlock (Flash)	I
$\overline{\text{WP/ACC}}$	Write Protect / Acceleration (Flash)	I
N.C.	No Internal Connection	—
V _{ss}	Device Ground (Common)	Power
V _{ccf}	Device Power Supply (Flash)	Power
V _{ccs}	Device Power Supply (SRAM)	Power

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■ BLOCK DIAGRAM



MB84VD2118XEM/MB84VD2119XEM-70

■ DEVICE BUS OPERATIONS

Table 1. 1 User Bus Operations (Flash=Word mode; CIOF=V_{ccf}, SRAM=Word mode; CIOs=V_{ccs})

Operation (1), (3)	$\overline{CEf}$	$\overline{CE1s}$	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅	$\overline{RESET}$	WP/ ACC (5)
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	High-Z	High-Z			
										X		
Read from Flash (2)	L	H	X	L	H	X	X	X	D _{OUT}	D _{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D _{IN}	D _{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	X	L	L	D _{OUT}	D _{OUT}	H	X
							H	L	High-Z	D _{OUT}		
							L	H	D _{OUT}	High-Z		
Write to SRAM	H	L	H	X	L	X	L	L	D _{IN}	D _{IN}	H	X
							H	L	High-Z	D _{IN}		
							L	H	D _{IN}	High-Z		
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

- Notes:**
1. Other operations except for indicated this column are inhibited.
 2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
 3. Do not apply $\overline{CEf}$ = V_{IL}, $\overline{CE1s}$ = V_{IL} and $\overline{CE2s}$ = V_{IH} at a time.
 4. It is also used for the extended sector group protections.
 5. $\overline{WP/ACC}$ = V_{IL}; protection of boot sectors.
 $\overline{WP/ACC}$ = V_{IH}; removal of boot sectors protection.
 $\overline{WP/ACC}$ = V_{ACC} (9V) ; Program time will reduce by 40%.

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Table 1. 2 User Bus Operations (Flash=Word mode; CIOf=V_{ccf}, SRAM=Byte mode; CIOs=V_{ss})

Operation (1), (3)	$\overline{CEf}$	$\overline{CE1s}$	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅	$\overline{RESET}$	$\overline{WP/ACC}$ (5)
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	X	High-Z	High-Z		
Read from Flash (2)	L	H	X	L	H	X	X	X	D _{OUT}	D _{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D _{IN}	D _{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	SA	X	X	D _{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	D _{IN}	High-Z	H	X
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

- Notes:**
1. Other operations except for indicated this column are inhibited.
 2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
 3. Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1s} = V_{IL}$ and $CE2s = V_{IH}$ at a time.
 4. It is also used for the extended sector group protections.
 5. $\overline{WP/ACC} = V_{IL}$; protection of boot sectors.
 $\overline{WP/ACC} = V_{IH}$; removal of boot sectors protection.
 $\overline{WP/ACC} = V_{ACC}$ (9V); Program time will reduce by 40%.

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Table 1. 3 User Bus Operations (Flash=Byte mode; CIOf=V_{SS}, SRAM=Byte mode; CIOs=V_{SS})

Operation (1), (3)	$\overline{CEf}$	$\overline{CE1s}$	CE2s	DQ _{15/A-1}	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₄	$\overline{RESET}$	$\overline{WP/ACC}$ (5)
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L										
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	X	H	H	High-Z	High-Z		
	L	H	X	A ₋₁	H	H	X	X	X	High-Z	High-Z		
Read from Flash (2)	L	H	X	A ₋₁	L	H	X	X	X	D _{OUT}	X	H	X
		X	L										
Write to Flash	L	H	X	A ₋₁	H	L	X	X	X	D _{IN}	X	H	X
		X	L										
Read from SRAM	H	L	H	X	L	H	SA	X	X	D _{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	SA	X	X	D _{IN}	High-Z	H	X
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	X	V _{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L										
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

- Notes:**
1. Other operations except for indicated this column are inhibited.
 2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
 3. Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1s} = V_{IL}$ and $CE2s = V_{IH}$ at a time.
 4. It is also used for the extended sector group protections.
 5. $\overline{WP/ACC} = V_{IL}$; protection of boot sectors.
 $\overline{WP/ACC} = V_{IH}$; removal of boot sectors protection.
 $\overline{WP/ACC} = V_{ACC}$ (9V); Program time will reduce by 40%.

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■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	T _{stg}	−55	+125	°C
Ambient Temperature with Power Applied	T _A	−40	+85	°C
Voltage with Respect to Ground All pins except RESET, $\overline{\text{WP/ACC}}$ (Note 1)	V _{IN} , V _{OUT}	−0.3	V _{ccf} +0.4	V
			V _{ccs} +0.4	V
V _{ccf} /V _{ccs} Supply (Note 1)	V _{ccf} , V _{ccs}	−0.3	+4.0	V
RESET (Note 2)	V _{IN}	−0.5	+ 13.0	V
$\overline{\text{WP/ACC}}$ (Note 3)	V _{IN}	−0.5	+10.5	V

- Notes:**
1. Minimum DC voltage on input or I/O pins is −0.3 V. During voltage transitions, input or I/O pins may undershoot V_{ss} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{ccf} +0.4 V or V_{ccs}+0.4 V. During voltage transitions, input or I/O pins may overshoot to V_{ccf}+2.0 V or V_{ccs}+2.0 V for periods of up to 20 ns.
 2. Minimum DC input voltage on RESET pin is −0.5 V. During voltage transitions, RESET pins may undershoot V_{ss} to −2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-V_{ccf} or V_{ccs}) does not exceed 9.0 V. Maximum DC input voltage on RESET pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
 3. Minimum DC input voltage on $\overline{\text{WP/ACC}}$ pin is −0.5 V. During voltage transitions, $\overline{\text{WP/ACC}}$ pin may undershoot V_{ss} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP/ACC}}$ pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when V_{ccf} is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Ambient Temperature	T _A	−40	+85	°C
V _{ccf} /V _{ccs} Supply Voltages	V _{ccf} , V _{ccs}	+2.7	+3.3	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MB84VD2118XEM/MB84VD2119XEM-70

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
I _{LI}	Input Leakage Current	V _{IN} = V _{SS} to V _{CCf} , V _{CCS}			−1.0	—	+1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = V _{SS} to V _{CCf} , V _{CCS}			−1.0	—	+1.0	μA
I _{LIT}	$\overline{\text{RESET}}$ Inputs Leakage Current	V _{CCf} = V _{CCf} Max., V _{CCS} = V _{CCS} Max., RESET = 12.5V			—	—	35	μA
I _{CC1f}	Flash V _{CC} Active Current (Read) (Note 1)	$\overline{\text{CE}}_{\text{f}} = V_{\text{IL}}$, $\overline{\text{OE}} = V_{\text{IH}}$	t _{CYCLE} = 5 MHz	Byte	—	—	13	mA
			t _{CYCLE} = 5 MHz	Word	—	—	15	
			t _{CYCLE} = 1 MHz	Byte	—	—	7	mA
			t _{CYCLE} = 1 MHz	Word	—	—	7	
I _{CC2f}	Flash V _{CC} Active Current (Program/Erase) (Note 2)	$\overline{\text{CE}}_{\text{f}} = V_{\text{IL}}$, $\overline{\text{OE}} = V_{\text{IH}}$			—	—	35	mA
I _{CC3f}	Flash V _{CC} Active Current (Read-While-Program) (Note 5)	$\overline{\text{CE}}_{\text{f}} = V_{\text{IL}}$, $\overline{\text{OE}} = V_{\text{IH}}$	Byte	—	—	48	mA	
			Word	—	—	50		
I _{CC4f}	Flash V _{CC} Active Current (Read-While-Erase) (Note 5)	$\overline{\text{CE}}_{\text{f}} = V_{\text{IL}}$, $\overline{\text{OE}} = V_{\text{IH}}$	Byte	—	—	48	mA	
			Word	—	—	50		
I _{CC5f}	Flash V _{CC} Active Current (Erase-Suspend-Program)	$\overline{\text{CE}}_{\text{f}} = V_{\text{IL}}$, $\overline{\text{OE}} = V_{\text{IH}}$			—	—	35	mA
I _{LIA}	ACC Input Leakage Current	V _{CCf} = V _{CCf} Max., V _{CCS} = V _{CCS} Max., WP/ACC = V _{ACC} Max			—	—	20	mA
I _{CC1S}	SRAM V _{CC} Active Current	V _{CCS} = V _{CCS} Max., CE1s = V _{IL} , CE2s = V _{IH}	t _{CYCLE} =10 MHz		—	—	40	mA
I _{CC2S}	SRAM V _{CC} Active Current	$\overline{\text{CE}}_{1\text{s}} = 0.2 \text{ V}$, CE2s = V _{CCS} − 0.2 V	t _{CYCLE} = 10 MHz		—	—	40	mA
			t _{CYCLE} = 1 MHz		—	—	8	mA
I _{SB1f}	Flash V _{CC} Standby Current	V _{CCf} = V _{CCf} Max., $\overline{\text{CE}}_{\text{f}} = V_{\text{CCf}} \pm 0.3 \text{ V}$ RESET = V _{CCf} ± 0.3 V, WP/ACC = V _{CCf} ± 0.3 V			—	1	5	μA
I _{SB2f}	Flash V _{CC} Standby Current (RESET)	V _{CCf} = V _{CCf} Max., $\overline{\text{RESET}} = V_{\text{SS}} \pm 0.3 \text{ V}$, WP/ACC = V _{CCf} ± 0.3 V			—	1	5	μA
I _{SB3f}	Flash V _{CC} Current (Automatic Sleep Mode) (Note 3)	V _{CCf} = V _{CCf} Max., $\overline{\text{CE}}_{\text{f}} = V_{\text{SS}} \pm 0.3 \text{ V}$ RESET = V _{CCf} ± 0.3 V, WP/ACC = V _{CCf} ± 0.3 V V _{IN} = V _{CCf} ± 0.3 V or V _{SS} ± 0.3 V			—	1	5	μA
I _{SB1S}	SRAM V _{CC} Standby Current	$\overline{\text{CE}}_{1\text{s}} \geq V_{\text{CCS}} - 0.2 \text{ V}$, CE2s ≥ V _{CCS} − 0.2 V LB = UB ≥ V _{CCS} −0.2 V or ≤ 0.2V			—	—	15	μA
I _{SB2S}	SRAM V _{CC} Standby Current	$\overline{\text{CE}}_{1\text{s}} \geq V_{\text{CCS}} - 0.2 \text{ V}$ or ≤ 0.2V, CE2s ≤ 0.2 V LB = UB ≥ V _{CCS} −0.2 V or ≤ 0.2V			—	—	15	μA

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Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V _{IL}	Input Low Level	—	−0.3	—	0.5	V
V _{IH}	Input High Level	—	2.4	—	V _{CC} +0.3*	V
V _{ID}	Voltage for Sector Protection, and Temporary Sector Unprotection (<u>RESET</u>) (Note 4)	—	11.5	—	12.5	V
V _{ACC}	Voltage for Program Acceleration (<u>WP/ACC</u>) (Note4)	—	8.5	9.0	9.5	V
V _{OL}	SRAM Output Low Level	V _{CCS} = V _{CCS} Min., I _{OL} =4.0 mA	—	—	0.45	V
V _{OH}	SRAM Output High Level	V _{CCS} = V _{CCS} Min., I _{OH} =−0.5 mA	2.4	—	—	V
V _{OL}	Flash Output Low Level	V _{CCf} = V _{CCf} Min., I _{OL} =4.0 mA	—	—	0.4	V
V _{OH}	Flash Output High Level	V _{CCf} = V _{CCf} Min., I _{OH} =−0.5 mA	2.4	—	—	V
V _{LKO}	Flash Low V _{CCf} Lock-Out Voltage	—	2.3	—	2.5	V

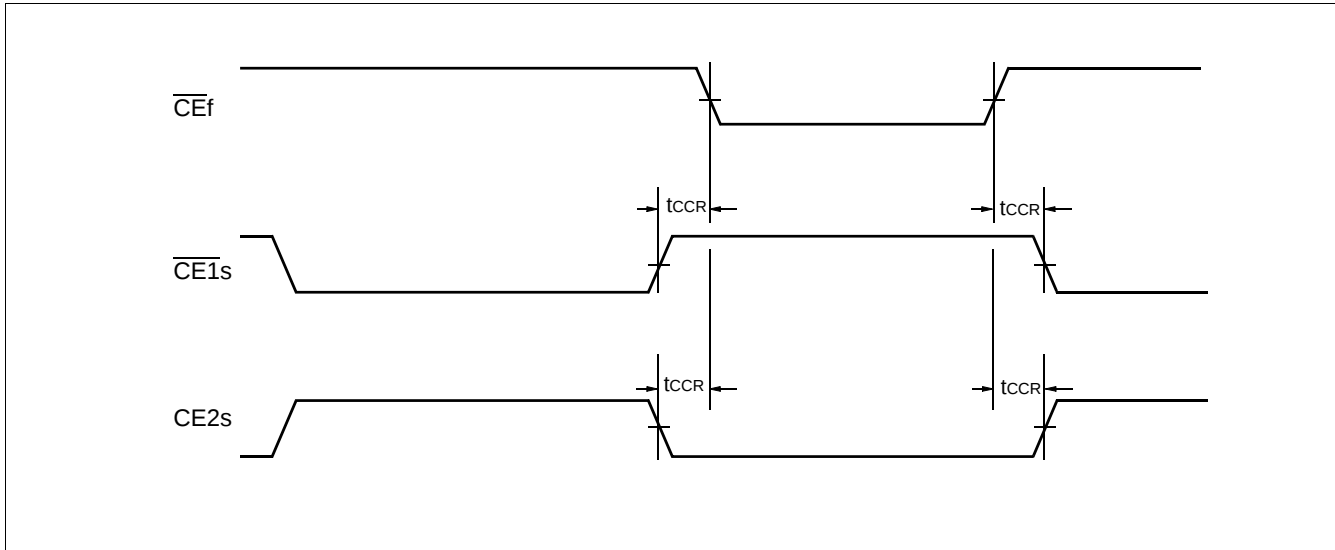
- Notes:**
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
 2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
 3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
 4. Applicable for only V_{CCf} applying.
 5. Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

2. AC Characteristics

- $\overline{CE}$ Timing

Parameter Symbols		Description	Test Setup		Value	Unit
JEDEC	Standard					
—	t_{CCR}	$\overline{CE}$ Recover Time	—	Min.	0	ns

- Timing Diagram for alternating SRAM to Flash

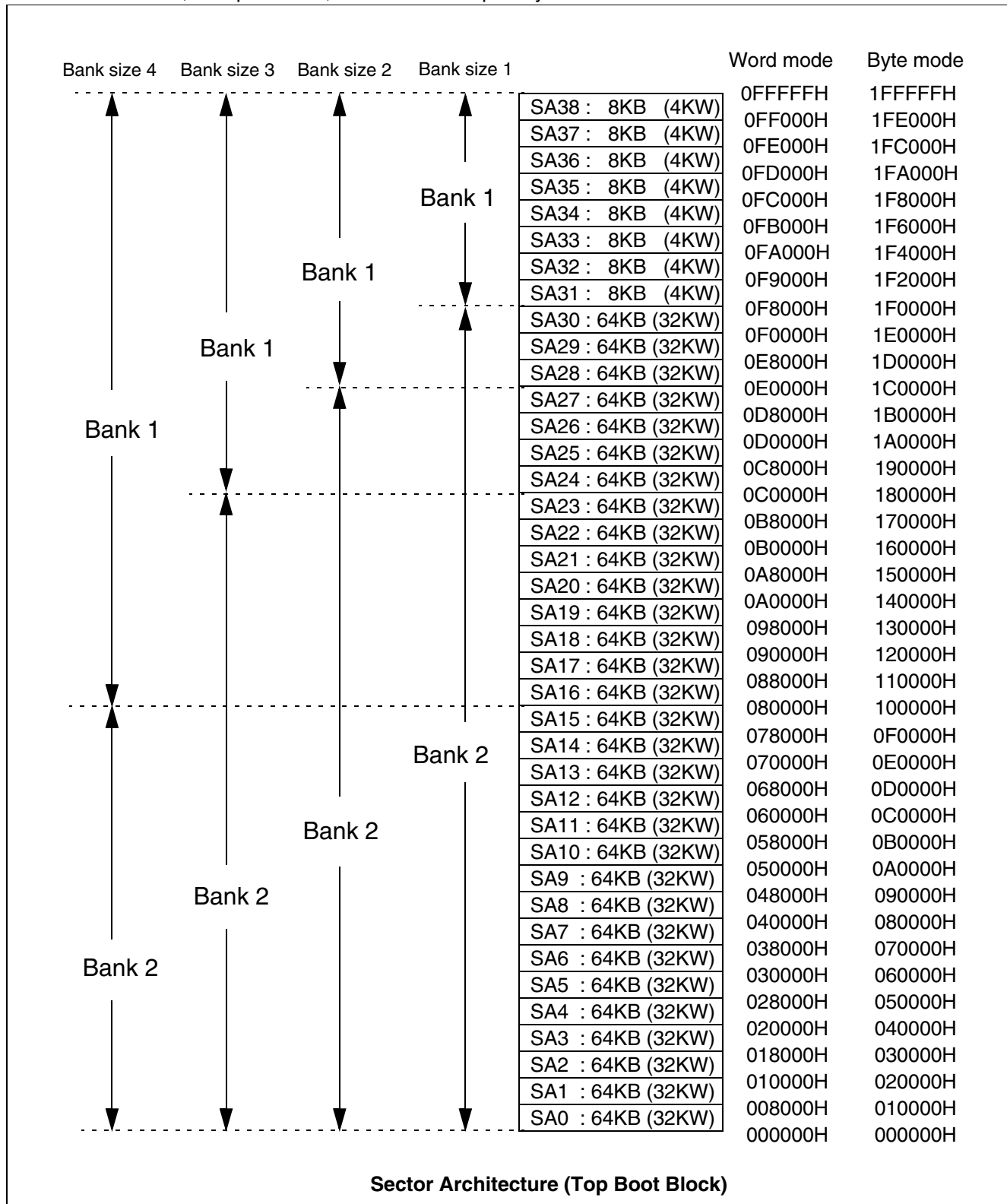


- **Flash Characteristics**
Please refer to “16M Flash Memory for MCP” part.
- **SRAM Characteristics,**
Please refer to “4M SRAM for MCP” part.

16M Flash for MCP

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

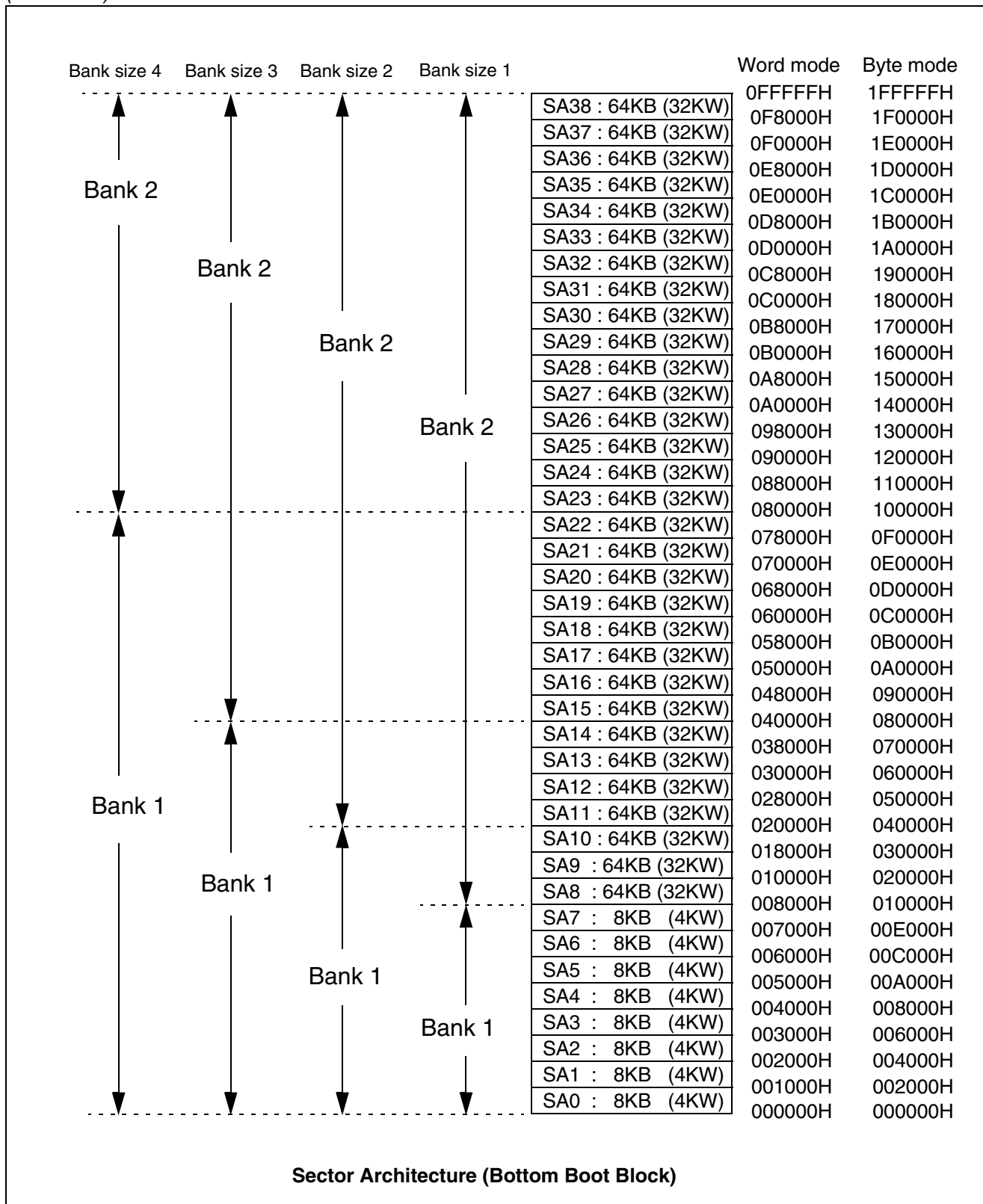
- Eight 4 K words, and thirty one 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



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16M Flash for MCP

(Continued)



16M Flash for MCP

Sector Address Tables (Top Boot Block, Bank Size=1)

Bank	Sector	Sector Address								Address Range (Byte mode)	Address Range (Word mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
Bank 1	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

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Sector Address Tables (Bottom Boot Block, Bank Size=1)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFFH	000000H to 000FFFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFFH	001000H to 001FFFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFFH	002000H to 002FFFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFFH	003000H to 003FFFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFFH	004000H to 004FFFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFFH	005000H to 005FFFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFFH	006000H to 006FFFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFFFH	007000H to 007FFFFH
Bank 2	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFFFH
	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFFFH
	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFFH
	SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFFH	078000H to 07FFFFFFH
	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFFH
SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH	

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Sector Address Tables (Top Boot Block, Bank Size=2)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
Bank 1	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

16M Flash for MCP

Sector Address Tables (Bottom Boot Block, Bank Size=2)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFFH	000000H to 000FFFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFFH	001000H to 001FFFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFFH	002000H to 002FFFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFFH	003000H to 003FFFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFFH	004000H to 004FFFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFFH	005000H to 005FFFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFFH	006000H to 006FFFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFFFH	007000H to 007FFFFH
	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFFFH	008000H to 00FFFFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFFFH	010000H to 017FFFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFFFH	018000H to 01FFFFFFH
Bank 2	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFFFH	020000H to 027FFFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFFFH	028000H to 02FFFFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFFFH	030000H to 037FFFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFFFH	038000H to 03FFFFFFH
	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFFFH	040000H to 047FFFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFFFH	048000H to 04FFFFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFFFH	050000H to 057FFFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFFFH	058000H to 05FFFFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFFFH	060000H to 067FFFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFFFH	068000H to 06FFFFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFFFH	070000H to 077FFFFH
	SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFFH	078000H to 07FFFFFFH
	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFFFH	080000H to 087FFFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFFFH	088000H to 08FFFFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFFFH	090000H to 097FFFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFFFH	098000H to 09FFFFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFFFH	0A0000H to 0A7FFFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFFFH	0A8000H to 0AFFFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFFFH	0B0000H to 0B7FFFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFFFH	0B8000H to 0BFFFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFFFH	0C0000H to 0C7FFFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFFFH	0C8000H to 0CFFFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFFFH	0D0000H to 0D7FFFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFFFH	0D8000H to 0DFFFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFFFH	0E0000H to 0E7FFFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFFFH	0E8000H to 0EFFFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFFFH	0F0000H to 0F7FFFFH
	SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH

16M Flash for MCP

Sector Address Tables (Top Boot Block, Bank Size=3)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
Bank 1	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

16M Flash for MCP

Sector Address Tables (Bottom Boot Block, Bank Size=3)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFFH	000000H to 000FFFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFFH	001000H to 001FFFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFFH	002000H to 002FFFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFFH	003000H to 003FFFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFFH	004000H to 004FFFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFFH	005000H to 005FFFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFFH	006000H to 006FFFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFFFH	007000H to 007FFFFH
	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFFFH	008000H to 00FFFFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFFFH	010000H to 017FFFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFFFH	018000H to 01FFFFFFH
	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFFFH	020000H to 027FFFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFFFH	028000H to 02FFFFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFFFH	030000H to 037FFFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFFFH	038000H to 03FFFFFFH
Bank 2	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFFFH	040000H to 047FFFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFFFH	048000H to 04FFFFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFFFH	050000H to 057FFFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFFFH	058000H to 05FFFFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFFFH	060000H to 067FFFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFFFH	068000H to 06FFFFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFFFH	070000H to 077FFFFH
	SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFFH	078000H to 07FFFFFFH
	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFFFH	080000H to 087FFFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFFFH	088000H to 08FFFFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFFFH	090000H to 097FFFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFFFH	098000H to 09FFFFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFFFH	0A0000H to 0A7FFFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFFFH	0A8000H to 0AFFFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFFFH	0B0000H to 0B7FFFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFFFH	0B8000H to 0BFFFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFFFH	0C0000H to 0C7FFFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFFFH	0C8000H to 0CFFFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFFFH	0D0000H to 0D7FFFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFFFH	0D8000H to 0DFFFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFFFH	0E0000H to 0E7FFFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFFFH	0E8000H to 0EFFFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFFFH	0F0000H to 0F7FFFFH
	SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH

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Sector Address Tables (Top Boot Block, Bank Size=4)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
Bank 1	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

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Sector Address Tables (Bottom Boot Block, Bank Size=4)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFFH	000000H to 000FFFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFFH	001000H to 001FFFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFFH	002000H to 002FFFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFFH	003000H to 003FFFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFFH	004000H to 004FFFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFFH	005000H to 005FFFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFFH	006000H to 006FFFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFFFH	007000H to 007FFFFH
	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFFFH	008000H to 00FFFFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFFFH	010000H to 017FFFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFFFH	018000H to 01FFFFFFH
	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFFFH	020000H to 027FFFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFFFH	028000H to 02FFFFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFFFH	030000H to 037FFFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFFFH	038000H to 03FFFFFFH
	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFFFH	040000H to 047FFFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFFFH	048000H to 04FFFFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFFFH	050000H to 057FFFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFFFH	058000H to 05FFFFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFFFH	060000H to 067FFFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFFFH	068000H to 06FFFFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFFFH	070000H to 077FFFFH
SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFFH	078000H to 07FFFFFFH	
Bank 2	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFFFH	080000H to 087FFFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFFFH	088000H to 08FFFFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFFFH	090000H to 097FFFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFFFH	098000H to 09FFFFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFFFH	0A0000H to 0A7FFFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFFFH	0A8000H to 0AFFFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFFFH	0B0000H to 0B7FFFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFFFH	0B8000H to 0BFFFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFFFH	0C0000H to 0C7FFFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFFFH	0C8000H to 0CFFFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFFFH	0D0000H to 0D7FFFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFFFH	0D8000H to 0DFFFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFFFH	0E0000H to 0E7FFFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFFFH	0E8000H to 0EFFFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFFFH	0F0000H to 0F7FFFFH
	SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFFH	0F8000H to 0FFFFFFH

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Sector Group Addresses (Top Boot Block)

Sector Group	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	1	X	X	X	SA1 to SA3
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA2	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	1	1	1	0	0	X	X	X	SA28 to SA30
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA9	1	1	1	1	1	0	0	0	SA31
SGA10	1	1	1	1	1	0	0	1	SA32
SGA11	1	1	1	1	1	0	1	0	SA33
SGA12	1	1	1	1	1	0	1	1	SA34
SGA13	1	1	1	1	1	1	0	0	SA35
SGA14	1	1	1	1	1	1	0	1	SA36
SGA15	1	1	1	1	1	1	1	0	SA37
SGA16	1	1	1	1	1	1	1	1	SA38

Sector Group Addresses (Bottom Boot Block)

Sector Group	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	Sectors
SGA0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	1	X	X	X	SA8 to SA10
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA9	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	1	1	1	0	0	X	X	X	SA35 to SA37
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA16	1	1	1	1	1	X	X	X	SA38

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Flash Memory Autoselect Codes

Type			A ₁₂ to A ₁₉	A ₆	A ₁	A ₀	A ₋₁ * ¹	Code (HEX)
Manufacturer's Code			X	V _{IL}	V _{IL}	V _{IL}	V _{IL}	04H
Device Code	Top Boot Block Bank Size=1	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	36H
		Word					X	2236H
	Bottom Boot Block Bank Size=1	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	39
		Word					X	2239H
	Top Boot Block Bank Size=2	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	2D
		Word					X	222DH
	Bottom Boot Block Bank Size=2	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	2E
		Word					X	222EH
	Top Boot Block Bank Size=3	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	28H
		Word					X	2228H
	Bottom Boot Block Bank Size=3	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	2BH
		Word					X	222BH
	Top Boot Block Bank Size=4	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	33H
		Word					X	2233H
	Bottom Boot Block Bank Size=4	Byte	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	35
		Word					X	2235H
Sector Group protect			Sector Group Address	V _{IL}	V _{IH}	V _{IL}	V _{IL}	01H* ²

*1: A₋₁ is for Byte mode.

*2: Output 01H at protected sector address and output 00H at unprotected sector address.

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Flash Memory Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset (Note 1)		1	XXHX	F0H	—	—	—	—	—	—	—	—	—	—
Read/Reset (Note 1)	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Autoselect	Word	3	555H	AAH	2AAH	55H	(BA) 555H	90H	—	—	—	—	—	—
	Byte		AAAH		555H		(BA) AAAH							
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H		SA	
Sector Erase Suspend		1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Sector Erase Resume		1	BA	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Fast Program (Note 2)	Word	2	XXHX	A0H	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXHX	A0H	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode (Note 2)	Word	2	BA	90H	XXHX	F0H (Note6)	—	—	—	—	—	—	—	—
	Byte		BA	90H	XXHX	F0H (Note6)	—	—	—	—	—	—	—	—
Extended Sector Group Protection (Note 3)	Word	4	XXHX	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
	Byte		XXHX	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
Query (Note 4)	Word	1	55H	98H	—	—	—	—	—	—	—	—	—	—
	Byte		AAH		—	—	—	—	—	—	—	—	—	—
Hi-ROM Entry	Word	3	555H	AAH	2AAH	55H	555H	88H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Hi-ROM Program (Note 5)	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Hi-ROM Erase (Note 5)	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	HRA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H		HRA	
Hi-ROM Exit (Note 5)	Word	4	555H	AAH	2AAH	55H	(HRBA) 555H	90H	XXHX	00H	—	—	—	—
	Byte		AAAH		555H		(HRBA) AAAH							

1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

2: This command is valid while Fast Mode.

3: This command is valid while $\overline{\text{RESET}} = V_{\text{ID}}$.

4: The valid Address is A_6 to A_0 .

5: This command is valid while Hi-ROM mode.

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6: The data "00H" is also acceptable.

Address bits A_{12} to $A_{19} = X = \text{"H" or "L"}$ for all address commands except for Program Address (PA), Sector Address (SA), and Bank Address (BA).

Bus operations are defined in Table 2 "User Bus Operations".

RA = Address of the memory location to be read.

PA = Address of the memory location to be programmed.

Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{19} , A_{18} , A_{17} , A_{16} , A_{15} , A_{14} , A_{13} , and A_{12} will uniquely select any sector.

BA = Bank address (A_{15} to A_{19})

SPA = Sector group address to be protected. Set sector group address (SGA) and $(A_6, A_1, A_0) = (0, 1, 0)$.

HRA = Address of the Hidden-ROM area.

Top Boot Block Word mode: 0F8000H to 0FFFFFFH

Byte mode: 1F0000H to 1FFFFFFH

Bottom Boot Block Word mode: 000000H to 007FFFFH

Byte mode: 000000H to 00FFFFFFH

HRBA = Bank address of the Hidden-ROM area.

Top Boot Block : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 1$

Bottom Boot Block : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 0$

RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA.

SD = Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

The system should generate the following address patterns;

Word mode: 555H or 2AAH to addresses A_{10} to A_0

Byte mode : AAH or 55H to addresses A_{10} to A_0 and A_{-1}

16M Flash for MCP

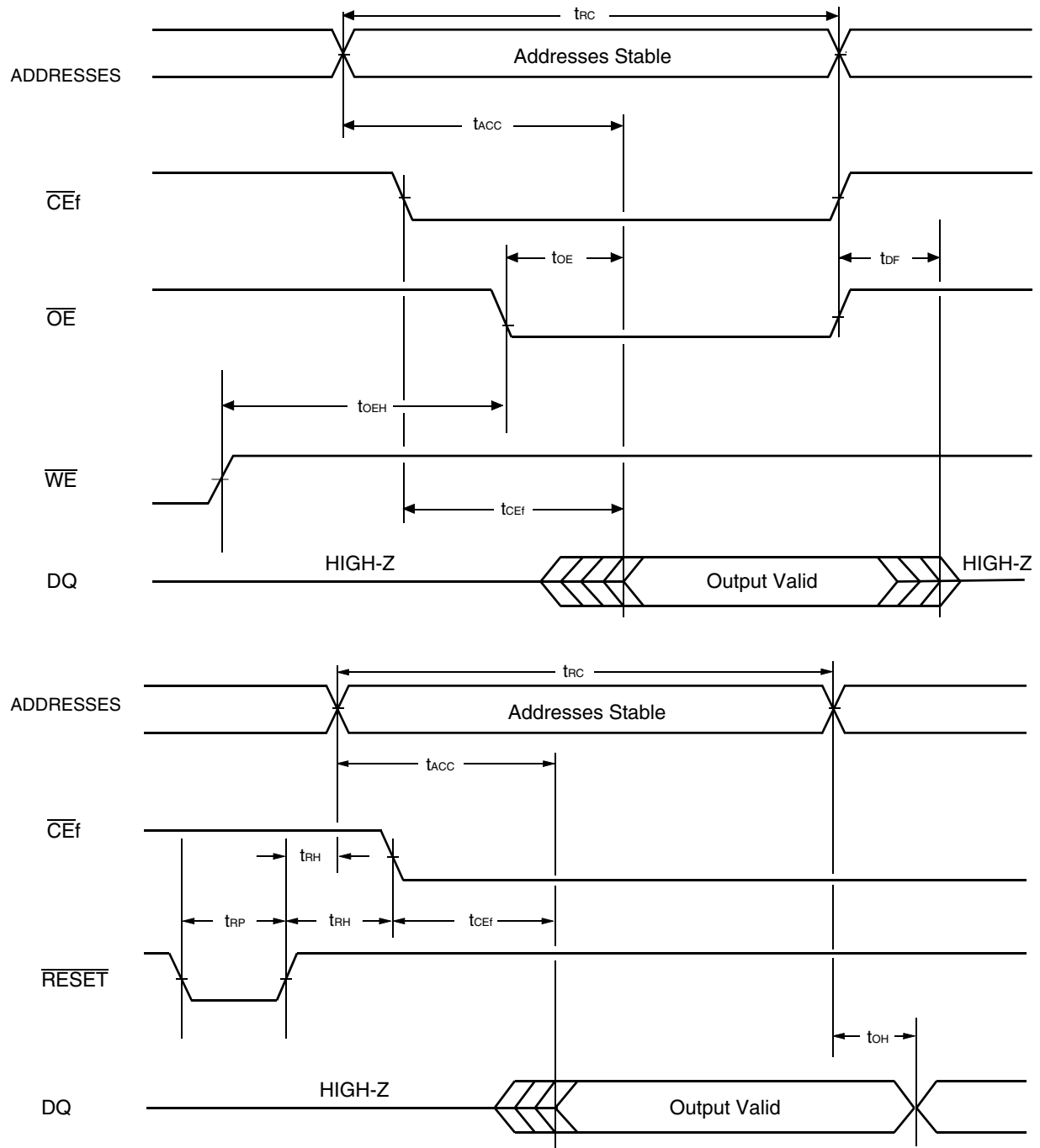
• Read Only Operations Characteristics (Flash)

Parameter Symbols		Description	Test Setup	Value (Note)		Unit
JEDEC	Standard			Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	—	70	—	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}_f = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	ns
t_{ELQV}	t_{CEf}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	—	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	—	25	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	—	25	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}_f$ or $\overline{OE}$, Whichever Occurs First	—	0	—	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	—	20	μs

Note: Test Conditions—Output Load: 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V to 3.0 V
 Timing measurement reference level
 Input: 1.5 V
 Output: 1.5 V

16M Flash for MCP

• Read Cycle (Flash)



16M Flash for MCP

• Erase/Program Operations (Flash)

Parameter Symbols		Description	Value			Unit
JEDEC	Standard		Min.	Typ.	Max.	
tAVAV	tWC	Write Cycle Time	70	—	—	ns
tAWL	tAS	Address Setup Time ($\overline{WE}$ to Addr.)	0	—	—	ns
—	tASO	Address Setup Time to $\overline{CEf}$ Low During Toggle Bit Polling	12	—	—	ns
tWLAX	tAH	Address Hold Time ($\overline{WE}$ to Addr.)	45	—	—	ns
—	tAHT	Address Hold Time from $\overline{CEf}$ or $\overline{OE}$ High During Toggle Bit Polling	0	—	—	ns
tDWH	tDS	Data Setup Time	30	—	—	ns
tWDH	tDH	Data Hold Time	0	—	—	ns
—	tOES	Output Enable Setup Time	0	—	—	ns
—	tOEH	Output Enable Hold Time	Read	0	—	ns
		Toggle and Data Polling	10	—	—	ns
—	tCEPH	$\overline{CEf}$ High During Toggle Bit Polling	20	—	—	ns
—	tOEPH	$\overline{OE}$ High During Toggle Bit Polling	20	—	—	ns
tGHEL	tGHEL	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CEf}$)	0	—	—	ns
tGHWL	tGHWL	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)	0	—	—	ns
tWLEL	tWS	$\overline{WE}$ Setup Time ($\overline{CEf}$ to $\overline{WE}$)	0	—	—	ns
tELWL	tCS	$\overline{CEf}$ Setup Time ($\overline{WE}$ to $\overline{CEf}$)	0	—	—	ns
tEHWL	tWH	$\overline{WE}$ Hold Time ($\overline{CEf}$ to $\overline{WE}$)	0	—	—	ns
tWHEH	tCH	$\overline{CEf}$ Hold Time ($\overline{WE}$ to $\overline{CEf}$)	0	—	—	ns
tWLWH	tWP	Write Pulse Width	35	—	—	ns
tELEH	tCP	$\overline{CEf}$ Pulse Width	35	—	—	ns
tWHWL	tWPH	Write Pulse Width High	25	—	—	ns
tEHEL	tCPH	$\overline{CEf}$ Pulse Width High	25	—	—	ns
tWHWH1	tWHWH1	Byte Programming Operation	—	8	—	μs
		Word Programming Operation	—	16	—	μs
tWHWH2	tWHWH2	Sector Erase Operation (Note 1)	—	1	—	sec
—	tVCS	V _{CCf} Setup Time	50	—	—	μs
—	tVLHT	Voltage Transition Time (Note 2)	4	—	—	μs
—	tVIDR	Rise Time to V _{ID} (Note 2)	500	—	—	ns
—	tVACCR	Rise Time to V _{ACC}	500	—	—	ns
—	tRB	Recover Time from RY/BY	0	—	—	ns
—	tRP	$\overline{RESET}$ Pulse Width	500	—	—	ns
—	tEOE	Delay Time from Embedded Output Enable	—	—	70	ns
—	tRH	$\overline{RESET}$ Hold Time Before Read	200	—	—	ns
—	tBUSY	Program/Erase Valid to RY/BY Delay	—	—	90	ns
—	tTOW	Erase Time-out Time (Note 3)	50	—	—	μs
—	tSPD	Erase Suspend Transition Time (Note 4)	—	—	20	μs

Notes: 1. This does not include the preprogramming time.

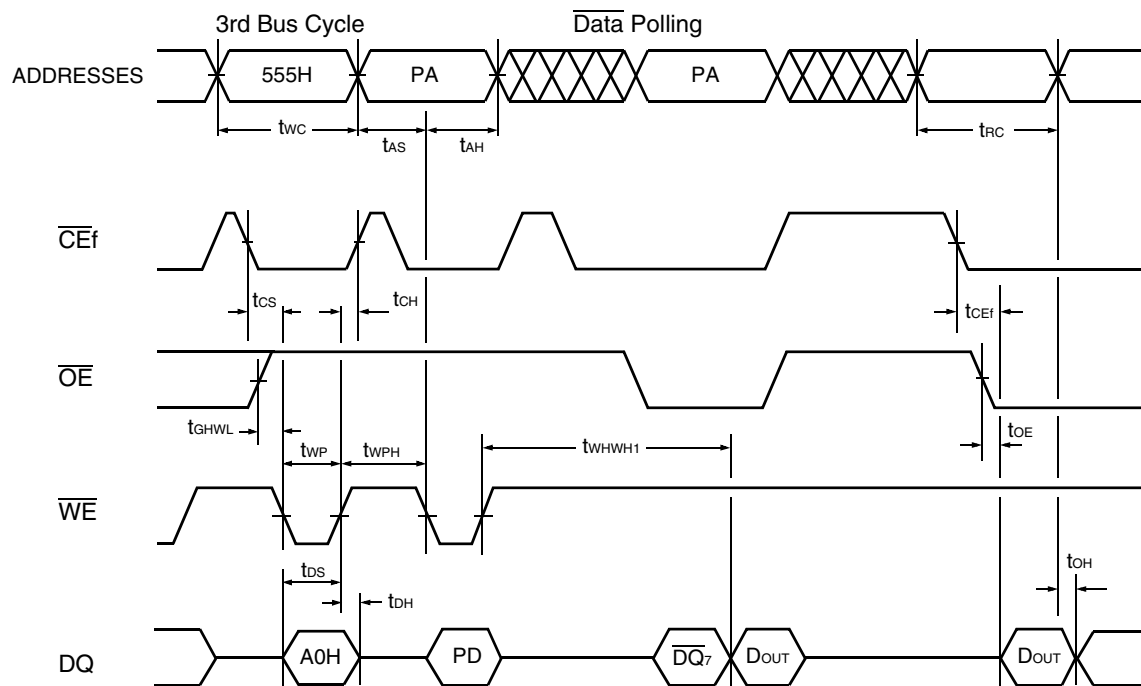
2. This timing is for Sector Protection Operation.

3. The time between writes must be less than "t_{TOW}" otherwise that command will not be accepted and erasure will start. A time-out or "t_{TOW}" from the rising edge of last $\overline{CEf}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s).

4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t_{SPD}" to suspend the erase operation.

16M Flash for MCP

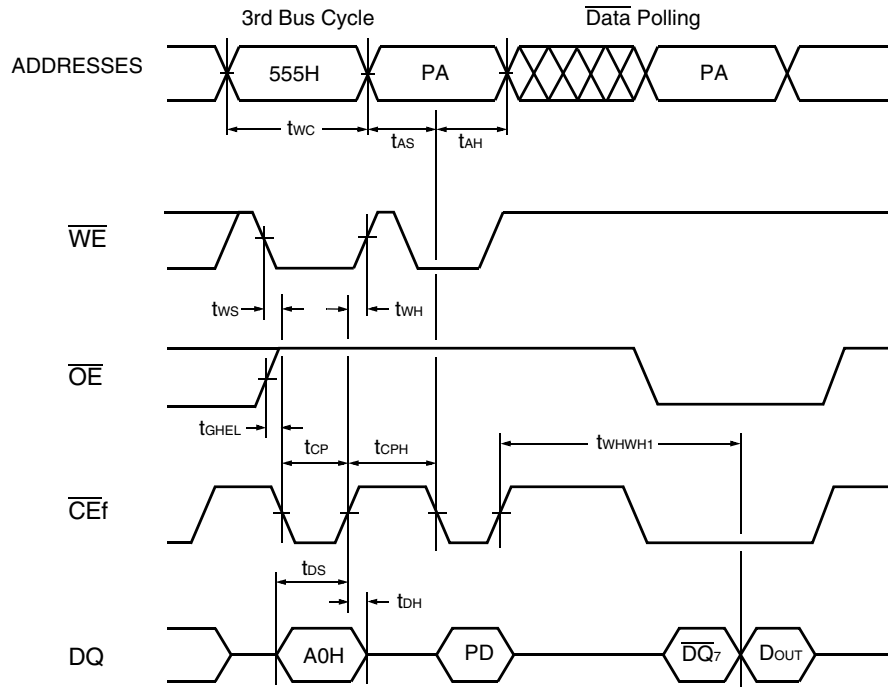
• Write Cycle ($\overline{WE}$ control) (Flash)



- Notes:
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

16M Flash for MCP

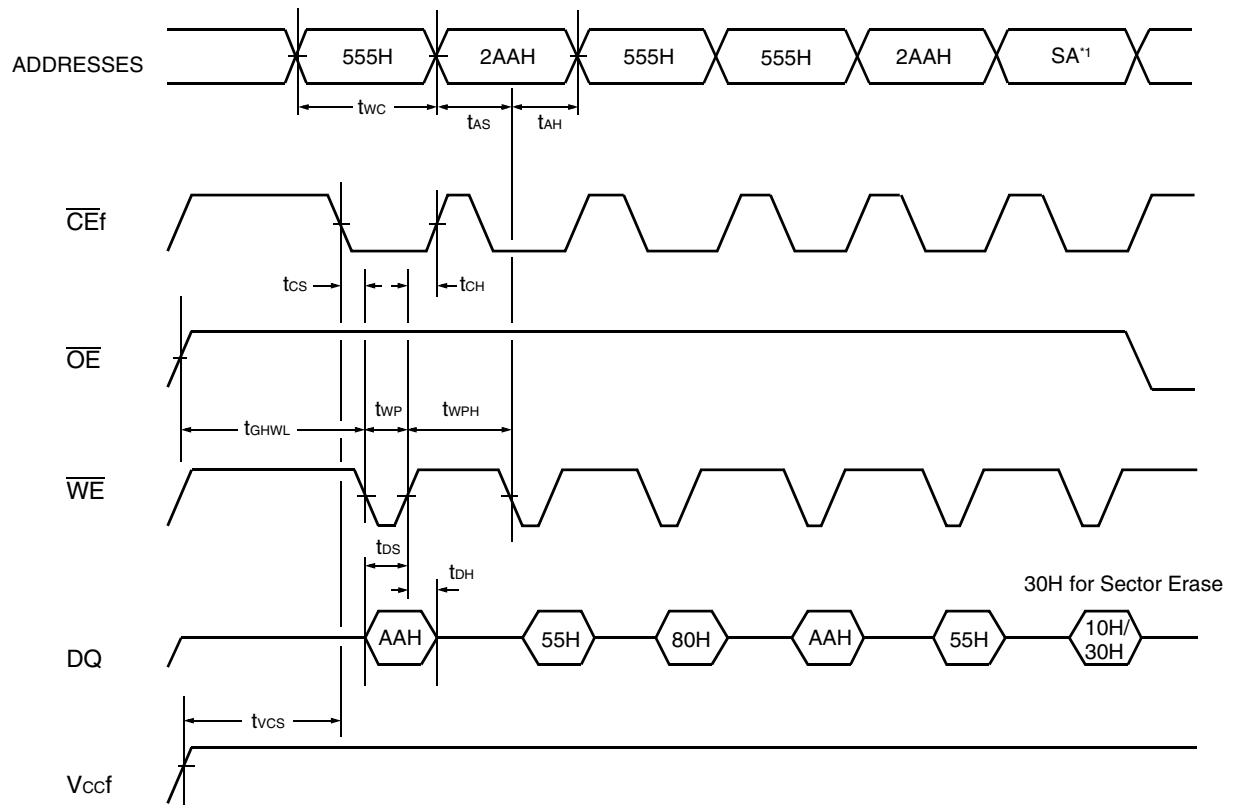
• Write Cycle ($\overline{\text{CEf}}$ control) (Flash)



- Notes:
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{\text{DQ}}_7$ is the output of the complement of the data written to the device.
 4. DOUT is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

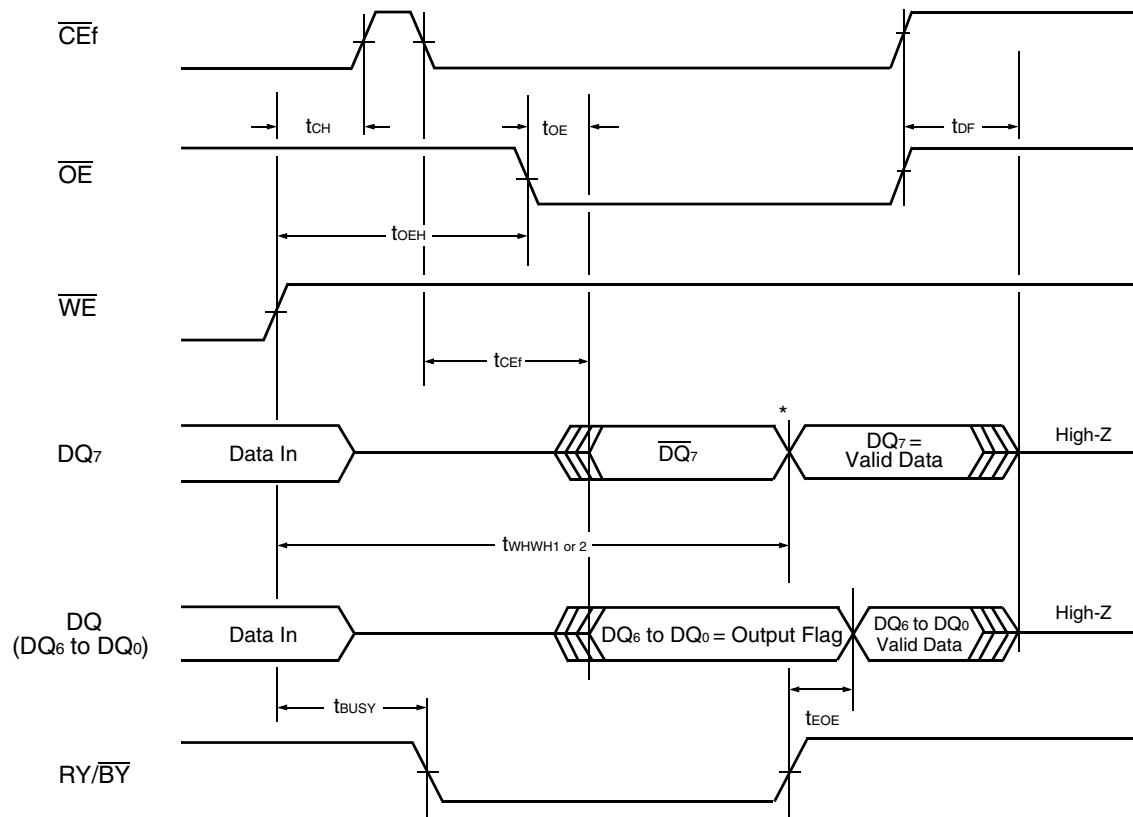
16M Flash for MCP

• AC Waveforms Chip/Sector Erase Operations (Flash)



16M Flash for MCP

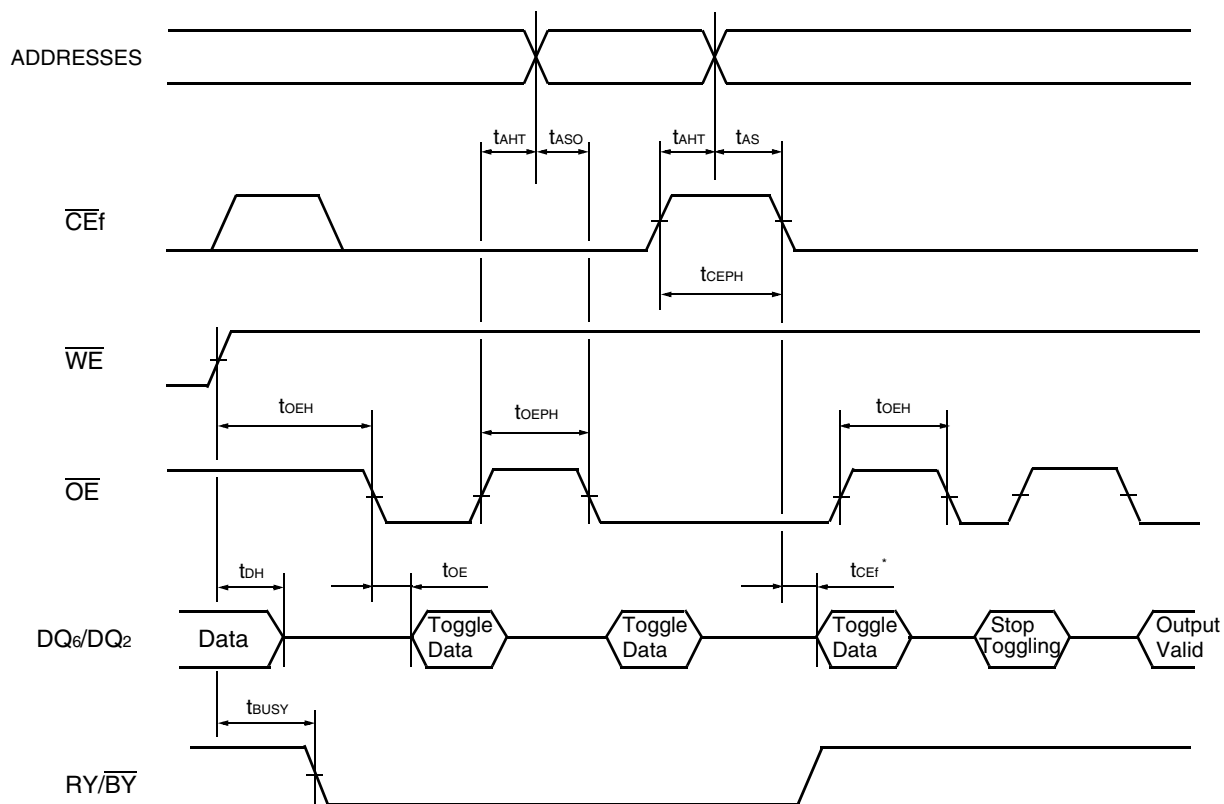
• AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)



* $\text{DQ}_7 = \text{Valid Data}$ (The device has completed the Embedded operation.)

16M Flash for MCP

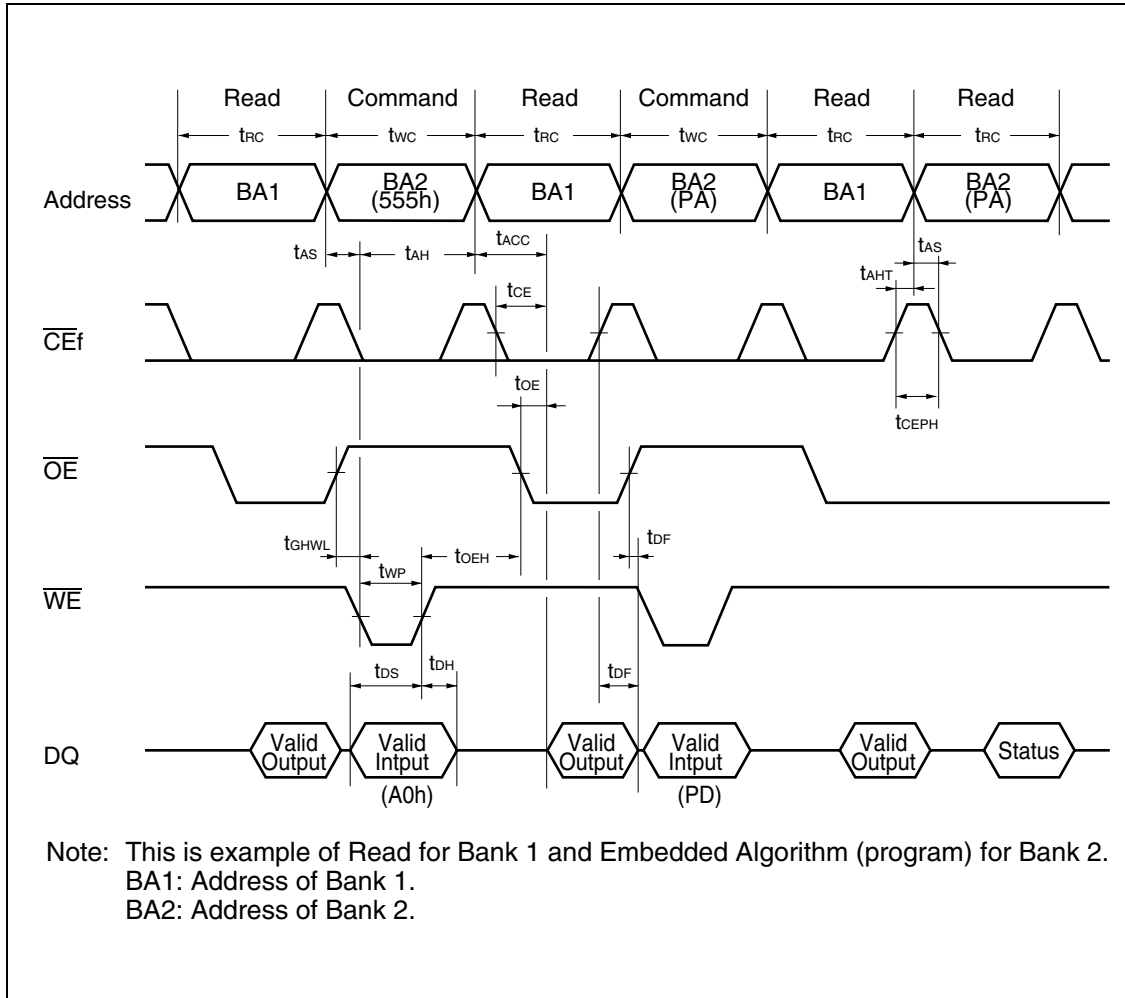
• AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)



* : DQ₆ stops toggling (The device has completed the Embedded operation).

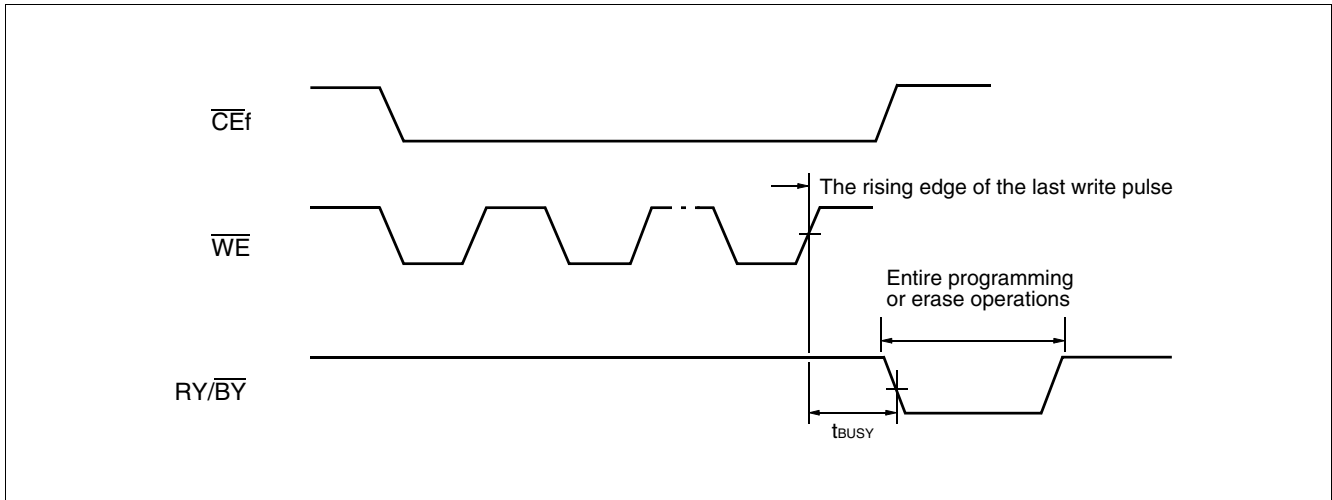
16M Flash for MCP

• Back-to-back Read/Write Timing Diagram (Flash)

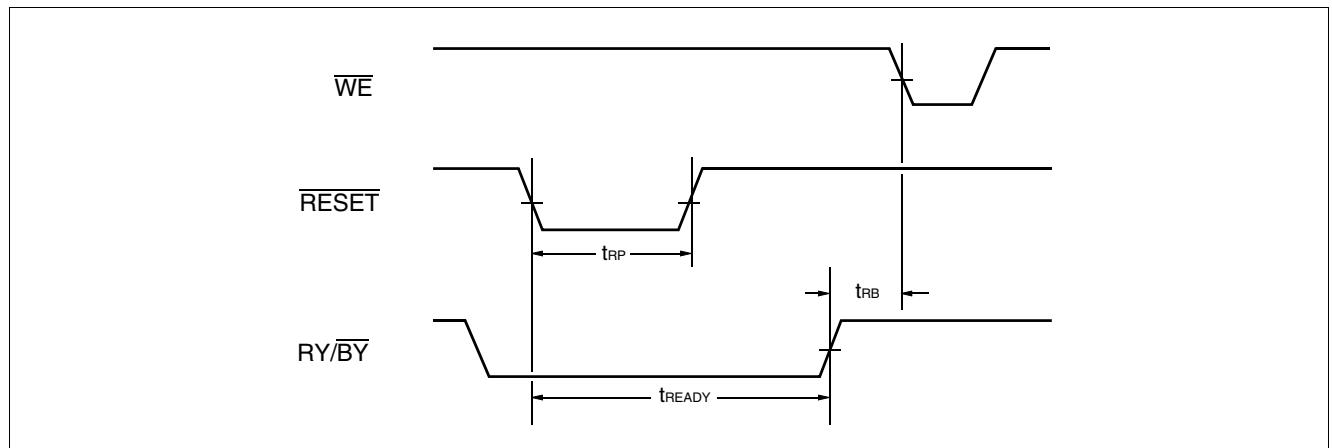


16M Flash for MCP

- **RY/ $\overline{\text{BY}}$ Timing Diagram during Write/Erase Operations (Flash)**

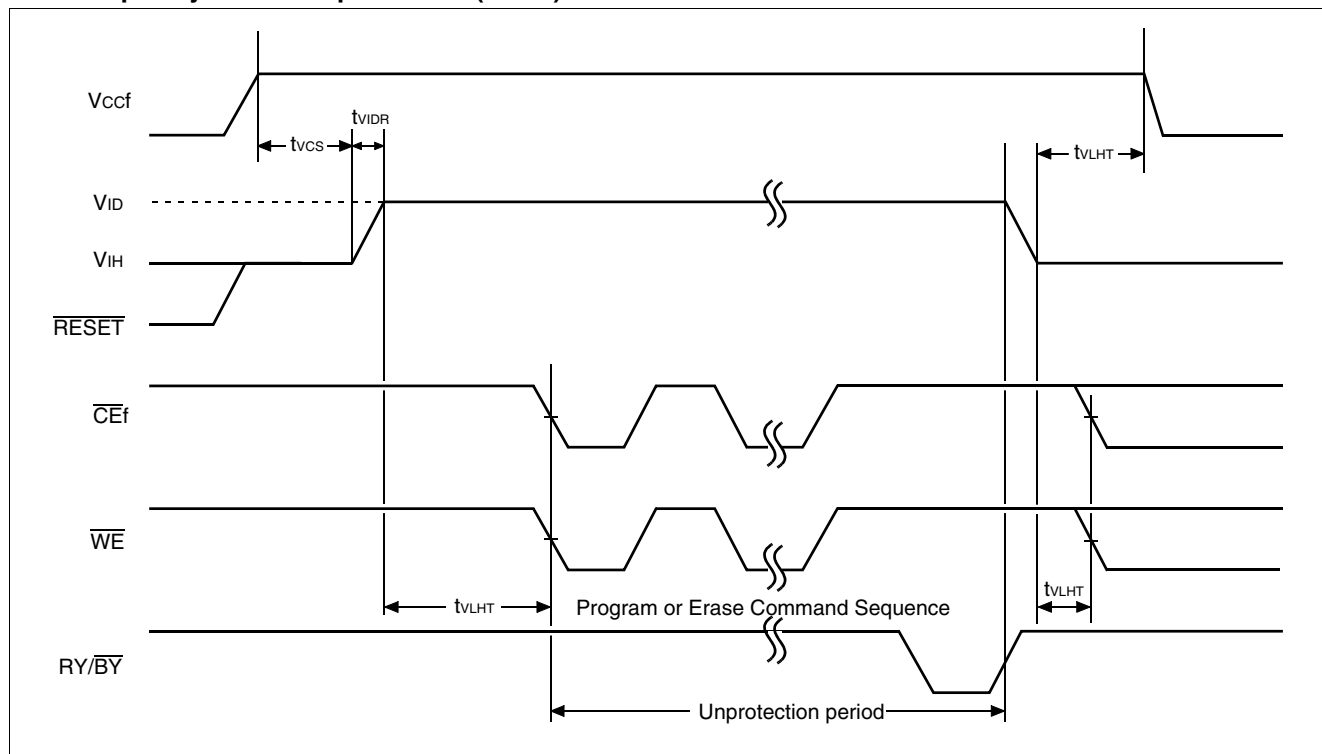


- **$\overline{\text{RESET}}$, $\text{RY}/\overline{\text{BY}}$ Timing Diagram (Flash)**

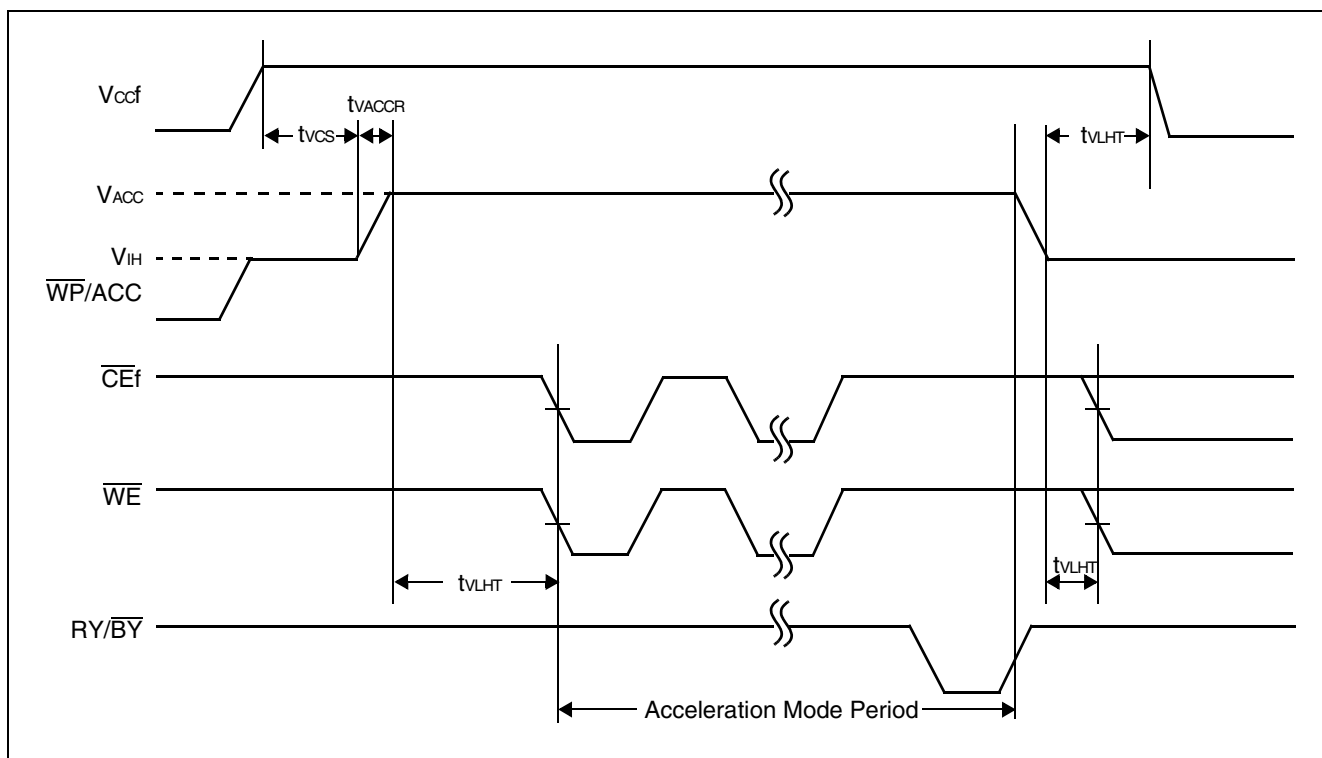


16M Flash for MCP

• Temporary Sector Unprotection (Flash)

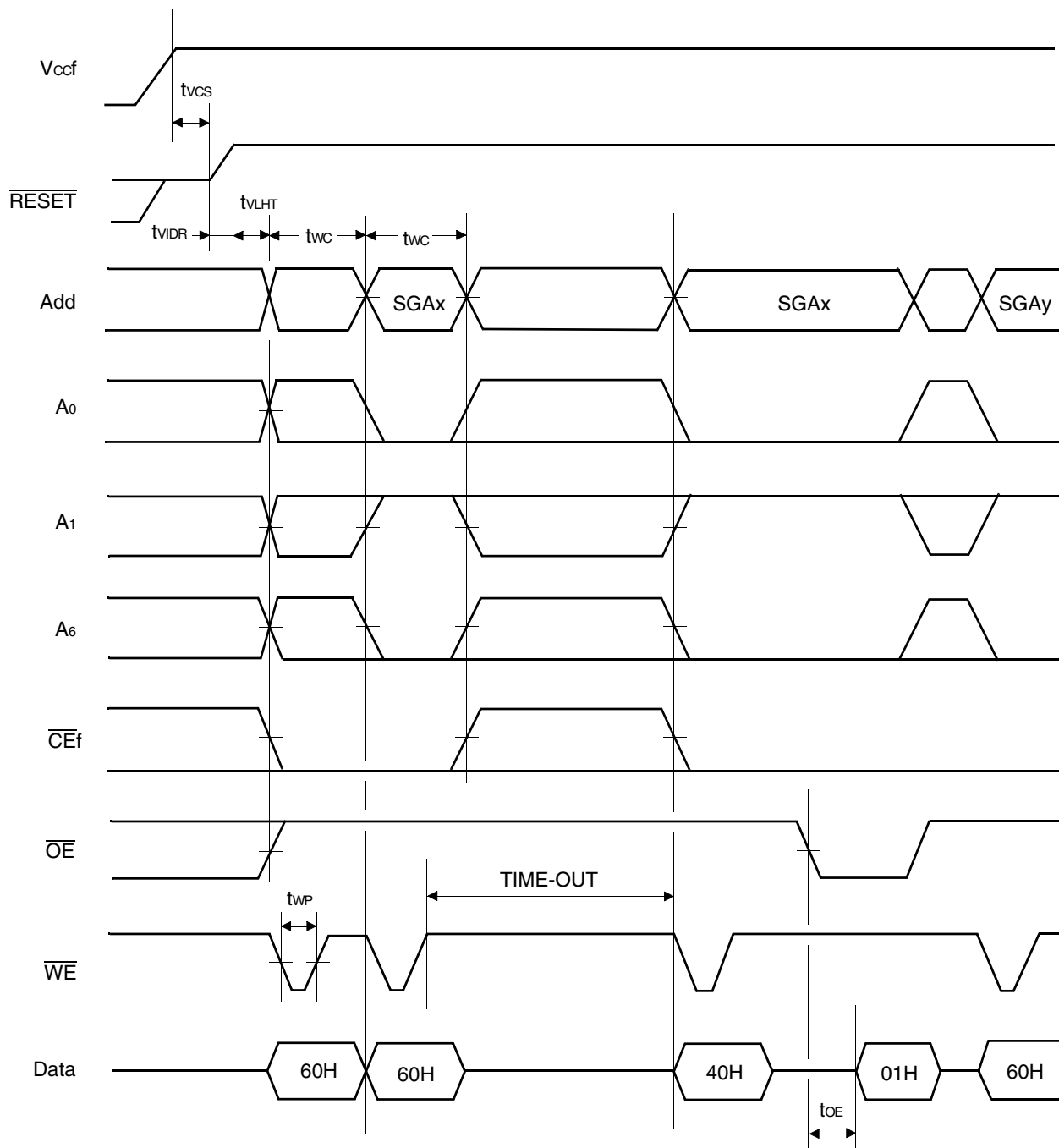


• Acceleration Mode Timing Diagram (Flash)



16M Flash for MCP

• Extended Sector Protection (Flash)



SGAx : Sector Group Address to be protected
 SGAy : Next Group Sector Address to be protected
 TIME-OUT : Time-Out window = 250 μ s (min)

16M Flash for MCP

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	sec	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	μs	Excludes system-level overhead
Word Programming Time	—	16	360	μs	Excludes system-level overhead
Chip Programming Time	—	—	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

4M SRAM for MCP

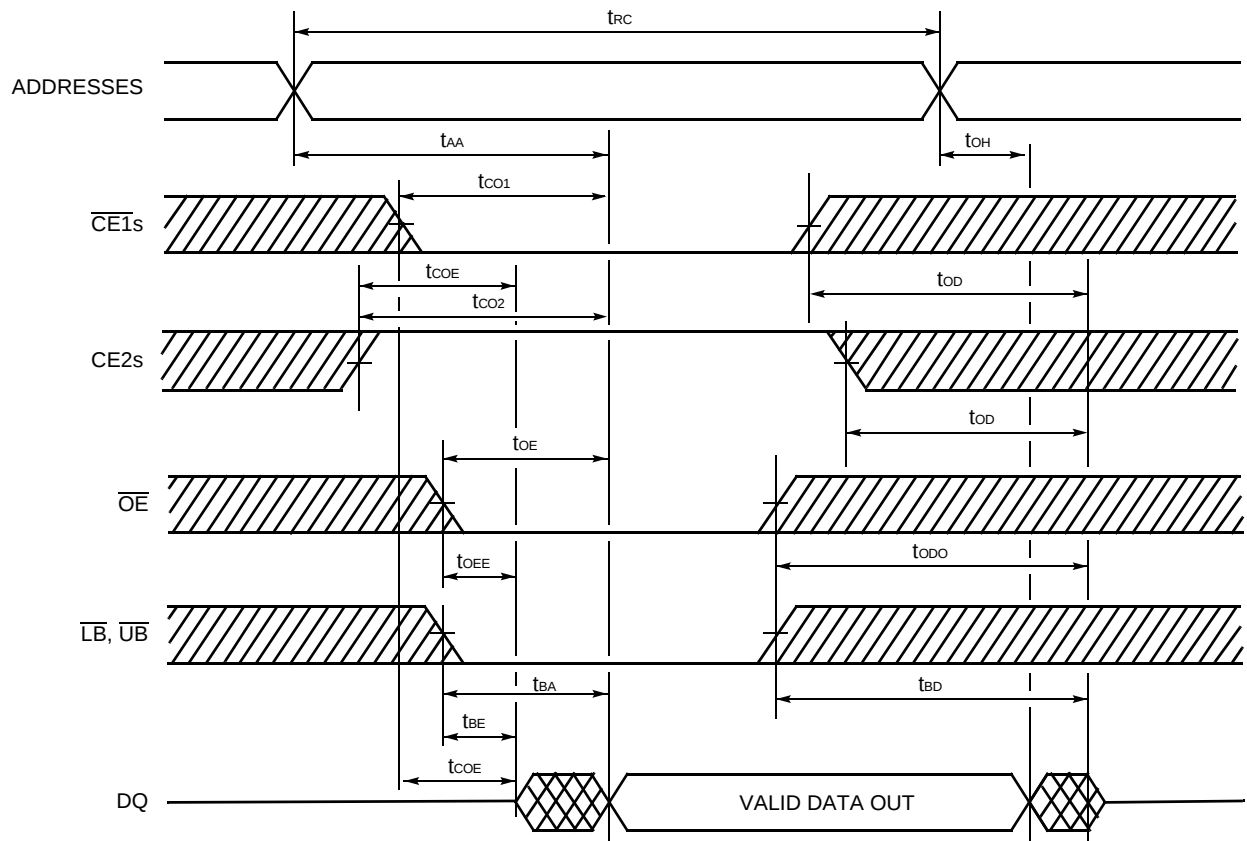
• Read Cycle (SRAM)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	70	—	ns
Address Access Time	t_{AA}	—	70	ns
Chip Enable ($\overline{CE1}$ s) Access Time	t_{CO1}	—	70	ns
Chip Enable (CE2s) Access Time	t_{CO2}	—	70	ns
Output Enable Access Time	t_{OE}	—	35	ns
$\overline{LB}$, $\overline{UB}$ to Output Valid	t_{BA}	—	70	ns
Chip Enable ($\overline{CE1}$ s Low and CE2s High) to Output Active	t_{COE}	5	—	ns
Output Enable Low to Output Active	t_{OEE}	0	—	ns
$\overline{UB}$, $\overline{LB}$ Enable Low to Output Active	t_{BE}	0	—	ns
Chip Enable ($\overline{CE1}$ s High or CE2s Low) to Output High-Z	t_{OD}	—	25	ns
Output Enable High to Output High-Z	t_{ODO}	—	25	ns
$\overline{UB}$, $\overline{LB}$ Output Enable to Output High-Z	t_{BD}	—	25	ns
Output Data Hold Time	t_{OH}	10	—	ns

Note: Test Conditions— Output Load: 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to V_{CCS}
Timing measurement reference level
Input: $0.5 \times V_{CCS}$
Output: $0.5 \times V_{CCS}$

4M SRAM for MCP

• Read Cycle (SRAM)



Note: $\overline{WE}$ remains HIGH for the read cycle.

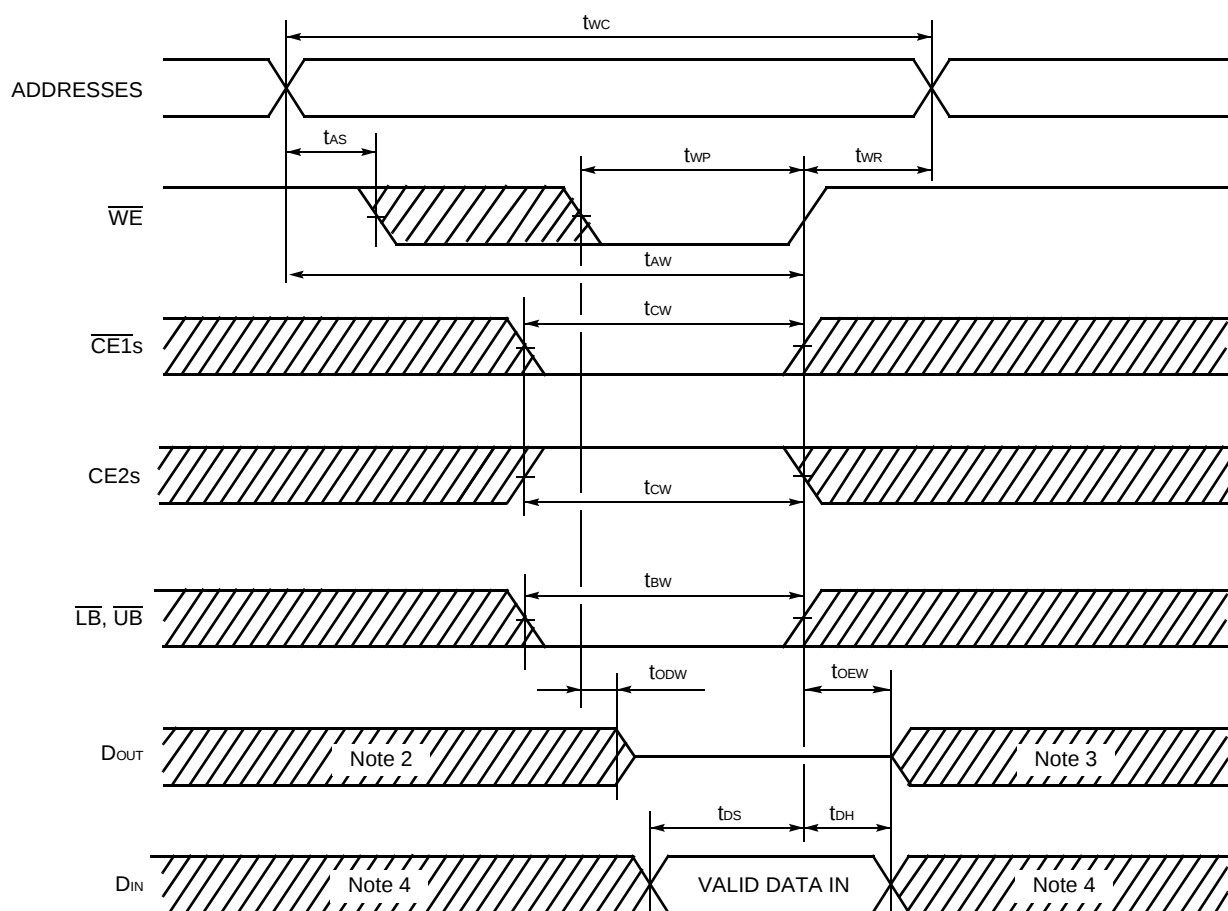
4M SRAM for MCP

• Write Cycle (SRAM)

Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	—	ns
Write Pulse Width	t_{WP}	50	—	ns
Chip Enable to End of Write	t_{CW}	55	—	ns
Address valid to End of Write	t_{AW}	55	—	ns
$\overline{UB}$, $\overline{LB}$ to End of Write	t_{BW}	55	—	ns
Address Setup Time	t_{AS}	0	—	ns
Write Recovery Time	t_{WR}	0	—	ns
$\overline{WE}$ Low to Output High-Z	t_{ODW}	—	25	ns
$\overline{WE}$ High to Output Active	t_{OEw}	0	—	ns
Data Setup Time	t_{DS}	30	—	ns
Data Hold Time	t_{DH}	0	—	ns

4M SRAM for MCP

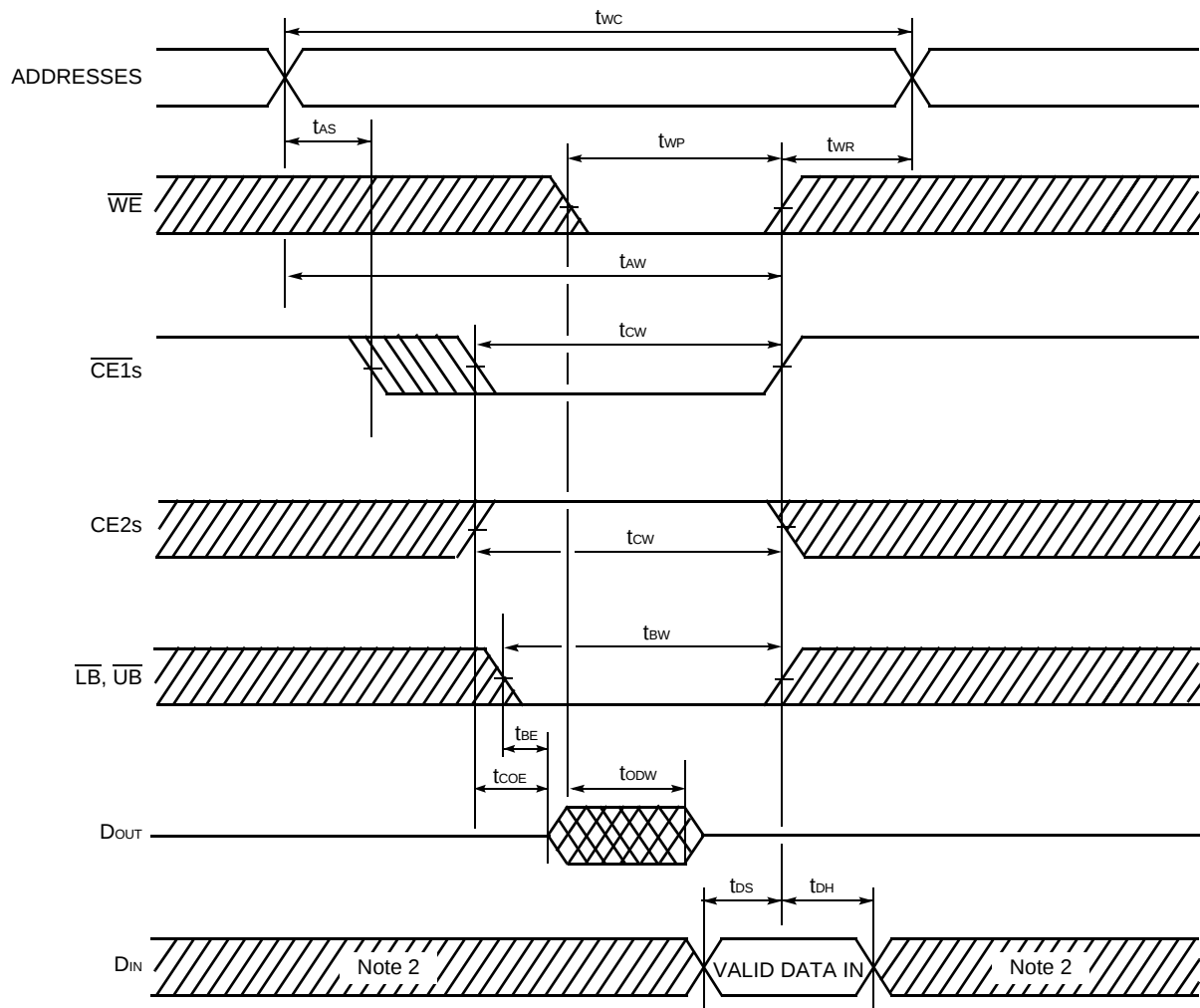
• Write Cycle (Note 1) ($\overline{WE}$ control) (SRAM)



- Note 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- Note 2. If $\overline{CE1s}$ goes LOW (or $\overline{CE2s}$ goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.
- Note 3. If $\overline{CE1s}$ goes HIGH (or $\overline{CE2s}$ goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
- Note 4. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

4M SRAM for MCP

• Write Cycle (Note 1) ($\overline{\text{CE1s}}$ control) (SRAM)

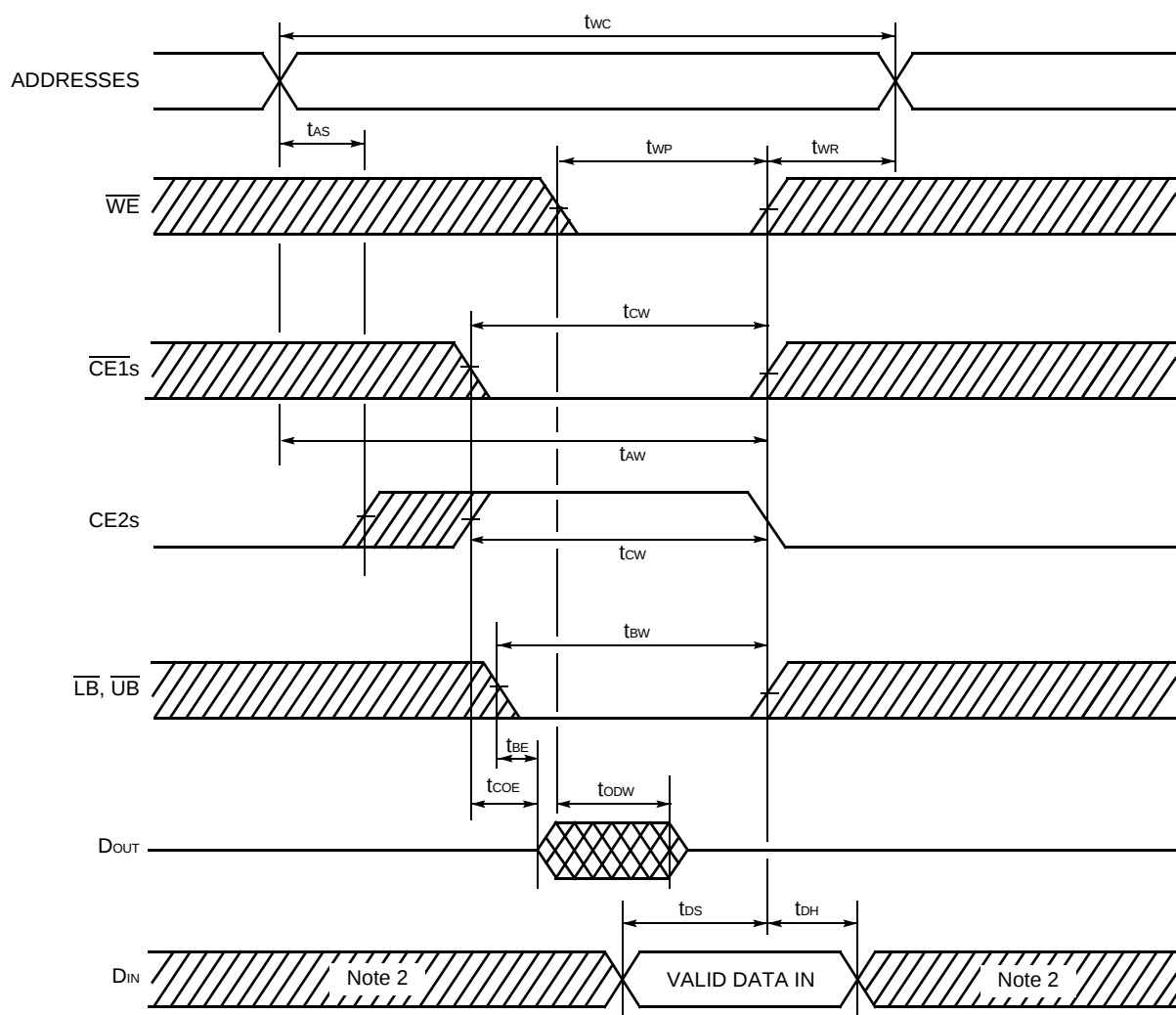


Notes: 1. If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.

2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

4M SRAM for MCP

• Write Cycle (Note 1) (CE2s Control) (SRAM)

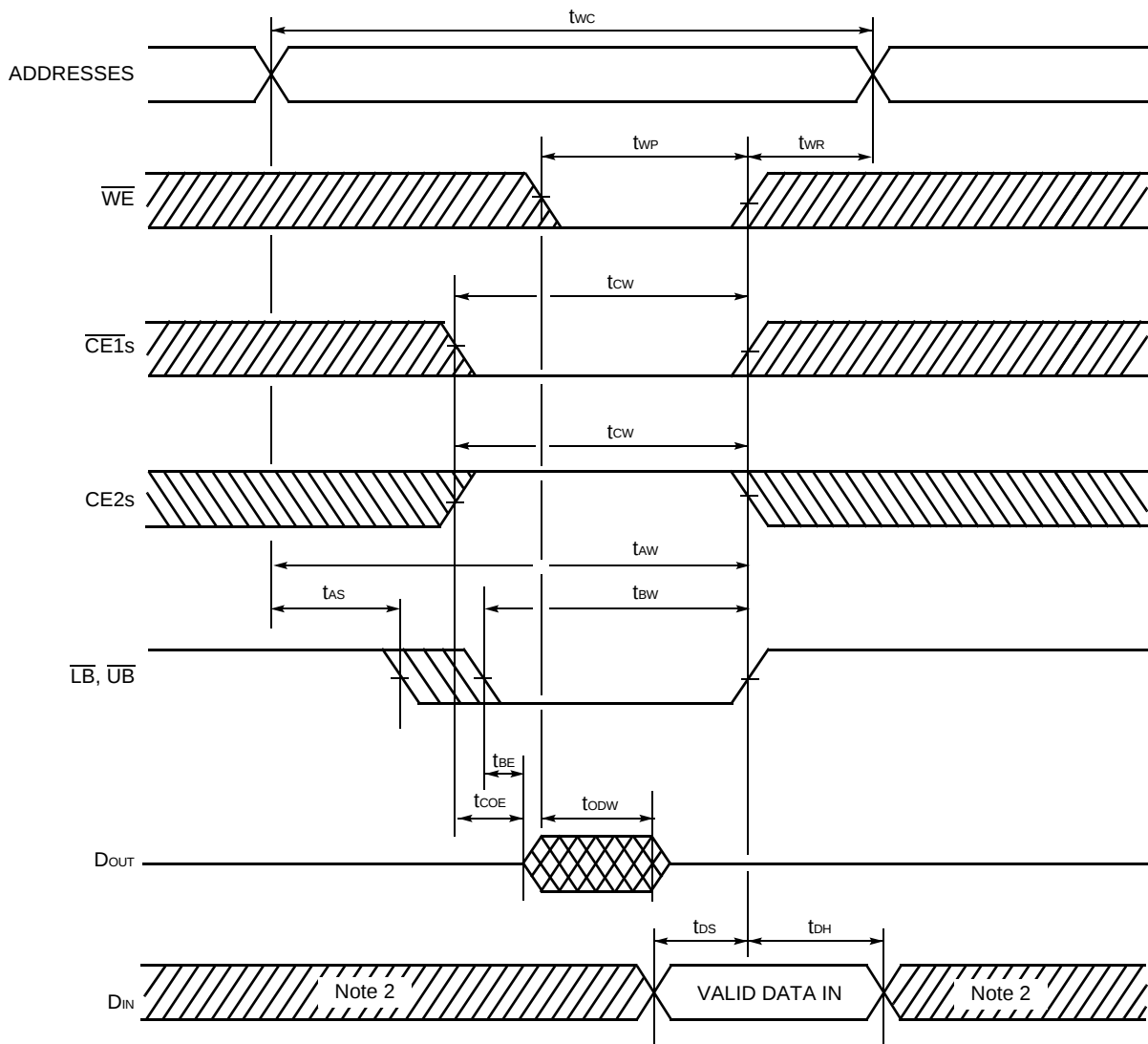


Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

4M SRAM for MCP

• Write Cycle (Note 1) ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Control) (SRAM)



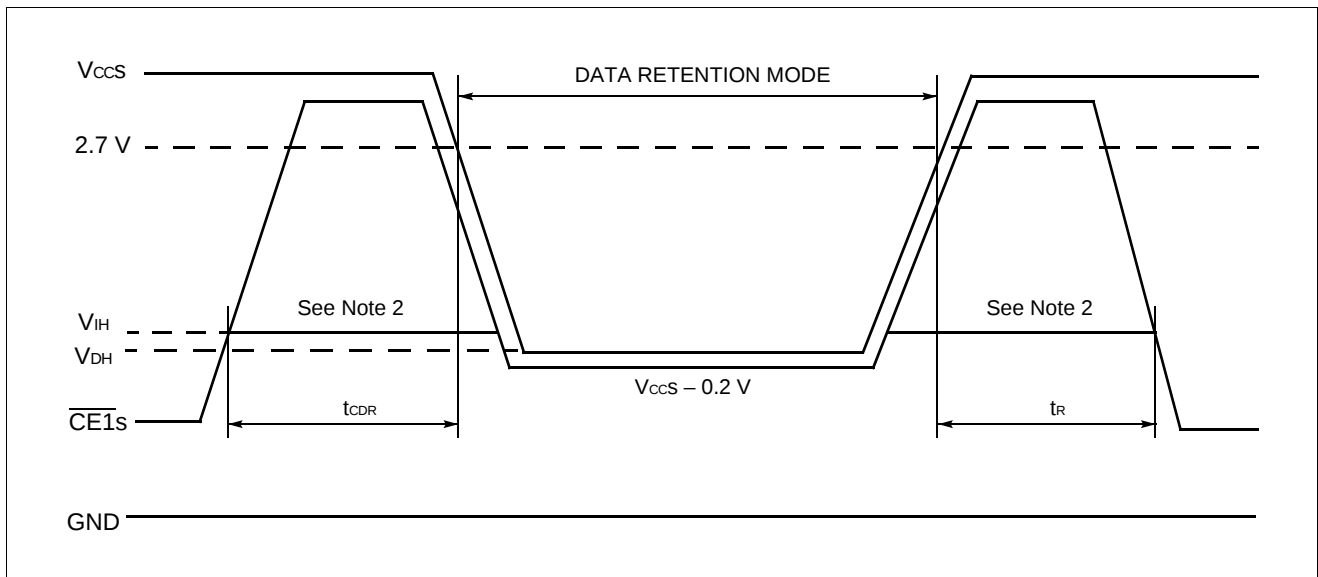
4M SRAM for MCP

■ DATA RETENTION CHARACTERISTICS (SRAM)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Data Retention Supply Voltage	V_{DH}	1.5	—	3.1	V
Standby Current	I_{DD2}	—	—	15	μA
Chip Deselect to Data Retention Mode Time	t_{CDR}	0	—	—	ns
Recovery Time	t_R	t_{RC}	—	—	ns

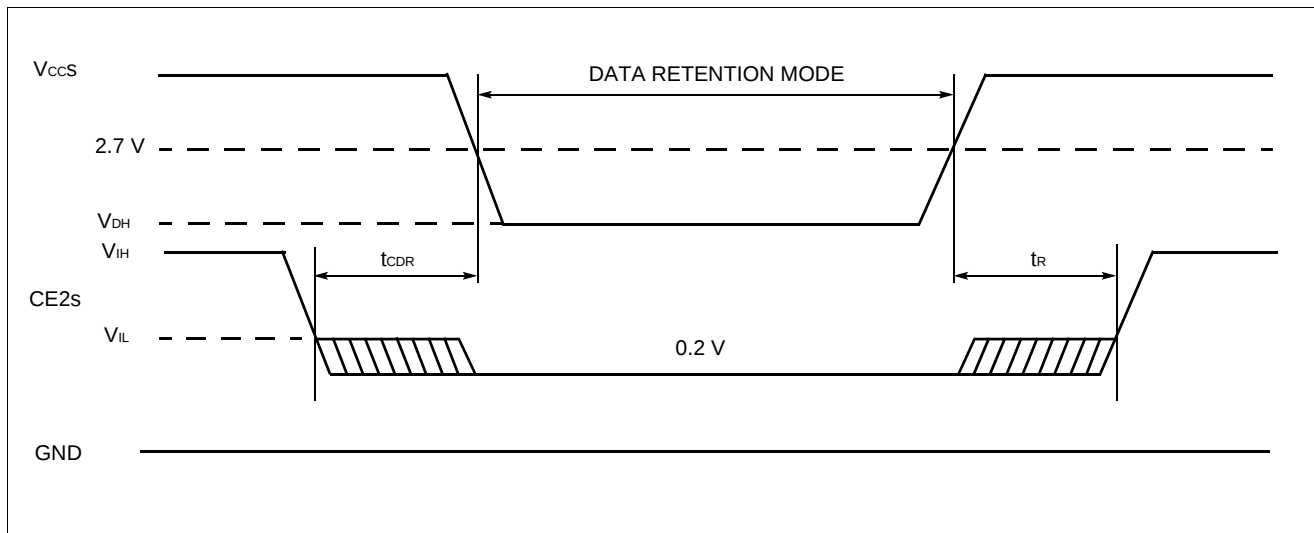
Note t_{RC} : Read cycle time

- $\overline{CE1}$ s Controlled Data Retention Mode (Note 1)



4M SRAM for MCP

• CE2s Controlled Data Retention Mode (Note 3)



- Notes:
1. In $\overline{CE1s}$ controlled data retention mode, input level of $CE2s$ should be fixed V_{CCS} to $V_{CCS}-0.2\text{ V}$ or V_{SS} to 0.2 V during data retention mode. Other input and input/output pins can be used between -0.3 V to $V_{CCS}+0.3\text{ V}$.
 2. When $\overline{CE1s}$ is operating at the V_{IH} Min. level, the standby current is given by I_{SB1S} during the transition of V_{CCS} from $V_{CCS}\text{ MAX}$ to V_{IH} Min. level.
 3. In $CE2s$ controlled data retention mode, input and input/output pins can be used between -0.3 V to $V_{CCS}+0.3\text{ V}$.

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	11	14	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	12	16	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	14	16	pF
C _{IN3}	$\overline{WP}/ACC$ Pin Capacitance	V _{IN} = 0	17	20	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ HANDLING OF PACKAGE

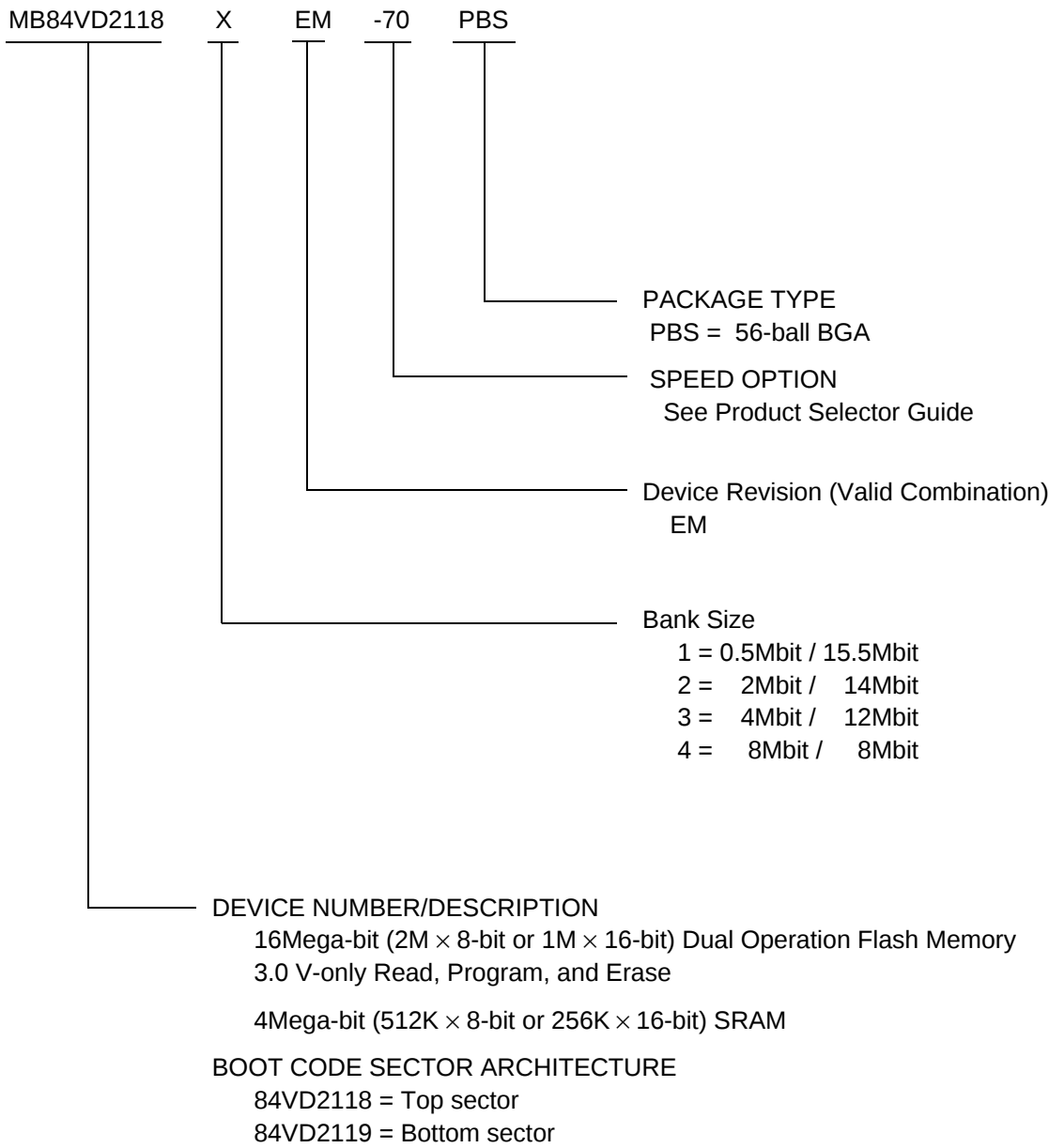
Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

- The high voltage (V_{ID}) cannot apply to address pins and control pins except $\overline{RESET}$.
Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to $\overline{RESET}$.
- Without the high voltage (V_{ID}), sector group protection can be achieved by using “Extended Sector Group Protection” command.

MB84VD2118XEM/MB84VD2119XEM-70

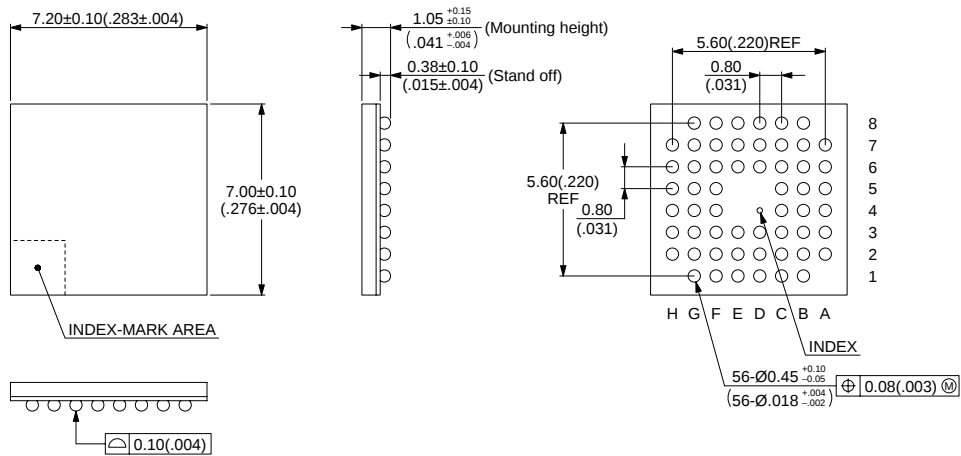
■ ORDERING INFORMATION



MB84VD2118XEM/MB84VD2119XEM-70

■ PACKAGE DIMENSIONS

56-pin plastic FBGA
(BGA-56P-M02)



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Dimension in mm.

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