MRF39RA

Low-Power, Integrated UHF Receiver

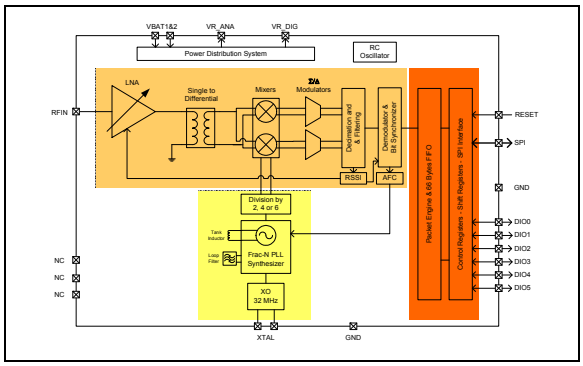
Features

- High Sensitivity:
  - down to -120 dBm at 1.2 kbps
- High Selectivity:
  - 16-Tap FIR channel filter
- Bullet-Proof Front End:
  - IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB blocking immunity, no image frequency response
- Low Current:
  - Rx = 16 mA, 100 nA register retention
- Constant RF Performance over Voltage Range of Chip
- FSK Bit Rates up to 300 kbps
- Fully Integrated Synthesizer with a Resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK Demodulation
- Built-in Bit Synchronizer Performing Clock Recovery
- Incoming Sync Word Recognition
- 115 dB+ Dynamic Range Received Signal Strength Indicator (RSSI)
- Automatic RF Sense with Ultra-Fast Automatic Frequency Control (AFC)
- Packet Engine with CRC, AES-128 Encryption and 66-Byte First In First Out (FIFO)
- Built-in Temperature Sensor and Low-Battery Indicator

General Description

The MRF39RA device is a highly integrated RF receiver capable of operation over a wide frequency range, including the 433, 868 and 915 MHz license-free Industry Scientific and Medical (ISM) frequency bands. Its highly integrated architecture enables for a minimum of external components while maintaining maximum design flexibility. All major RF communication parameters are programmable and most of these can be dynamically set. The MRF39RA offers the unique advantage of programmable narrow-band and wide-band communication modes without the need of modifying external components. The MRF39RA is optimized for low-power consumption while offering high sensitivity and channelized operation. TrueRF™ technology enables a low-cost external component count (elimination of the SAW filter) while still satisfying the European Telecommunications Standards Institute (ETSI) and Federal Communications Commission (FCC) regulations.

FIGURE 1: MRF39RA RECEIVER: LOW-POWER INTEGRATED UHF RECEIVER

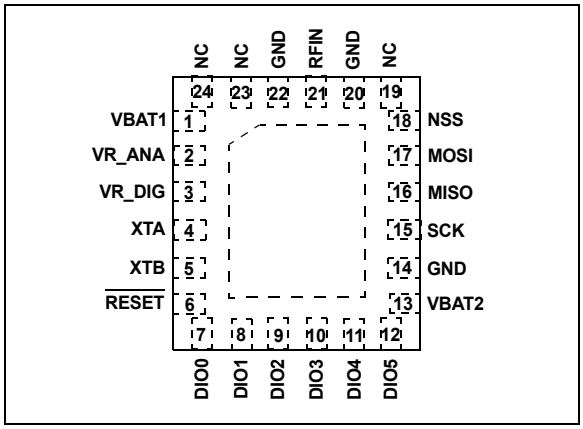


Typical Applications

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless M-Bus

Pin Diagram

FIGURE 2: 24-PIN QFN



Markets

- Europe: EN 300-220-1
- North America: FCC Part 15.247, 15.249, 15.231
- Narrow Korean and Japanese Bands

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1.0 OVERVIEW

The MRF39RA is a single-chip integrated circuit ideally suited for today's high-performance ISM band RF applications. The MRF39RA's advanced features set, including state-of-the-art packet engine, greatly simplifies system design while the high level of integration reduces the external bill of materials (BOM) to a handful of passive decoupling and matching components. It is intended for use as a high-performance, low-cost FSK and OOK RF receiver for robust frequency agile RF links, and where stable and constant RF performance is required over the full operating range of the device down to 1.8V.

The MRF39RA is intended for applications over a wide frequency range, including the 433 MHz and 868 MHz European and 902-928 MHz North American ISM bands. Coupled with a very aggressive sensitivity, the advanced system features of the MRF39RA include a 66-byte RX FIFO, configurable automatic packet handler, Listen mode, temperature sensor and configurable DIOs, which greatly enhance system flexibility while significantly reducing MCU requirements at the same time.

The MRF39RA complies with both ETSI and FCC regulatory requirements and is available in a 5 x 5 mm 24-lead QFN package.

FIGURE 1-1: SIMPLIFIED BLOCK DIAGRAM

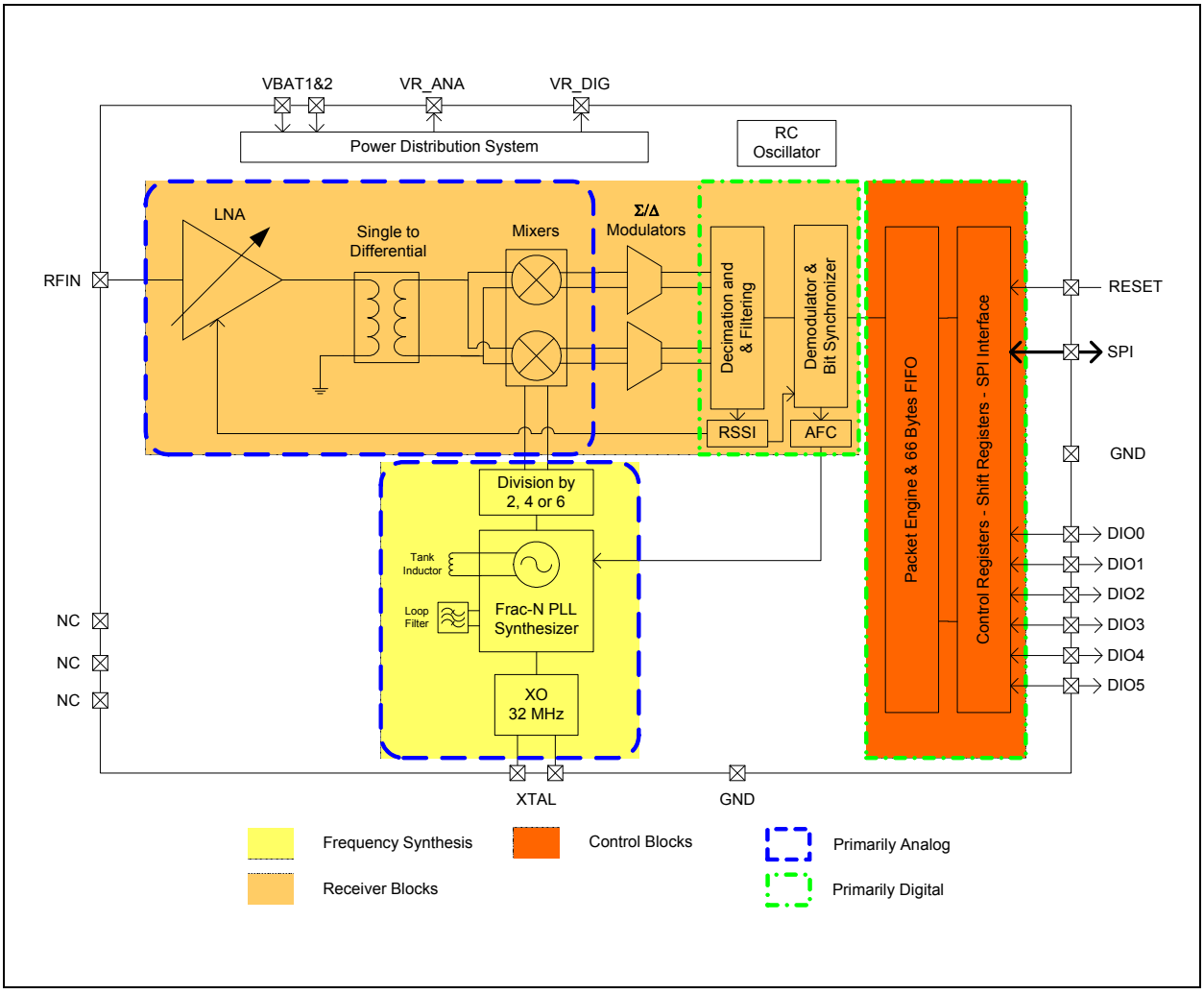


Table 1-1 lists the MRF39RA pinouts.

TABLE 1-1: MRF39RA PINOUTS

Number	Name	Type	Description
0	GROUND	—	Exposed Ground Pad
1	VBAT1	—	Supply Voltage
2	VR_ANA	—	Regulated Supply Voltage for Analogue Circuitry
3	VR_DIG	—	Regulated Supply Voltage for Digital Blocks
4	XTA	I/O	XTAL Connection
5	XTB	I/O	XTAL Connection
6	$\overline{\text{RESET}}$	I/O	Reset Trigger Input
7	DIO0	I/O	Digital I/O; Software Configured
8	DIO1/DCLK	O	Digital Output; Software Configured
9	DIO2/DATA	O	Digital Output; Software Configured
10	DIO3	I/O	Digital I/O; Software Configured
11	DIO4	I/O	Digital I/O; Software Configured
12	DIO5	I/O	Digital I/O; Software Configured
13	VBAT2	—	Supply Voltage
14	GND	—	Ground
15	SCK	I	SPI Clock Input
16	MISO	O	SPI Data Output
17	MOSI	I	SPI Data Input
18	NSS	I	SPI Chip Select Input
19	NC	—	Do not connect
20	GND	—	Ground
21	RFIN	I	RF Input
22	GND	—	Ground
23	NC	—	Do not connect
24	NC	—	Do not connect

2.0 DEVICE DESCRIPTION

This section describes in detail the architecture of the MRF39RA low-power, highly integrated receiver.

2.1 Power Supply Strategy

The MRF39RA employs an advanced power supply scheme, which provides stable operating characteristics over the full temperature and voltage range of operation.

The MRF39RA can be powered from any low-noise voltage source via pins VBAT1 and VBAT2. As suggested in the reference design, decoupling capacitors must be connected on VR_DIG and VR_ANA pins to ensure a correct operation of the built-in voltage regulators.

2.2 Low Battery Detector

A low battery detector is also included enabling the generation of an interrupt signal in response to passing a programmable threshold adjustable through the RegLowBat register. The interrupt signal can be mapped to any of the DIO pins through the programming of RegDioMapping.

2.3 Frequency Synthesis

The LO generation on the MRF39RA is based on a state-of-the-art fractional-N PLL. The PLL is fully integrated with automatic calibration.

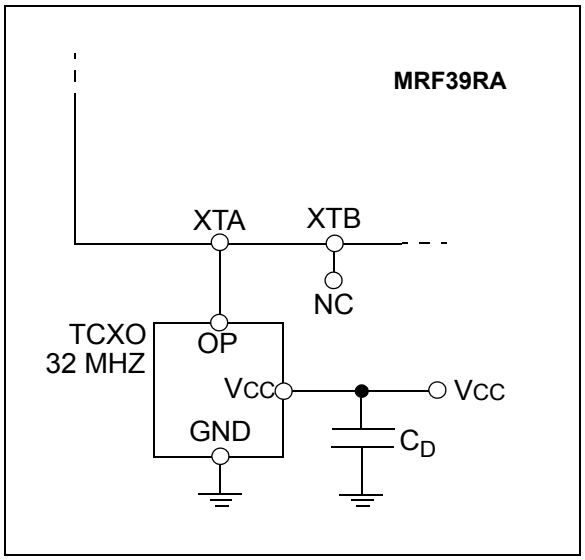
2.3.1 REFERENCE OSCILLATOR

The crystal oscillator is the main timing reference of the MRF39RA. It is used as a reference for the frequency synthesizer and as a clock for the digital processing.

The XO start-up time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. When using the built-in sequencer, the MRF39RA optimizes the start-up time and automatically triggers the PLL when the XO signal is stable. To manually control the start-up time, the user must either wait for TS_OSC max, or monitor the signal CLKOUT, which is only made available on the output buffer when a stable XO oscillation is achieved.

An external clock can be used to replace the crystal oscillator, for instance a tight tolerance TCXO. To do this, bit 4 at address 0x59 must be set to '1', and the external clock has to be provided on XTA (pin 4). XTB (pin 5) must be left open. The peak-peak amplitude of the input signal must never exceed 1.8V. Consult the TCXO supplier for an appropriate value of decoupling capacitor, CD. Figure 2-1 shows the TCXO connection.

FIGURE 2-1: TCXO CONNECTION



2.3.2 CLKOUT OUTPUT

The reference frequency, or a fraction of it, can be provided on DIO5 (pin 12) by modifying bits ClkOut in RegDioMapping2. Two typical applications of the CLKOUT output include:

- Providing a clock output for a companion processor, thus saving the cost of an additional oscillator; CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at Power-on Reset
- Providing an oscillator reference output; measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the MRF39RA, ensure that the CLKOUT signal is disabled when not required.

2.3.3 PLL ARCHITECTURE

The frequency synthesizer generating the LO frequency for the receiver is a fractional-N sigma-delta PLL. The PLL incorporates a third-order loop capable of fast auto-calibration, and it has a fast switching time. The VCO and the loop filter are both fully integrated, removing the need for an external tight-tolerance, high-Q inductor in the VCO tank circuit.

2.3.3.1 VCO

The VCO runs at two, four or six times the RF frequency (respectively in the 915, 434 and 315 MHz bands) to reduce any LO leakage in Receiver mode, to improve the quadrature precision of the receiver.

The VCO calibration is fully automated. A coarse adjustment is carried out at Power-on Reset, and a fine tuning is performed each time the MRF39RA PLL is activated. Automatic calibration times are fully transparent to the end user as their processing time is included in the TS_RE specifications.

2.3.3.2 PLL Bandwidth

The bandwidth of the MRF39RA Fractional-N PLL is wide enough to enable for very fast PLL lock times, enabling both short start-up and fast hop times required for frequency-agile applications.

2.3.3.3 Carrier Frequency and Resolution

The MRF39RA PLL embeds a 19-bit sigma-delta modulator and its frequency resolution, constant over the whole frequency range, see Equation 2-1.

EQUATION 2-1: CARRIER FREQUENCY STEP

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The carrier frequency is programmed through RegFrf, split across addresses 0x07 to 0x09:

EQUATION 2-2: CARRIER FREQUENCY

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

Note:	The Frf setting is split across three bytes. A change in the center frequency is only taken into account when the Least Significant Byte FrfLsb in RegFrfLsb is written.

2.3.4 LOCK TIME

PLL lock time TS_FS is a function of a number of technical factors, such as synthesized frequency, frequency step, and so on. When using the built-in sequencer, the MRF39RA optimizes the start-up time and automatically starts the receiver when the PLL is locked. To manually control the start-up time, the user must either wait for TS_FS max as given in the specification, or monitor the signal PLL lock detect indicator, which is set when the PLL is within its locking range.

When performing an AFC, which usually corrects very small frequency errors, the PLL response time is shown in Equation 2-3.

EQUATION 2-3: PLL RESPONSE TIME

$$T_{PLLAFC} = \frac{5}{PLLBW}$$

In a frequency hopping scheme, the TS_HOP timings in Table 7-4 give an order of magnitude for the expected lock times.

2.3.5 LOCK DETECT INDICATOR

A lock indication signal can be made available on some of the DIO pins, which is toggled high when the PLL reaches its locking range. Refer to Table 4-2 and Table 4-3 to map this interrupt to the desired pins.

2.4 Receiver Description

The MRF39RA features a digital receiver with the Analog-to-Digital conversion process being performed directly following the LNA-mixers block. The zero-IF receiver is able to handle (G)FSK and (G)MSK modulation. ASK and OOK modulation is, however, demodulated by a low-IF architecture. All the filtering, demodulation, gain control, synchronization and packet handling is performed digitally, which enables a very wide range of bit rates and frequency deviations to be selected. The receiver is also capable of automatic gain calibration to improve precision on RSSI measurements.

FIGURE 2-2: RECEIVER BLOCK DIAGRAM

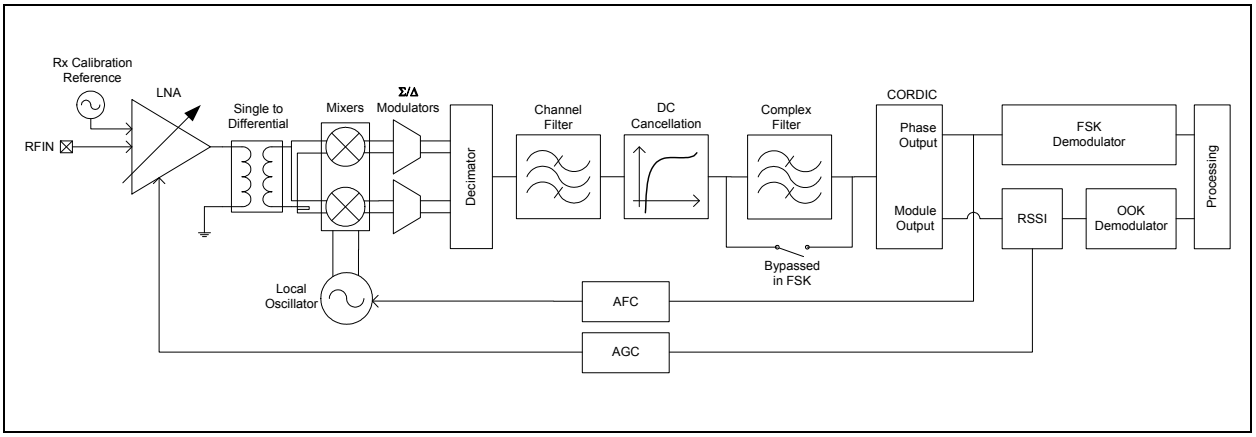


Figure 2-2 shows the receiver block diagram, and the following sections provides a brief description of each of the receiver blocks.

2.4.1 LNA – SINGLE-TO-DIFFERENTIAL BUFFER

The LNA uses a common-gate topology, which enables for a flat characteristic over the whole frequency range. It is designed to have an input impedance of 50 Ohms or 200 Ohms (as selected with bit LnaZin in RegLna), and the parasitic capacitance at the LNA input port is canceled with the external RF choke. A single-to-differential buffer is implemented to improve the second order linearity of the receiver.

The LNA gain, including the single-to-differential buffer, is programmable over a 48 dB dynamic range, and control is either manual or automatic with the embedded AGC function.

Note: In the specific case where the LNA gain is manually set by the user, the receiver is unable to properly handle FSK signals with a modulation index smaller than 2 at an input power greater than the 1 dB compression point, tabulated in **Section 2.4.2 "Automatic Gain Control"**.

Table 2-1 shows the LNA Gain settings.

TABLE 2-1: LNA GAIN SETTINGS

LnaGainSelect	LNA Gain	Gain Setting
000	Any of the below, set by the AGC loop	—
001	Max gain	G1
010	Max gain – 6 dB	G2
011	Max gain – 12 dB	G3
100	Max gain – 24 dB	G4
101	Max gain – 36 dB	G5
110	Max gain – 48 dB	G6
111	Reserved	—

2.4.2 AUTOMATIC GAIN CONTROL

By default (LnaGainSelect = `000`) the LNA gain is controlled by a digital AGC loop to obtain the optimal sensitivity/linearity trade-off.

Regardless of the Data Transfer mode (Packet or Continuous), the following series of events takes place when the receiver is enabled:

- The receiver stays in Wait mode, until RssiValue exceeds RssiThreshold for two consecutive samples. Its power consumption is the receiver power consumption.
- When this condition is satisfied, the receiver automatically selects the most suitable LNA gain, optimizing the sensitivity/linearity trade-off.
- The programmed LNA gain, read-accessible with LnaCurrentGain in RegLna, is carried on for the whole duration of the packet, until one of the following conditions is fulfilled:
- **Packet mode**: if AutoRxRestartOn = `0`, the LNA gain remains the same for the reception of the following packet. If AutoRxRestartOn = `1`, after the controller has emptied the FIFO the receiver re-enters the Wait mode, after a delay of InterPacketRxDelay, enabling for the distant transmitter to ramp down, hence avoiding a false RSSI detection. In both cases (AutoRxRestartOn = `0` or AutoRxRestartOn = `1`), the receiver can also re-enter the Wait mode by setting RestartRx bit to '`1`'. The user can decide to do this to manually launch a new AGC procedure.
- **Continuous mode**: upon reception of valid data, the user can decide to either leave the receiver enabled with the same LNA gain, or to restart the procedure, by setting RestartRx bit to '`1`', resuming the Wait mode of the receiver, described above.

Figure 2-3 illustrates the AGC behavior.

Note 1: The AGC procedure must be performed while receiving preamble in FSK mode.

2: In OOK mode, the AGC gives better results if performed while receiving a constant '`1`' sequence.

FIGURE 2-3: AGC THRESHOLDS SETTINGS

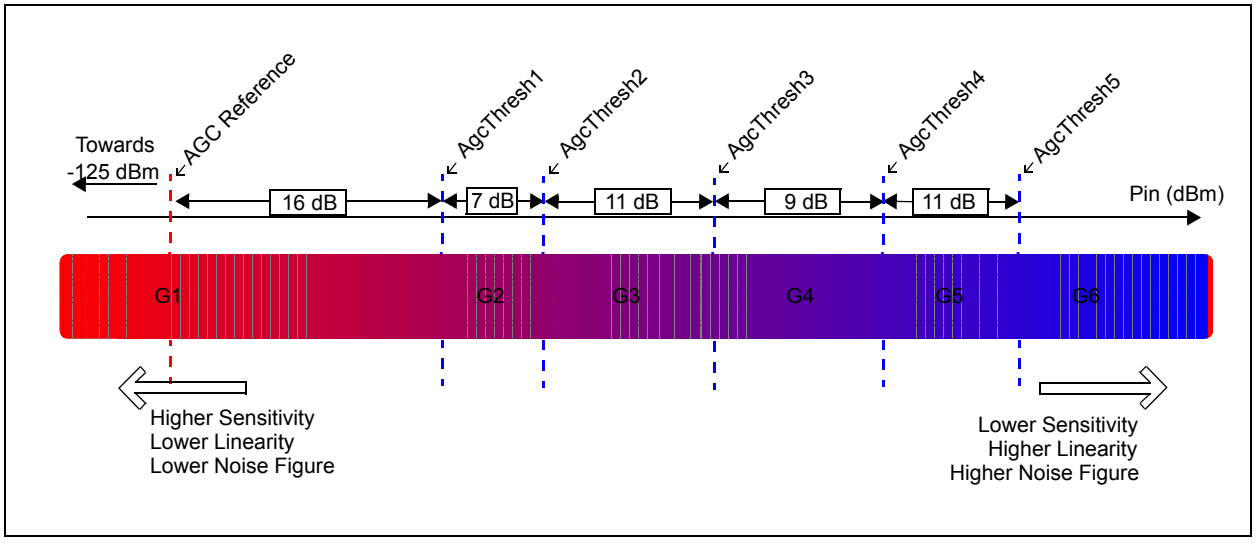


Table 2-2 summarizes the performance (typical figures) of the complete receiver.

TABLE 2-2: RECEIVER PERFORMANCE SUMMARY

Input Power Pin	Gain Setting	Receiver Performance (typ.)			
		P_{-1dB} [dBm]	NF [dB]	IIP3 [dBm]	IIP2 [dBm]
Pin < AgcThresh1	G1	-37	7	-18	+35
AgcThresh1 < Pin < AgcThresh2	G2	-31	13	-15	+40
AgcThresh2 < Pin < AgcThresh3	G3	-26	18	-8	+48
AgcThresh3 < Pin < AgcThresh4	G4	-14	27	-1	+62
AgcThresh4 < Pin < AgcThresh5	G5	>-6	36	+13	+68
AgcThresh5 < Pin	G6	>0	44	+20	+75

2.4.2.1 RssiThreshold Setting

For correct operation of the AGC, set the RssiThreshold in RegRssiThresh to the sensitivity of the receiver. The receiver remains in Wait mode until RssiThreshold is exceeded.

Note: When AFC is enabled and automatically performed at the receiver start-up, the channel filter used by the receiver during the AFC and AGC is RxBwAfc instead of the standard RxBw setting. This may impact the sensitivity of the receiver and the setting of RssiThreshold accordingly.

2.4.2.2 AGC Reference

The AGC reference level is automatically computed in the MRF39RA, according to the formula in Equation 2-4.

EQUATION 2-4: AGC REFERENCE LEVEL

$$AGC\ Reference\ [dBm] = -174 + NF + DemoSnr + 10.log(2*RxBw) + FadingMargin[dBm]$$

Where:

- NF = 7 dB : LNA's Noise Figure at maximum gain
- DemodSnr = 8 dB : SNR needed by the demodulator
- RxBw : Single sideband channel filter bandwidth
- FadingMargin = 5 dB : Fading margin

2.4.3 CONTINUOUS-TIME DAGC

In addition to the automatic gain control described in **Section 2.4.2 "Automatic Gain Control"**, the MRF39RA is capable of continuously adjusting its gain in the digital domain, after the Analog-to-Digital conversion has occurred. This feature, named DAGC, is fully transparent to the end user. The digital gain adjustment is repeated every two bits and has the following benefits:

- Fully transparent to the end user
- Improves the fading margin of the receiver during the reception of a packet, even if the gain of the LNA is frozen
- Improves the receiver robustness in fast fading signal conditions by quickly adjusting the receiver gain (every two bits)
- Works in Continuous, Packet and Unlimited Length Packet modes.

The DAGC is enabled by setting RegTestDagc to 0x20 for low modulation index systems (i.e., when AfcLowBetaOn = '1') and 0x30 for other systems. See **Section 2.4.17 "Optimized Setup for Low Modulation Index Systems"**. It is recommended to always enable the DAGC.

2.4.4 QUADRATURE MIXER – ADCs – DECIMATORS

The mixer is inserted between the output of the RF buffer stage and the input of the Analog-to-Digital Converter (ADC) of the receiver section. This block is designed to translate the spectrum of the input RF signal to base-band, and offer both high IIP2 and IIP3 responses.

In the lower bands of operation (290 to 510 MHz), the multi-phase mixing architecture with weighted phases improves the rejection of the LO harmonics in Receiver mode, hence increasing the receiver immunity to out-of-band interferers.

The I and Q digitalization is made by two 5th order continuous-time sigma-delta Analog-to-Digital Converters (ADC). Gain is not constant over temperature, but the whole receiver is calibrated before reception that this inaccuracy has no impact on the RSSI precision. The ADC output is one bit per channel. It needs to be decimated and filtered afterwards. This ADC can also be used for temperature measurement. For more details, refer to **Section 2.4.18 "Temperature Sensor"**.

The decimators decrease the sample rate of the incoming signal to optimize the area and power consumption of the following receiver blocks.

2.4.5 CHANNEL FILTER

The role of the channel filter is to filter out the noise and interferers outside of the channel. Channel filtering on the MRF39RA is implemented with a 16-tap finite impulse response (FIR) filter, providing an outstanding adjacent channel rejection performance, even for narrow-band applications.

Note:	To respect oversampling rules in the decimation chain of the receiver, the bit rate cannot be set at a higher value than two times the single-side receiver bandwidth (BitRate < 2 x RxBw)

The single-side channel filter bandwidth RxBw is controlled by the RxBwMant and RxBwExp parameters in RegRxBw, as shown in Equation 2-5.

EQUATION 2-5: RXBW

When FSK modulation is enabled:

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp + 2}}$$

When OOK modulation is enabled:

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp + 3}}$$

Table 2-3 lists the accessible channel filter bandwidths (oscillator is mandated at 32 MHz).

TABLE 2-3: AVAILABLE RxBw SETTINGS

RxBwMant (binary/value)	RxBwExp (decimal)	RxBw (kHz)	
		FSK ModulationType = 00	OOK ModulationType = 01
10b/24	7	2.6	1.3
01b/20	7	3.1	1.6
00b/16	7	3.9	2.0
10b/24	6	5.2	2.6
01b/20	6	6.3	3.1
00b/16	6	7.8	3.9
10b/24	5	10.4	5.2
01b/20	5	12.5	6.3
00b/16	5	15.6	7.8
10b/24	4	20.8	10.4
01b/20	4	25.0	12.5
00b/16	4	31.3	15.6
10b/24	3	41.7	20.8
01b/20	3	50.0	25.0
00b/16	3	62.5	31.3
10b/24	2	83.3	41.7
01b/20	2	100.0	50.0
00b/16	2	125.0	62.5
10b/24	1	166.7	83.3
01b/20	1	200.0	100.0
00b/16	1	250.0	125.0
10b/24	0	333.3	166.7
01b/20	0	400.0	200.0
00b/16	0	500.0	250.0

2.4.6 DC CANCELLATION

DC cancellation is required in zero-IF architecture transceivers to remove any DC offset generated through self-reception. It is built in the MRF39RA and its adjustable cutoff frequency (fc) is controlled in RegRxBw. Table 2-4 shows the available DCC cutoff frequencies.

TABLE 2-4: AVAILABLE DCC CUTOFF FREQUENCIES

DccFreq in RegRxBw	fc in % of RxBw
000	16
001	8
010 (default)	4
011	2
100	1
101	0.5
110	0.25
111	0.125

The default value of DccFreq cutoff frequency is typically 4% of the RxBw (channel filter BW). The cutoff frequency of the DCC can however be increased to slightly improve the sensitivity, under wider modulation conditions. It is advised to adjust the DCC setting while monitoring the receiver sensitivity.

2.4.7 COMPLEX FILTER – OOK

In OOK mode the MRF39RA is modified to a low-IF architecture. The IF frequency is automatically set to half the single-side bandwidth of the channel filter (FIF = 0.5 x RxBw). The Local Oscillator is automatically offset by the IF in the OOK receiver. A complex filter is implemented on the chip to attenuate the resulting image frequency by typically 30 dB.

Note:	This filter is automatically bypassed when receiving FSK signals (ModulationType = 00 in RegDataModul).

2.4.8 RSSI

The RSSI block evaluates the amount of energy available within the receiver channel bandwidth. Its resolution is 0.5 dB, and it has a wide dynamic range to accommodate both small and large signal levels that may be present. Its acquisition time is very short, only taking 2-bit periods. The RSSI sampling must occur during the reception of preamble in FSK and constant '1' reception in OOK. Figure 2-4 shows the RSSI dynamic curve.

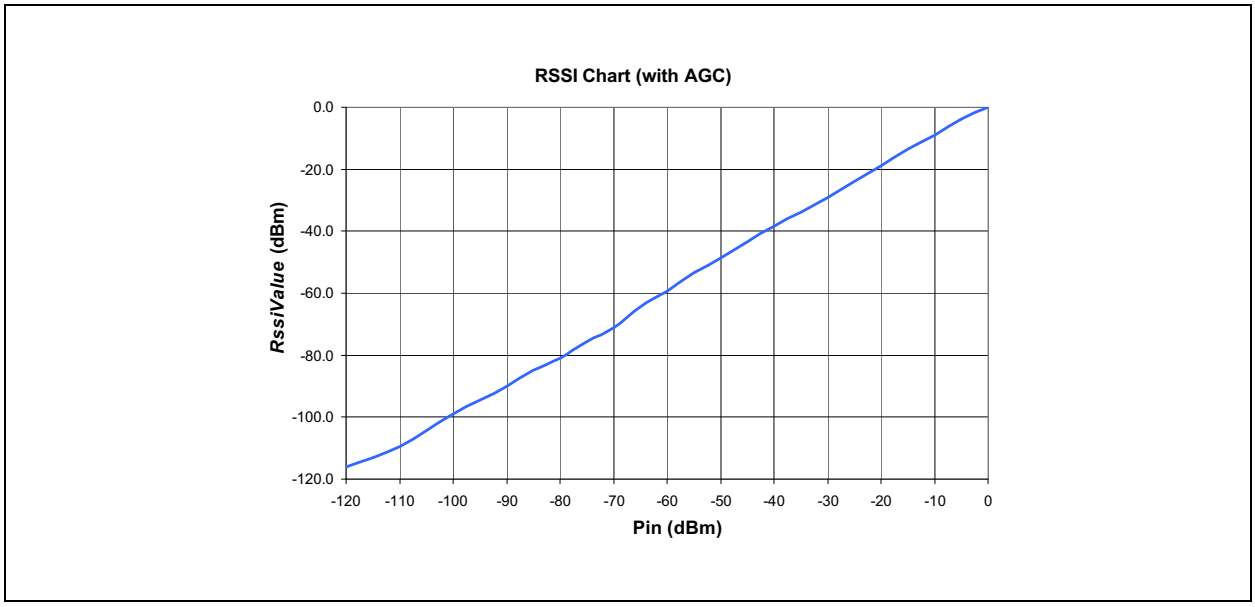
Note 1: RssiValue can only be read when it exceeds RssiThreshold.

2: RssiStart command and RssiDone flags are not usable when DAGC is turned on. See **Section 2.4.3 "Continuous-Time DAGC"**.

3: The receiver is capable of automatic gain calibration to improve the precision of its RSSI measurements. This function injects a known RF signal at the LNA input and calibrates the receiver gain accordingly. This calibration is automatically performed during the PLL start-up, making it a transparent process to the end user.

4: RSSI accuracy depends on all components located between the antenna port and pin RFIO and is therefore limited to a few decibels. Board-level calibration is advised to further improve accuracy.

FIGURE 2-4: RSSI DYNAMIC CURVE



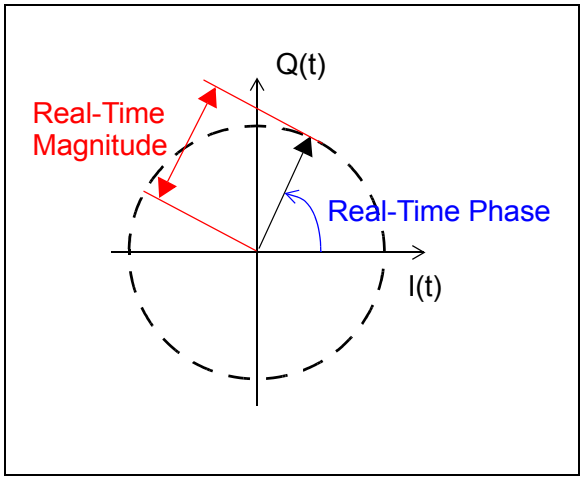
2.4.9 CORDIC

The Cordic task is to extract the phase and the amplitude of the modulation vector (I + j.Q). The following information is used, still in the digital domain:

- **Phase output**: used by the FSK demodulator and the AFC blocks
- **Amplitude output**: used by the RSSI block for FSK demodulation, AGC and automatic gain calibration purposes.

Figure 2-5 shows the cordic extraction.

FIGURE 2-5: CORDIC EXTRACTION



2.4.10 BIT RATE SETTING

The bit rate (BR) is controlled by the BitRate bits in RegBitrate, as shown in Equation 2-6 below.

EQUATION 2-6: BIT RATE

$$BR = \frac{F_{XOSC}}{BitRate}$$

Table 2-5 lists some of the accessible bit rates.

TABLE 2-5: BIT RATE EXAMPLES

Type	BitRate <15:8>	BitRate <7:0>	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical Modem Baud Rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps	—	38415.36
	0x01	0xA1	76.8 kbps	—	76738.60
	0x00	0xD0	153.6 kbps	—	153846.1
Classical Modem Baud Rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps	—	57553.95
	0x01	0x16	115.2 kbps	—	115107.9
Round Bit Rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x02	0x80	50 kbps	—	50000.00
	0x01	0x40	100 kbps	—	100000.0
	0x00	0xD5	150 kbps	—	150234.7
	0x00	0xA0	200 kbps	—	200000.0
	0x00	0x80	250 kbps	—	250000.0
	0x00	0x6B	300 kbps	—	299065.4
Watch Xtal Frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

2.4.11 FSK DEMODULATOR

The FSK demodulator of the MRF39RA is designed to demodulate FSK, GFSK, MSK and GMSK modulated signals. It is most efficient when the modulation index of the signal is greater than 0.5 and below 10, see Equation 2-7.

EQUATION 2-7: MODULATION INDEX

$$0.5 \leq \beta = \frac{2 \times F_{DEV}}{BR} \leq 10$$

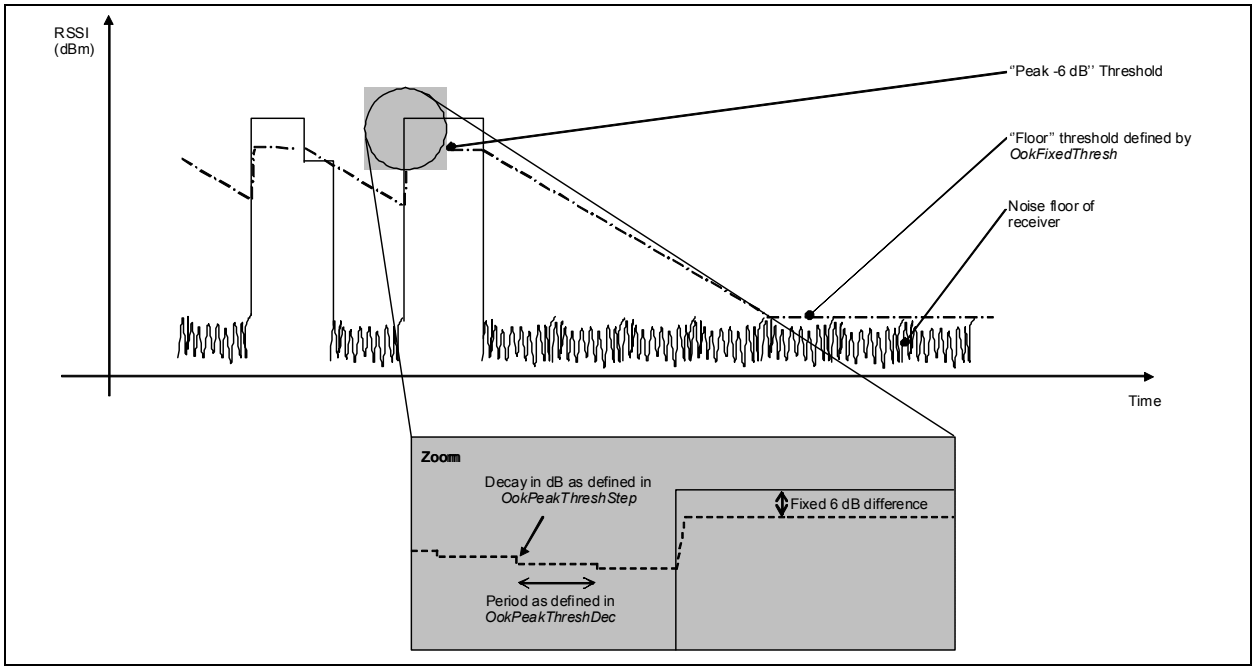
The output of the FSK demodulator can be fed to the bit synchronizer as described in **Section 2.4.14 "Bit Synchronizer"** to provide the companion processor with a synchronous data stream in Continuous mode.

2.4.12 OOK DEMODULATOR

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, configured through bits OokThreshType in RegOokPeak.

The recommended mode of operation is the Peak Threshold mode as illustrated in Figure 2-6.

FIGURE 2-6: OOK PEAK DEMODULATOR DESCRIPTION



In Peak Threshold mode the comparison threshold level is the peak value of the RSSI, reduced by 6 dB. In the absence of an input signal or during the reception of a logical '0', the acquired peak value is decremented by one OokPeakThreshStep every OokPeakThreshDec period.

When the RSSI output is null for a long time (for instance after a long string of '0' received, or if no transmitter is present), the peak threshold level continues to fall until it reaches the Floor Threshold, programmed in OokFixedThresh.

The default settings of the OOK demodulator lead to the performance stated in the electrical specification. However, in applications in which sudden signal drops are awaited during a reception, the three parameters must be optimized accordingly.

2.4.13 OPTIMIZING THE FLOOR THRESHOLD

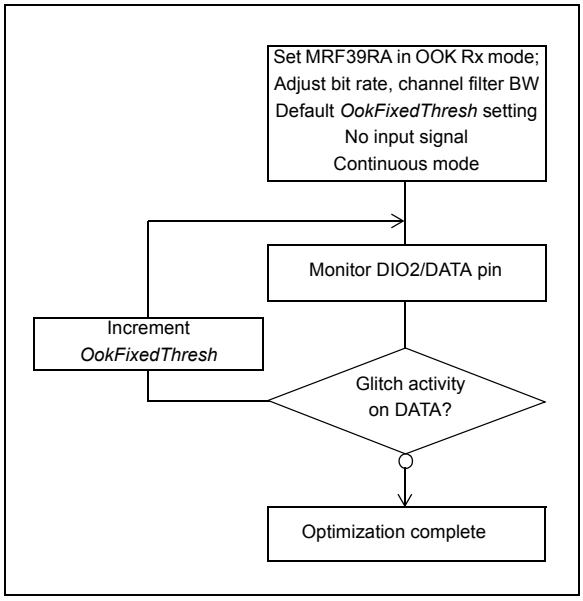
OokFixedThresh determines the sensitivity of the OOK receiver as it sets the comparison threshold for weak input signals (i.e., those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

Note that the noise floor of the receiver at the demodulator input depends on:

- The noise figure of the receiver
- The gain of the receive chain from antenna to base band
- The matching, including SAW filter (if any)
- The bandwidth of the channel filters.

It is important to note that OokFixedThresh setting is application-dependent. The following procedure as illustrated in Figure 2-7 is recommended to optimize OokFixedThresh.

FIGURE 2-7: FLOOR THRESHOLD OPTIMIZATION



The new floor threshold value found during this test must be used for OOK reception with those receiver settings.

2.4.13.1 Optimizing OOK Demodulator for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated, the OokPeakThreshStep and OokPeakThreshDec parameters can be optimized for a given number of threshold decrements per bit. Refer to RegOokPeak to access those settings.

2.4.13.2 Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK Threshold mode, the user can alternatively select two other types of threshold detectors:

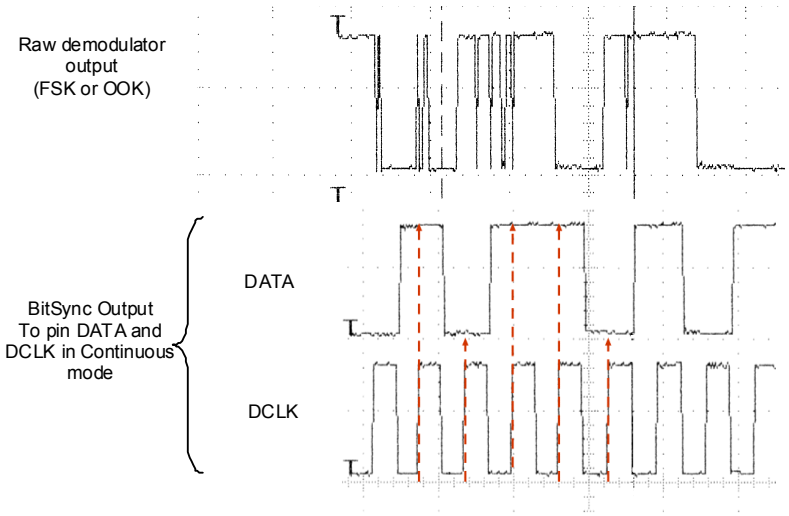
- **Fixed Threshold**: the value is selected through OokFixedThresh
- **Average Threshold**: data supplied by the RSSI block is averaged and this operation mode must be used only with DC-free encoded data.

2.4.14 BIT SYNCHRONIZER

The bit synchronizer is a block that provides a clean and synchronized digital output, free of glitches. Its output is made available on pin DIO1/DCLK in Continuous mode and can be disabled through register settings. However, for optimum receiver performance it is used when running Continuous mode is strongly advised.

The bit synchronizer is automatically activated in Packet mode. Its bit rate is controlled by BitRateMsb and BitRateLsb in RegBitrate.

FIGURE 2-8: BIT SYNCHRONIZER DESCRIPTION



To ensure correct operation of the bit synchronizer, the following conditions must be satisfied:

- A preamble (0x55 or 0xAA) of at least 12 bits is required for synchronization; the longer the synchronization, the better the packet success rate
- The subsequent payload bit stream must have at least one transition from '0' to '1' or '1' to '0' every 16 bits during data transmission
- The bit rate matching between the transmitter and the receiver must be better than 6.5%.

2.4.15 FREQUENCY ERROR INDICATOR (FEI)

This function provides information about the frequency error of the local oscillator (LO) compared with the carrier frequency of a modulated signal at the input of the receiver. When the FEI block is launched, the frequency error is measured and the signed result is loaded in FeiValue in RegFei, in two's complement format. The time required for an FEI evaluation is four times the bit period.

To ensure a proper behavior of the FEI:

- The operation must be done during the reception of preamble
- The sum of the frequency offset and the 20 dB signal bandwidth must be lower than the base band filter bandwidth.

The 20 dB bandwidth of the signal (double-side bandwidth) can be evaluated as shown in Equation 2-8.

EQUATION 2-8: 20 DB BANDWIDTH

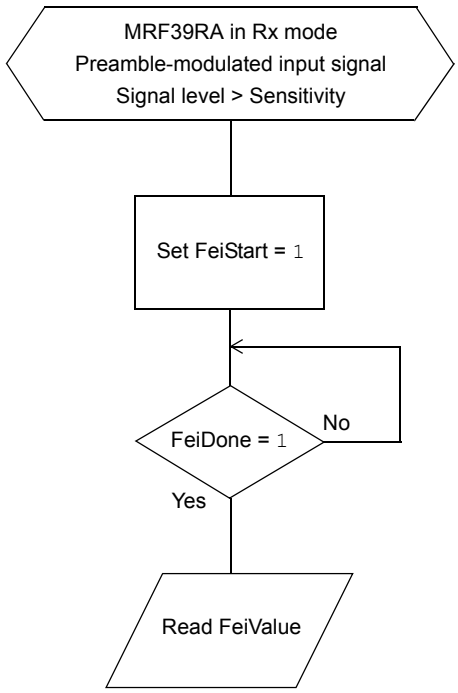
$$BW_{20dB} = 2 \times \left(F_{DEV} + \frac{BR}{2} \right)$$

The frequency error, in Hz, can be calculated with the formula in Equation 2-9.

EQUATION 2-9: FREQUENCY ERROR-HZ

$$FEI = F_{STEP} \times FeiValue$$

FIGURE 2-9: FEI PROCESS



2.4.16 AUTOMATIC FREQUENCY CORRECTION

The AFC is based on the FEI block and, therefore, the same input signal and receiver setting conditions apply. When the AFC procedure is done, AfcValue is directly subtracted to the register that defines the frequency of operation of the chip, FRF. The AFC can be launched in the following cases:

- Each time the receiver is enabled, if AfcAutoOn = 1
- Upon user request, by setting bit AfcStart in RegAfcFei, if AfcAutoOn = 0

When the AFC is automatically triggered (AfcAutoOn = 1), the user has the option to:

- Clear the former AFC correction value, if AfcAutoClearOn = 1
- Start the AFC evaluation from the previously corrected frequency. This may be useful in systems in which the LO keeps on drifting in the same direction. Aging compensation is a good example.

The MRF39RA offers an alternate receiver bandwidth setting during the AFC phase to accommodate large LO drifts. If the user considers that the received signal may be out of the receiver bandwidth, a higher channel filter bandwidth can be programmed in RegAfcBw, at the expense of the receiver noise floor, which produces impact upon sensitivity.

2.4.17 OPTIMIZED SETUP FOR LOW MODULATION INDEX SYSTEMS

For wide band systems, where AFC is usually not required (XTAL inaccuracies do not typically impact the sensitivity), it is recommended to offset the LO frequency of the receiver to avoid desensitization. This can be simply done by modifying Frf in RegFrfLsb. A good rule of thumb is to offset the receiver's LO by 10% of the expected transmitter frequency deviation.

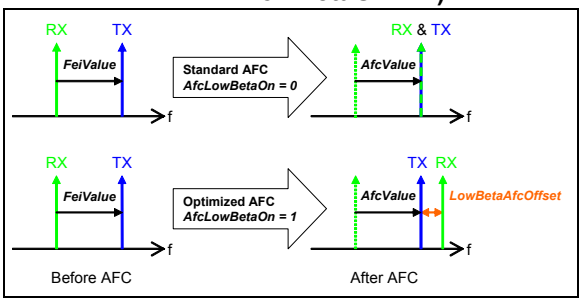
For narrow band systems, it is recommended to perform AFC. The MRF39RA has a dedicated AFC, enabled when AfcLowBetaOn in RegAfcCtrl is set to '1'. A frequency offset, programmable through LowBetaAfcOffset in RegTestAfc, is added and is calculated as shown in Equation 2-10.

EQUATION 2-10: FREQUENCY OFFSET

$$Offset = LowBetaAFCOffset \times 488\ Hz$$

The user must ensure that the programmed offset exceeds the DC canceler's cutoff frequency, set through DccFreqAfc in RegAfcBw.

FIGURE 2-10: OPTIMIZED AFC (Afc LowBetaOn = 1)



As shown in Figure 2-10, a standard AFC sequence uses the result of the FEI to correct the LO frequency and align both local oscillators. When the optimized AFC is enabled (AfcLowBetaOn = 1), the receiver's LO is corrected by FeiValue + LowBetaAfcOffset.

When the optimized AFC routine is enabled, the receiver start-up time can be computed as shown in Equation 2-11, see **Section 3.2.1 "Receiver Start-up Time"**.

EQUATION 2-11: RECEIVER START-UP TIME

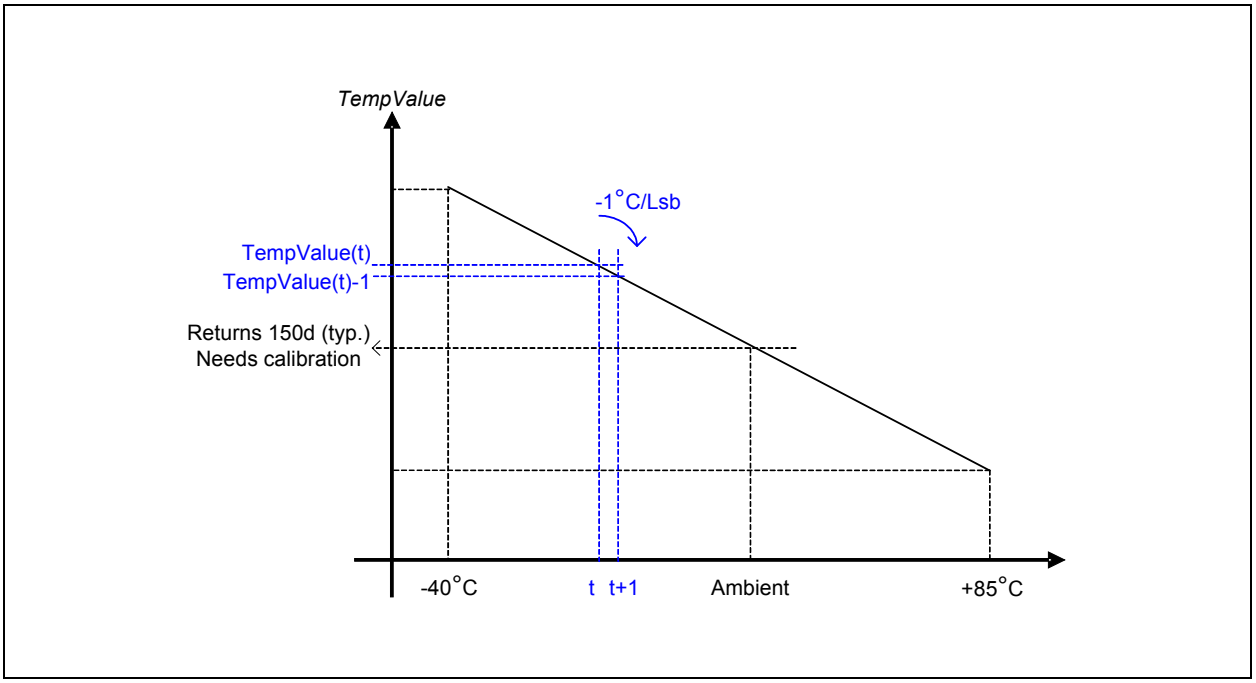
$$TS\_RE\_AGC\&AFC\ (optimized\ AFC) =$$
$$= T_{ANA} + 4.T_{CF} + 4.T_{DCC} + 3.T_{RSSI} + 2.T_{AFC} + 2.T_{PLLAFC}$$

2.4.18 TEMPERATURE SENSOR

When temperature is measured, the receiver ADC is used to digitize the sensor response. Most receiver blocks are disabled, and temperature measurement can only be triggered in Standby or Frequency Synthesizer modes.

As shown in Figure 2-11, the response of the temperature sensor is -1°C/Lsb. A CMOS temperature sensor is not accurate by nature; therefore, it must be calibrated at ambient temperature for precise temperature readings.

FIGURE 2-11: TEMPERATURE SENSOR RESPONSE



It takes less than 100 microseconds for the MRF39RA to evaluate the temperature from setting TempMeasStart to '1' to TempMeasRunning Reset.

2.4.19 TIME-OUT FUNCTION

The MRF39RA includes a time-out function, which enables it to automatically shut down the receiver after a receive sequence and, therefore, save energy.

- Time-out interrupt is generated, TimeoutRxStart x 16 x Tbit, after switching to RX mode if RssiThreshold flag does not raise within this time frame.
- Time-out interrupt is generated, TimeoutRssiThresh x 16 x Tbit, after RssiThreshold flag is raised.

Use Time-out interrupt to warn the companion processor to shut down the receiver and return to a lower power mode.

3.0 OPERATING MODES

3.1 Basic Modes

The circuit is set in four different basic modes as described in Table 3-1.

By default when switching from one mode to another, the sub-blocks wakes up according to a pre-defined and optimized sequence. Alternatively, these operating modes can be selected directly by disabling the automatic sequencer (SequencerOff in RegOpMode = 1).

TABLE 3-1: BASIC RECEIVER MODES

ListenOn in *RegOpMode*	Mode in *RegOpMode*	Selected mode	Enabled blocks
0	0 0 0	Sleep mode	None
0	0 0 1	Stand-by mode	Top regulator and crystal oscillator
0	0 1 0	FS mode	Frequency synthesizer
0	1 0 0	Receive mode	Frequency synthesizer and receiver
1	x	Listen mode	See **Section 3.3 "Listen Mode"**

3.2 Automatic Sequencer and Wake-up Times

By default when switching from one operating mode to another, the circuit takes care of the sequence of events in a manner that the transition timing is optimized. For example, when switching from Sleep mode to Receive mode, the MRF39RA first goes to Standby mode (XO started), then to Frequency Synthesizer mode, and finally, when the PLL has locked, to Receive mode.

The crystal oscillator wake-up time, TS_OSC, is directly related to the time for the crystal oscillator to reach its steady state. This depends notably on the crystal characteristics.

The frequency synthesizer wake-up time, TS_FS, is directly related to the time needed by the PLL to reach its steady state. The PLL_LOCK signal, provided on an external pin, gives an indication of the lock status. It goes high when the PLL reaches its locking range.

Three specific cases can be highlighted:

- Receiver wake-up time from Sleep mode = TS_OSC + TS_FS + TS_RE
- Receiver wake-up time from Sleep mode, AGC enabled = TS_OSC + TS_FS + TS_RE_AGC
- Receiver wake-up time from Sleep mode, AGC and AFC enabled = TS_OSC + TS_FS + TS_RE_AGC&AFC.

These timings are detailed in **Section 3.2.1 "Receiver Start-up Time"**.

In applications where the target average power consumption, or the target start-up time do not require setting the MRF39RA in the lowest power modes (Sleep or Standby), the respective TS_OSC and TS_FS timings in the equations above can be omitted.

3.2.1 RECEIVER START-UP TIME

It is highly recommended to use the built-in sequencer of the MRF39RA to optimize the delays when setting the chip in Receive mode. It ensures the shortest start-up times, hence the lowest possible energy usage for battery-operated systems.

The start-up times of the receiver can be calculated as shown in Figure 3-1 through Figure 3-3.

FIGURE 3-1: Rx START-UP – NO AGC, NO AFC

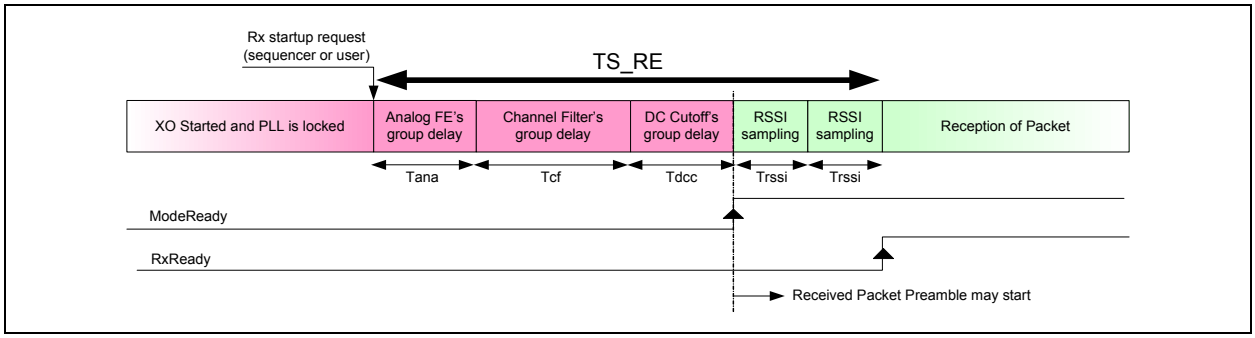


FIGURE 3-2: Rx START-UP – AGC, NO AFC

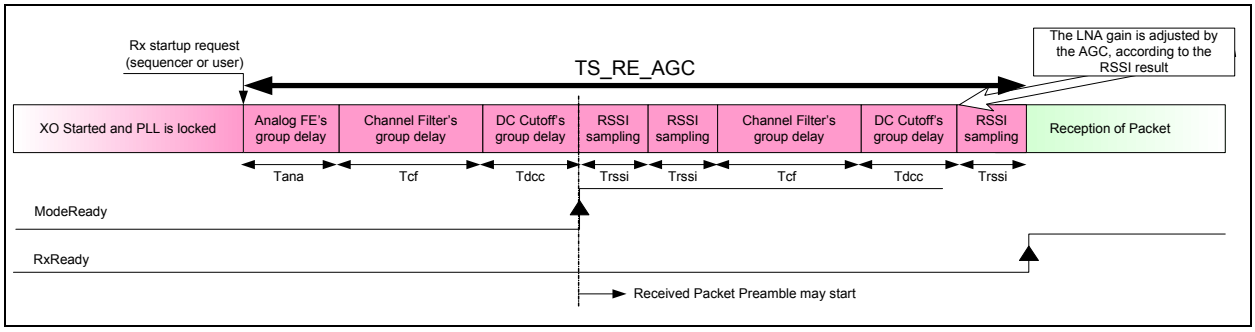
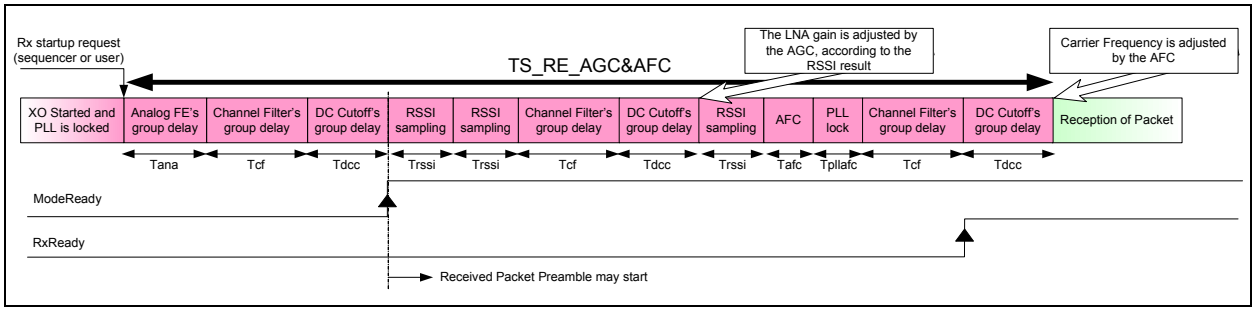


FIGURE 3-3: Rx START-UP – AGC AND AFC



The different timings shown above are as follows:

- Group delay of the analog front end: Tana = 20 µs
- Channel filter's group delay in FSK mode: Tcf = 21/(4.RxBw)
- Channel filter's group delay in OOK mode: Tcf = 34/(4.RxBw)
- DC Cutoff's group delay: Tdcc = max(8, 2^(round(log2(8.RxBw.Tbit)+1))/(4.RxBw)
- PLL lock time after AFC adjustment: Tpllafc = 5/ PLLBW (PLLBW = 300 kHz)
- AFC sample time: Tafc = 4 x Tbit (also denoted TS_AFC in the general specification)
- RSSI sample time: Trssi = 2 x int(4.RxBw.Tbit)/ (4.RxBw) (also known as TS_RSSI).

Note: The timings represent maximum settling times. Shorter settling times may be observed in real cases.

3.2.2 Rx Start Procedure

As described in the previous sections, the RxReady interrupt warns the uC that the receiver is ready.

- In Continuous mode with bit synchronizer, the receiver starts locking its bit synchronizer on a minimum or 12 bits of received preamble before the reception of correct data or sync word (if enabled) can occur. See **Section 2.4.14 "Bit Synchronizer"** for details.
- In Continuous mode without bit synchronizer, valid data is available on DIO2/DATA right after the RxReady interrupt.
- In Packet mode, the receiver starts locking its bit synchronizer on a minimum or 12 bits of received preamble before the reception of correct data or sync word (if enabled) can occur. See **Section 2.4.14 "Bit Synchronizer"** for details.

3.2.3 Optimized Frequency Hopping Sequences

In a frequency hopping-like application, it is required to turn off the receiver when hopping from one channel to another, to optimize the hopping sequence:

Receiver hop from Ch A to Ch B:

1. MRF39RA is in Rx mode in Ch A
2. Change the carrier frequency in the RegFrf registers
3. Program the MRF39RA in FS mode
4. Turn the receiver back to Rx mode
5. Respect the Rx start procedure, described in **Section 3.2.2 "Rx Start Procedure"**.

Note:	The sequence assumes that the sequencer is turned on (SequencerOff = 0 in RegOpMode).

3.3 Listen Mode

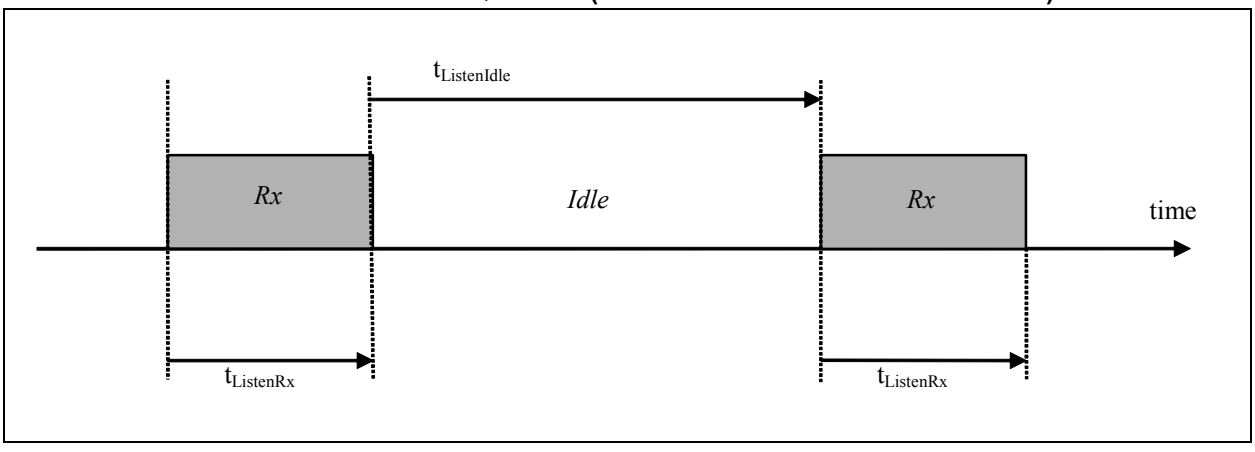
To set the circuit to Listen mode, ListenOn in RegOpMode must be set to '1' while in Standby mode. In this mode, MRF39RA spends most of the time in Idle mode, during which only the RC oscillator runs. Periodically the receiver wakes up and listens for an RF signal. If a wanted signal is detected, the receiver is kept on and the data is demodulated.

Otherwise, if a wanted signal is not detected after a predefined period of time, the receiver is disabled until the next time period.

This periodical Rx wake-up requirement is very common in low-power applications. On MRF39RA, it is locally handled by the Listen mode block without using uC resources or energy.

The simplified timing diagram of this procedure is illustrated in Figure 3-4.

FIGURE 3-4: LISTEN MODE SEQUENCE (NO WANTED SIGNAL IS RECEIVED)



3.3.1 Timings

The duration of the idle phase is given by $t_{ListenIdle}$. The time during which the receiver is on and is waiting for a signal is given by $t_{ListenRx}$. The $t_{ListenRx}$ includes the wake-up time of the receiver as described in **Section 3.2.1 "Receiver Start-up Time"**. This duration is programmed in the Configuration registers via the serial interface.

Both time periods $t_{ListenRx}$ and $t_{ListenIdle}$ (denoted $t_{ListenX}$ in the text below) are fixed by two parameters from the Configuration register and are calculated as follows:

EQUATION 3-1: TIME PERIODS

$$t_{ListenX} = ListenCoefX \bullet ListenResolX$$

Where:

ListenResolX is the Rx or idle resolution and is independently programmable on three values (64 µs, 4.1 ms or 262 ms), whereas ListenCoefX is an integer between 1 and 255. All parameters are located in RegListen registers.

The timing ranges are tabulated in Table 3-2.

TABLE 3-2: RANGE OF DURATIONS IN LISTEN MODE

ListenResolX	Min duration (ListenCoef = 1)	Max duration (ListenCoef = 255)
01	64 µs	16 ms
10	4.1 ms	1.04s
11	0.26s	67s

Note 1: The accuracy of the typical timings given in Table 3-2 depends on the RC oscillator calibration.

2: RC oscillator calibration is required and must be performed at power-up. See **Section 3.3.5 "RC Timer Accuracy"** for details.

3.3.2 Criteria

The criteria taken for detecting a wanted signal and hence deciding to maintain the receiver on is defined by ListenCriteria in RegListen1.

TABLE 3-3: SIGNAL ACCEPTANCE CRITERIA IN LISTEN MODE

ListenCriteria	Input Signal Power ≥ *RssiThreshold*	*SyncAddressMatch*
0	Required	Not Required
1	Required	Required

3.3.3 End of Cycle Actions

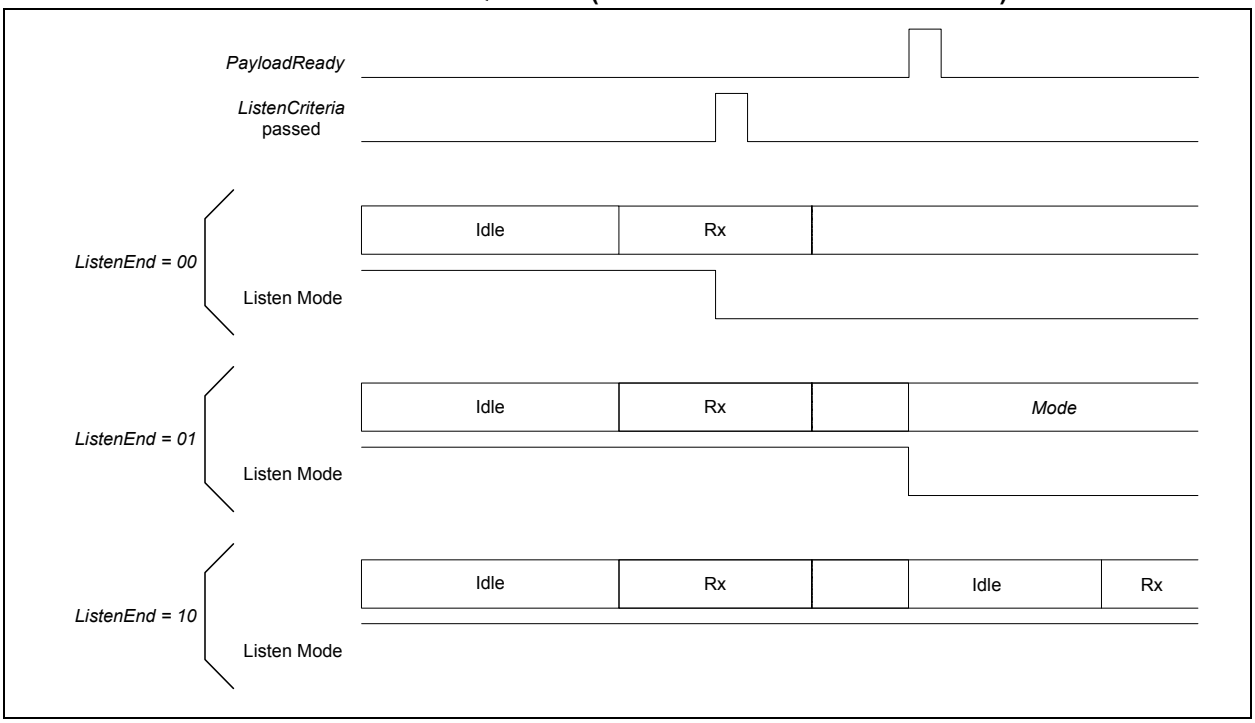
The action taken after detection of a packet is defined by ListenEnd in RegListen3 as described in Table 3-4.

TABLE 3-4: END OF LISTEN CYCLE ACTION

ListenEnd	Description
00	Chip stays in Rx mode. Listen mode stops and must be disabled.
01	Chip stays in Rx mode until *PayloadReady* or *Time-out* interrupt occurs. It then goes to the mode defined by *Mode*. Listen mode stops and must be disabled.
10	Chip stays in Rx mode until *PayloadReady* or *Time-out* interrupt occurs. Listen mode then resumes in Idle state. FIFO content is lost at next Rx wake-up.

Upon detection of a valid packet, the sequencing is altered as shown in Figure 3-5.

FIGURE 3-5: LISTEN MODE SEQUENCE (WANTED SIGNAL IS RECEIVED)



Listen mode can be disabled by writing ListenOn to '0'.

3.3.4 Stopping Listen Mode

To abort Listen mode operation, observe the following procedure:

- Program RegOpMode with ListenOn = 0, ListenAbort = 1 and the desired setting for the Mode bits (Sleep, Stdby, FS, Rx or Tx mode) in a single SPI access
- Program RegOpMode with ListenOn = 0, ListenAbort = 0 and the desired setting for the Mode bits (Sleep, Stdby, FS, Rx or Tx mode) in a second SPI access.

3.3.5 RC Timer Accuracy

All timings of the Listen mode rely on the accuracy of the internal low-power RC oscillator. This oscillator is automatically calibrated at the device power-up. This is a user-transparent process.

For applications enduring large temperature variations and for which the power supply is never removed, RC calibration can be performed on user request. RcCalStart in RegOsc1 is used to trigger this calibration and the flag RcCalDone automatically sets when the calibration is over.

3.4 Auto Modes

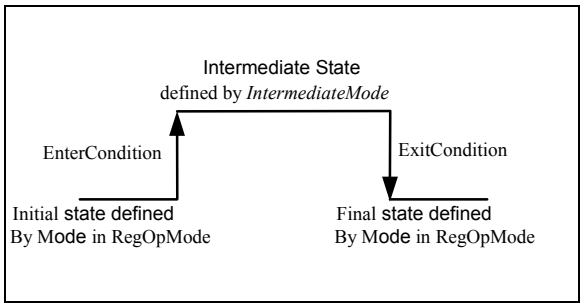
Automatic modes of packet handler can be enabled by configuring the related parameters in RegAutoModes.

The Intermediate mode of the chip is called *IntermediateMode* and the Enter and Exit conditions to and from this Intermediate mode can be configured through the parameters EnterCondition and ExitCondition.

The Enter and Exit conditions cannot be used independently of each other (i.e., both must be enabled at the same time).

The initial and the final state is the one configured in the mode in RegOpMode. The initial and final states can be different by configuring the Modes register while the chip is in Intermediate mode. The pictorial description of the AutoModes is shown in Figure 3-6.

FIGURE 3-6: AUTO MODES OF PACKET HANDLER



Some typical examples of AutoModes usage are described below:

- Automatic reception (AutoRx):
  - Mode = Rx
  - IntermediateMode = Sleep
  - EnterCondition = CrcOk
  - ExitCondition = falling edge of FifoNotEmpty

4.0 DATA PROCESSING

4.1 Overview

4.1.1 BLOCK DIAGRAM

Figure 4-1 illustrates the MRF39RA data processing circuit. Its role is to interface the data from the demodulator and the uC access points (SPI and DIO pins). It also controls all the Configuration registers.

The circuit contains several control blocks that are described in the following paragraphs.

The MRF39RA implements several data operation modes, each with their own data path through the data processing section. Depending on the data operation mode selected, some control blocks are active while others remain disabled.

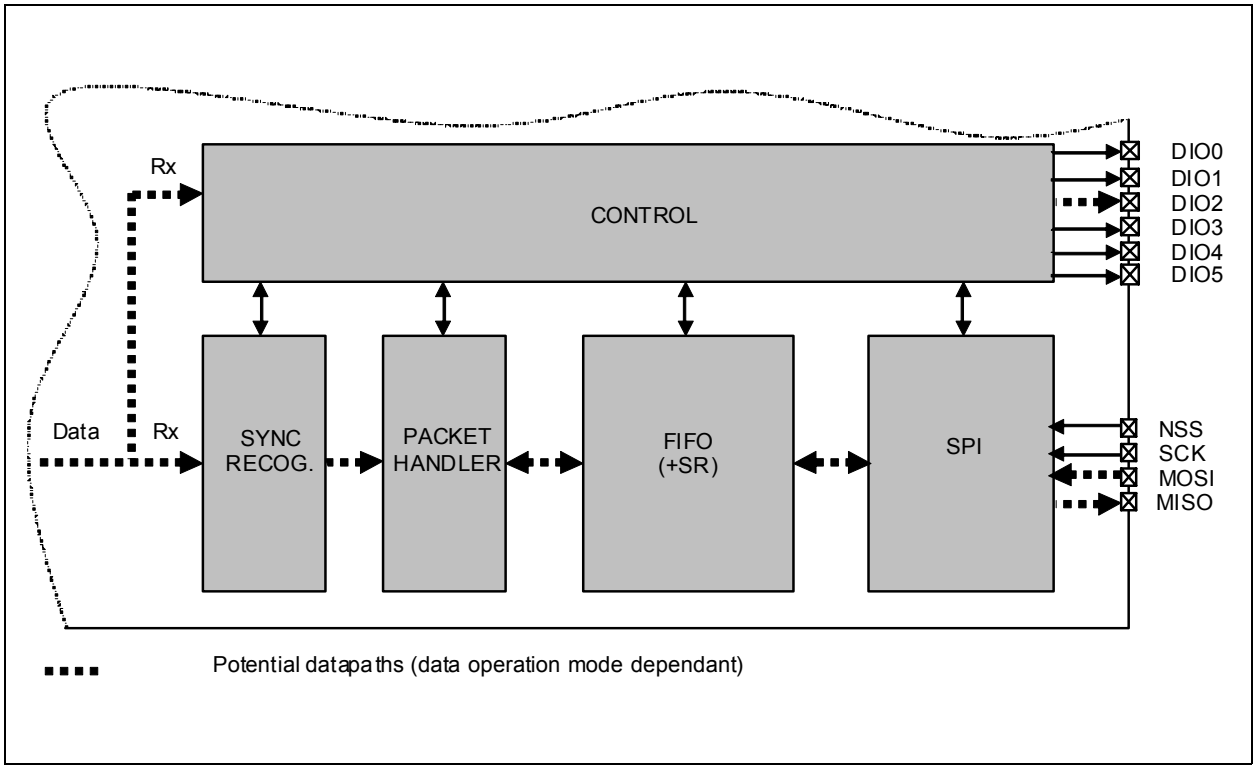
4.1.2 DATA OPERATION MODES

The MRF39RA has two different data operation modes that the user can select:

- **Continuous mode**: each received bit is accessed in real time at the DIO2/DATA pin. This mode may be used if adequate external signal processing is available.
- **Packet mode** (recommended): user only retrieves payload bytes from the FIFO. The packet engine automatically removes the preamble, checks the sync word, performs AES decryption, checks the CRC and decodes DC-free schemes, if enabled. The uC processing overhead is significantly reduced compared to Continuous mode. Depending on the optional features activated (CRC, AES, etc) the maximum payload length is limited to FIFO size, 255 bytes or unlimited.

Each of these data operation modes is fully described in the following sections.

FIGURE 4-1: MRF39RA DATA PROCESSING CONCEPTUAL VIEW



4.2 Control Block Description

4.2.1 SPI INTERFACE

The SPI interface gives access to the Configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/ Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

- **Single Access**: an address byte followed by a data byte is sent for a write access, whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte.
- **Burst Access**: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stays low between each byte. It goes high only after the last byte transfer.
- **FIFO access**: if the address byte corresponds to the address of the FIFO, then succeeding data byte contains the address of the FIFO. The address is not automatically incremented, but it is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stays low between each byte. It goes high only after the last byte transfer.

Figure 4-2 shows a typical SPI single access to a register.

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e., this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer always starts by the NSS pin going low. MISO is high-impedance when NSS is high.

The first byte is the address byte. It is made of:

- wnr bit, which is '1' for write access and '0' for read access
- 7 bits of address, MSB first

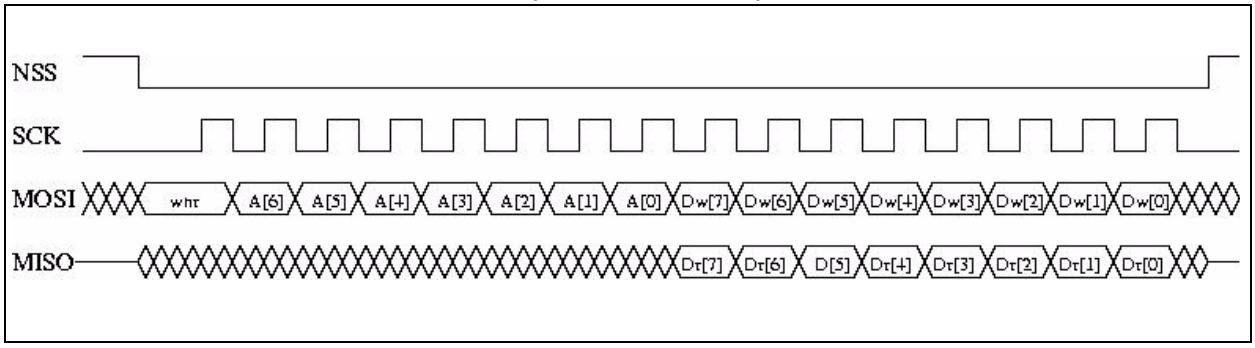
The second byte is a data byte, either sent on MOSI by the master in case of a write access, or received by the master on MISO in case of a read access. The data byte is transmitted MSB first.

Proceeding bytes may be sent on MOSI (for write access) or received on MISO (for read access) without rising NSS and re-sending the address. In FIFO mode, if the address was the FIFO address, then the bytes will is read at the FIFO address. In Burst mode, if the address was not the FIFO address, then it is automatically incremented at each new byte received.

The frame ends when NSS goes high. The next frame must start with an address byte. The Single Access mode is actually a special case of FIFO/Burst mode with only one data byte transferred.

During the write access, the byte transferred from the slave to the master on the MISO line is the value of the written register before the write operation.

FIGURE 4-2: SPI TIMING DIAGRAM (SINGLE ACCESS)



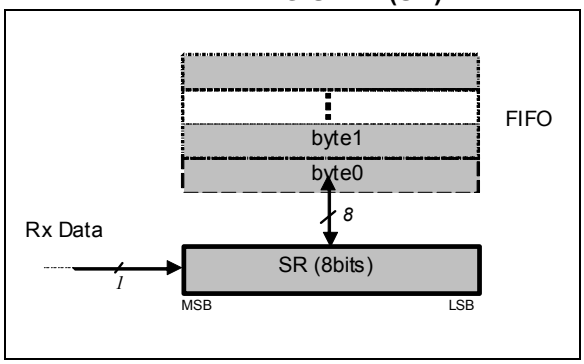
4.2.2 FIFO

4.2.2.1 Overview and Shift Register (SR)

In Packet mode of operation, received data is stored in a configurable FIFO (First In First Out) device. It is accessed via the SPI interface and provides several interrupts for transfer management.

The FIFO is 1-byte wide, hence it only performs byte (parallel) operations, whereas the demodulator functions serially. A Shift register is therefore employed to interface the two devices. In Rx the Shift register gets bit by bit data from the demodulator and writes these byte by byte to the FIFO as illustrated in Figure 4-3.

FIGURE 4-3: FIFO AND SHIFT REGISTER (SR)



Note: When switching to Sleep mode, only use the FIFO once the ModeReady flag is set (quasi immediate from all modes).

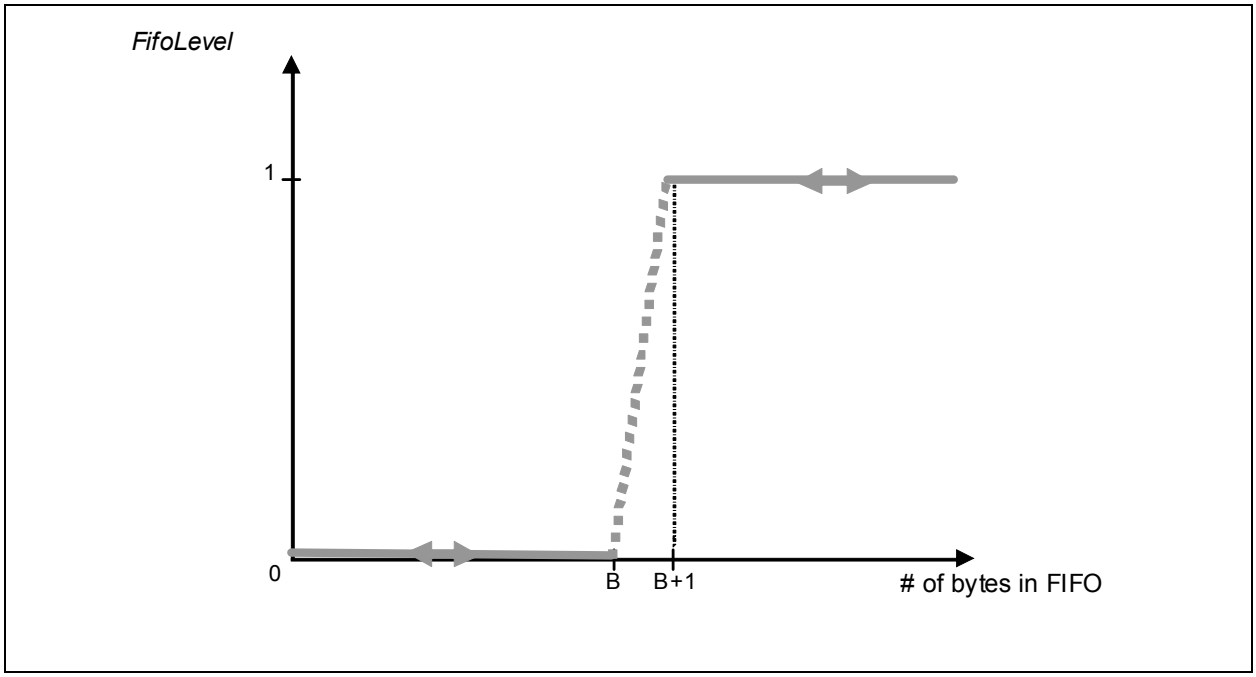
4.2.2.2 Size

The FIFO size is fixed to 66 bytes.

4.2.2.3 Interrupt Sources and Flags

- **FifoNotEmpty**: FifoNotEmpty interrupt source is low when byte 0 (i.e., whole FIFO, is empty). Otherwise it is high. Note that when retrieving data from the FIFO, FifoNotEmpty is updated on NSS falling edge (i.e., when FifoNotEmpty is updated to low state, the currently started read operation must be completed). In other words, FifoNotEmpty state must be checked after each read operation for a decision on the next one (FifoNotEmpty = `1`: more bytes to read; FifoNotEmpty = `0`: no more bytes to read).
- **FifoFull**: Fifofull interrupt source is high when the last FIFO byte (i.e., the whole FIFO, is full). Otherwise, it is low.
- **FifoOverrunFlag**: FifoOverrunFlag is set when a new byte is written by the SR while the FIFO is already full. Data is lost and the flag must be cleared by writing a '`1`', note that the FIFO is also be cleared.
- **FifoLevel**: Threshold is programmed by FifoThreshold in RegFifoThresh. Its behavior is illustrated in Figure 4-4.

FIGURE 4-4: FIFOLEVEL IRQ SOURCE BEHAVIOR



4.2.2.4 FIFO Clearing

Table 4-1 summarizes the status of the FIFO when switching between different modes.

TABLE 4-1: STATUS OF FIFO WHEN SWITCHING BETWEEN DIFFERENT MODES

From	To	FIFO status	Comments
Stdby	Sleep	Not cleared	
Sleep	Stdby	Not cleared	
Stdby/Sleep	Rx	Cleared	
Rx	Stdby/Sleep	Not cleared	To enable the user to read FIFO in Stdby/Sleep mode after Rx

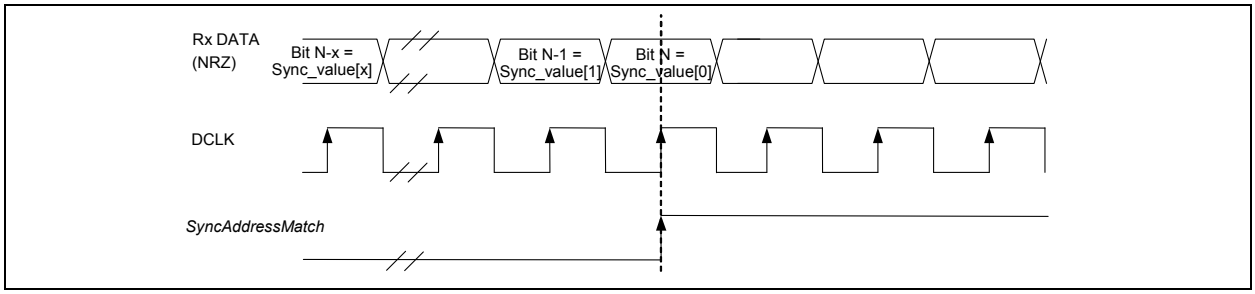
4.2.3 SYNC WORD RECOGNITION

4.2.3.1 Overview

Sync word recognition, also called pattern recognition, is activated by setting SyncOn in RegSyncConfig. The bit synchronizer must also be activated in Continuous mode (automatically done in Packet mode).

The block behaves like a Shift register; it continuously compares the incoming data with its internally programmed sync word and sets SyncAddressMatch when a match is detected as illustrated in Figure 4-5.

FIGURE 4-5: SYNC WORD RECOGNITION



During the comparison of the demodulated data, the first bit received is compared with bit 7 (MSB) of RegSyncValue1 and the last bit received is compared with bit 0 (LSB) of the last byte whose address is determined by the length of the sync word.

When the programmed sync word is detected, the user can assume that this incoming packet is for the node and can be processed accordingly.

SyncAddressMatch is cleared when leaving Rx or FIFO is emptied.

4.2.3.2 Configuration

- **Size**: sync word size is set from 1 to 8 bytes (i.e., 8 to 64 bits) via SyncSize in RegSyncConfig
- **Error tolerance**: the number of errors tolerated in the sync word recognition is set from 0 to 7 bits via SyncTol
- **Value**: the sync word value is configured in SyncValue(63:0)

Note:	SyncValue choices containing 0x00 bytes are not allowed.

4.2.4 PACKET HANDLER

The packet handler is the block used in Packet mode. Its functionality is fully described in **Section 4.5 "Packet Mode"**.

4.2.5 CONTROL

The control block configures and controls the full chip behavior according to the settings programmed in the Configuration registers.

4.3 Digital I/O Pins Mapping

Six general purpose I/O pins are available on the MRF39RA. Their configuration in Continuous or Packet mode is controlled through RegDioMapping1 and RegDioMapping2.

4.3.1 DIO PINS MAPPING IN CONTINUOUS MODE

TABLE 4-2: DIO MAPPING, CONTINUOUS MODE

Mode	Diox Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
Sleep	00	—	—	—	—	—	—
	01	—	—	—	—	—	—
	10	LowBat	LowBat	AutoMode	—	LowBat	LowBat
	11	ModeReady	—	—	—	—	ModeReady
Stdby	00	ClkOut	—	—	—	—	—
	01	—	—	—	—	—	—
	10	LowBat	LowBat	AutoMode	—	LowBat	LowBat
	11	ModeReady	—	—	—	—	ModeReady
FS	00	ClkOut	—	—	—	—	PllLock
	01	—	—	—	—	—	—
	10	LowBat	LowBat	AutoMode	—	LowBat	LowBat
	11	ModeReady	PllLock	—	—	PllLock	ModeReady
Rx	00	ClkOut	Timeout	Rssi	Data	Dclk	SyncAddress
	01	Rssi	RxReady	RxReady	Data	RxReady	Timeout
	10	LowBat	SyncAddress	AutoMode	Data	LowBat	Rssi
	11	ModeReady	PllLock	Timeout	Data	SyncAddress	ModeReady

4.3.2 DIO PINS MAPPING IN PACKET MODE

TABLE 4-3: DIO MAPPING, PACKET MODE

Mode	Diox Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
Sleep	00	—	—	FifoFull	FifoNotEmpty	FifoLevel	—
	01	—	—	—	—	FifoFull	—
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	—	—	AutoMode	—	—
Stdby	00	ClkOut	—	FifoFull	FifoNotEmpty	FifoLevel	—
	01	—	—	—	—	FifoFull	—
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	—	—	AutoMode	—	—
FS	00	ClkOut	—	FifoFull	FifoNotEmpty	FifoLevel	—
	01	—	—	—	—	FifoFull	—
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PllLock	PllLock	AutoMode	PllLock	PllLock
Rx	00	ClkOut	Timeout	FifoFull	FifoNotEmpty	FifoLevel	CrcOk
	01	Data	Rssi	Rssi	Data	FifoFull	Payload-Ready
	10	LowBat	RxReady	SyncAddress	LowBat	FifoNotEmpty	SyncAddress
	11	ModeReady	PllLock	PllLock	AutoMode	Timeout	Rssi

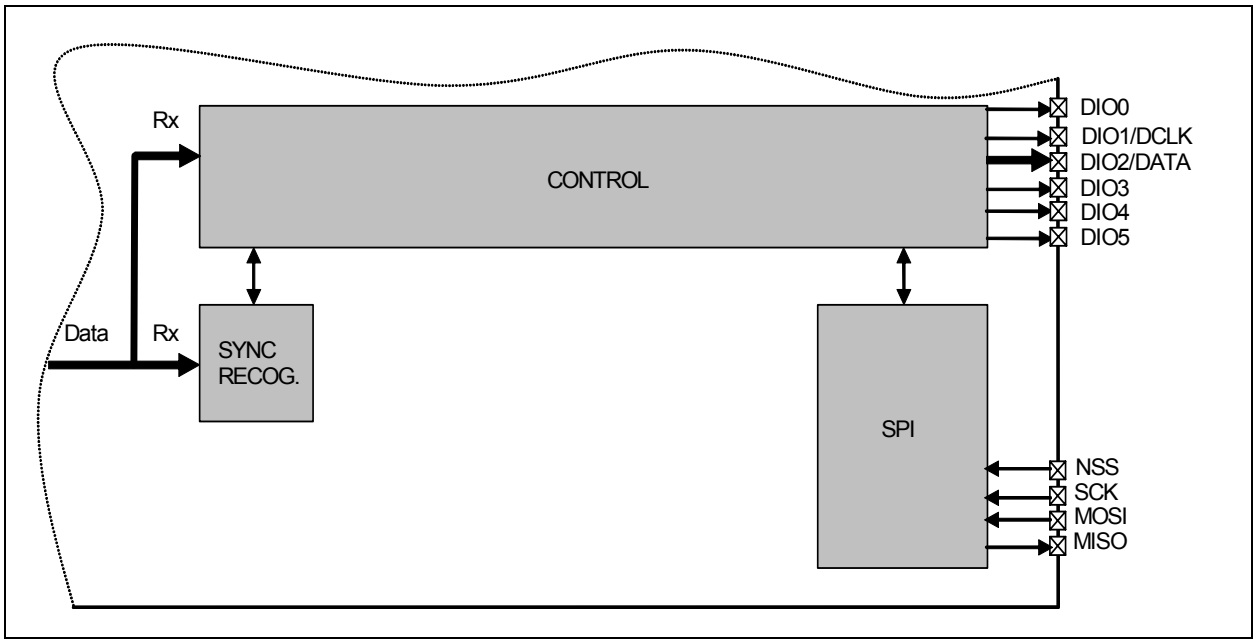
Note: Received data is only shown on the data signal between RxReady and PayloadReady's rising edges.

4.4 Continuous Mode

4.4.1 GENERAL DESCRIPTION

As illustrated in Figure 4-6, in Continuous mode, the NRZ data from the demodulator is directly accessed by the uC on the DIO2/DATA pin. The FIFO and packet handler are inactive.

FIGURE 4-6: CONTINUOUS MODE CONCEPTUAL VIEW

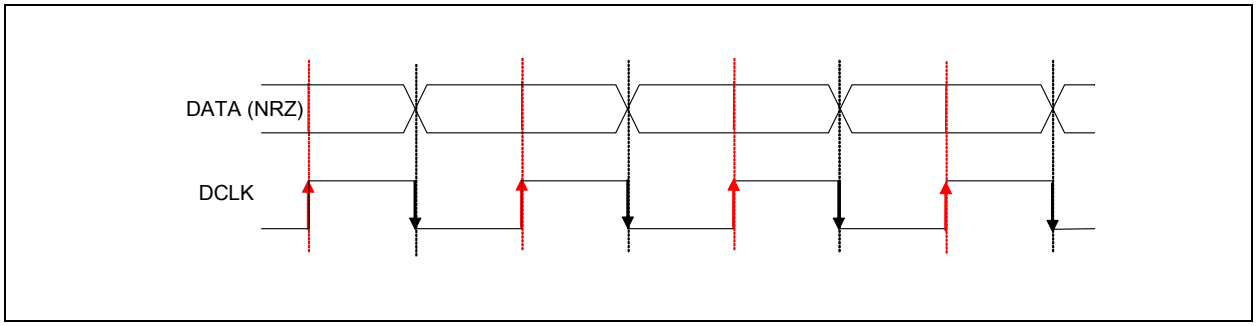


4.4.2 RX PROCESSING

If the bit synchronizer is disabled, the raw demodulator output is made directly available on DATA pin and no DCLK signal is provided.

Conversely, if the bit synchronizer is enabled, synchronous cleaned data and clock are made available on DIO2/DATA and DIO1/DCLK pins, respectively. DATA is sampled on the rising edge of DCLK and updated on the falling edge as illustrated in Figure 4-7.

FIGURE 4-7: RX PROCESSING IN CONTINUOUS MODE



Note: In Continuous mode it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the uC (bit synchronizer is automatically enabled in Packet mode).

4.5 Packet Mode

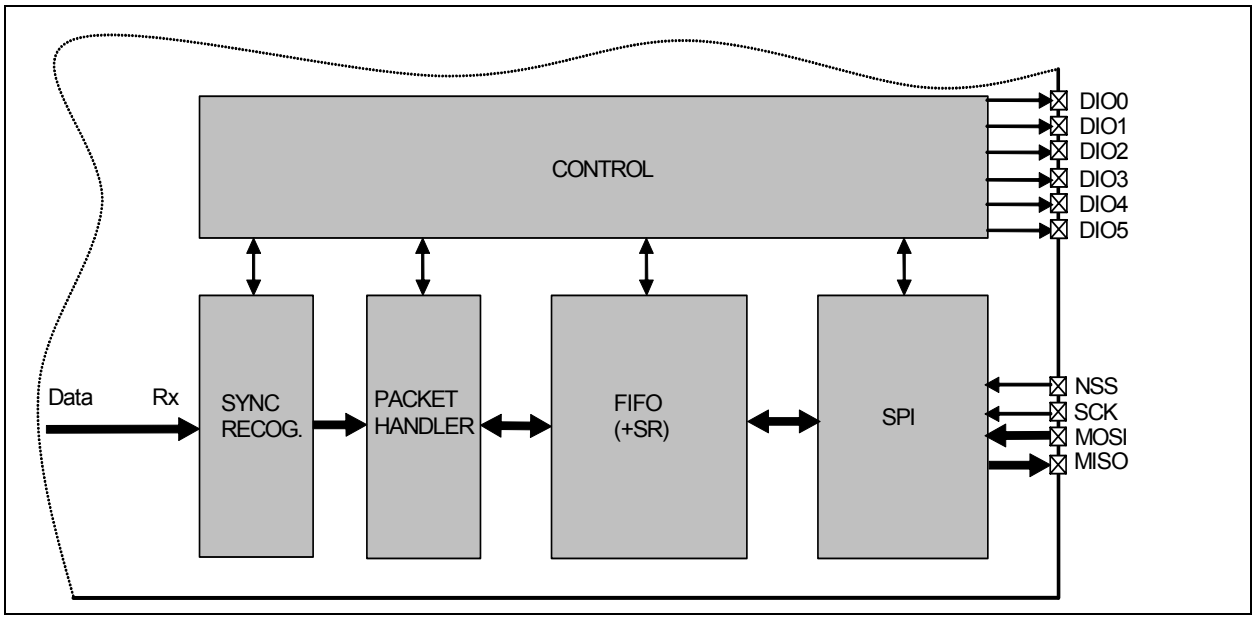
4.5.1 GENERAL DESCRIPTION

In Packet mode the NRZ data from the demodulator is not directly accessed by the uC, but stored in the FIFO and accessed via the SPI interface.

In addition, the MRF39RA packet handler performs several packet-oriented tasks such as preamble and sync word check, CRC check, de-whitening of data, Manchester decoding, address filtering, AES decryption, etc. This simplifies software and reduces uC overhead by performing these repetitive tasks within the RF chip itself.

Another important feature is ability to empty the FIFO in Sleep/Standby mode, ensuring optimum power consumption and adding more flexibility for the software.

FIGURE 4-8: PACKET MODE CONCEPTUAL VIEW



Note:	The bit synchronizer is automatically enabled in Packet mode.

4.5.2 PACKET FORMAT

4.5.2.1 Fixed Length Packet Format

Fixed length packet format is selected when bit PacketFormat is set to '0' and PayloadLength is set to any value greater than '0'.

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes must be programmed with the same packet length value.

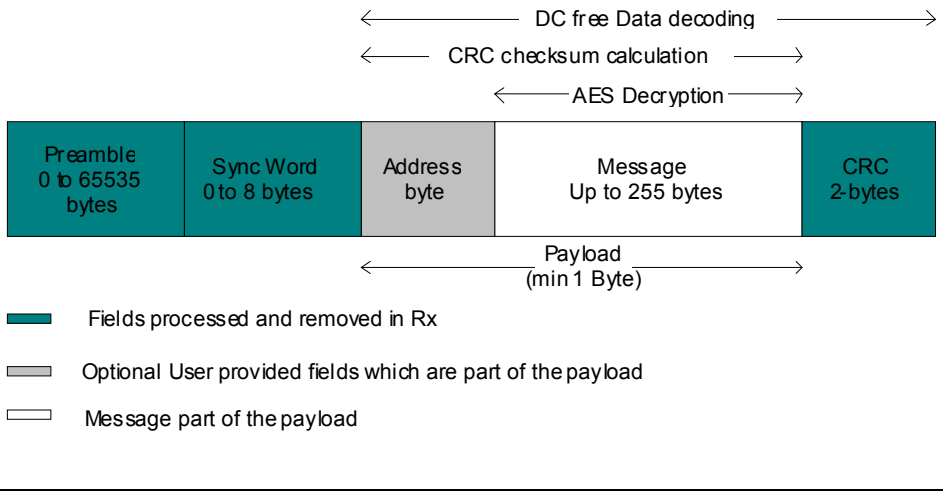
The length of the payload is limited to 255 bytes if AES is not enabled; otherwise, the message is limited to 64 bytes (i.e., maximum 65 bytes payload if Address byte is enabled).

The length programmed in PayloadLength relates only to the payload, which includes the message and the optional address byte. In this mode, the payload must contain at least one byte (i.e., address or message byte).

An illustration of a fixed length packet is shown in Figure 4-9, which contains the following fields:

- Preamble (1010...)
- Sync Word (Network ID)
- Optional Address Byte (Node ID)
- Message Data
- Optional 2-Byte CRC Checksum

FIGURE 4-9: FIXED LENGTH PACKET FORMAT



4.5.2.2 Variable Length Packet Format

Variable length packet format is selected when bit PacketFormat is set to '1'.

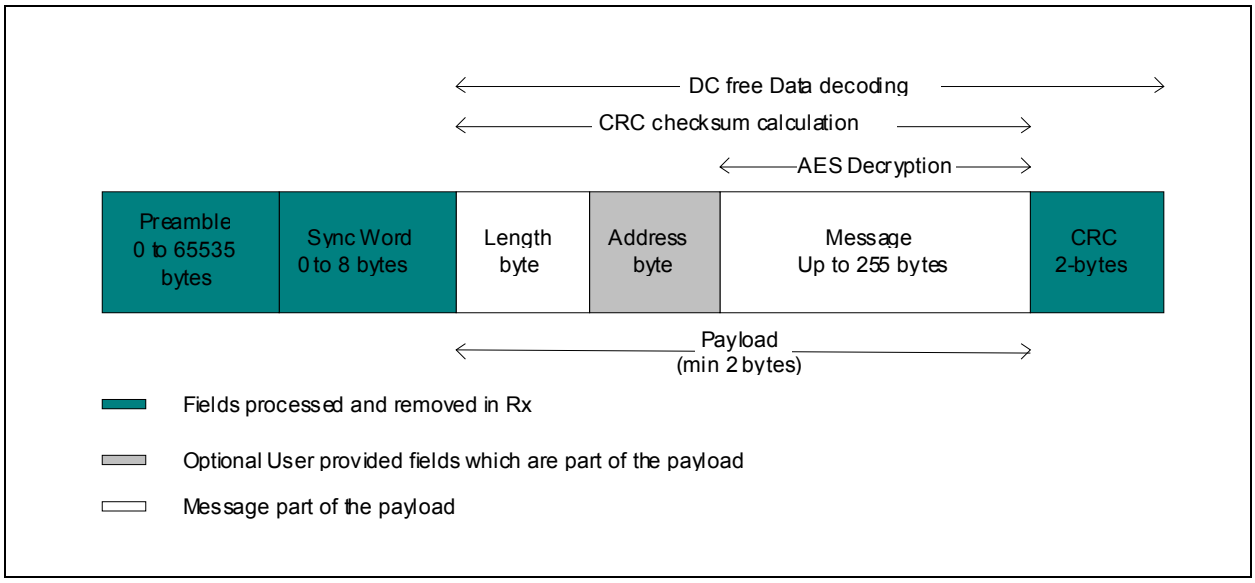
This mode is useful in applications where the length of the packet is not known in advance and can vary over time. It is necessary for the transmitter to send the length information together with each packet to enable the receiver to operate properly.

In this mode, the length of the payload indicated by the length byte is given by the first byte of the FIFO and is limited to 255 bytes if AES is not enabled; otherwise, the message is limited to 64 bytes (i.e., max 66 bytes payload, if address byte is enabled). Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least two bytes (i.e., length + address or message byte).

An illustration of a variable length packet is shown in Figure 4-10, which contains the following fields:

- Preamble (1010...)
- Sync Word (Network ID)
- Length Byte
- Optional Address Byte (Node ID)
- Message Data
- Optional 2-Byte CRC Checksum

FIGURE 4-10: VARIABLE LENGTH PACKET FORMAT



4.5.2.3 Unlimited Length Packet Format

Unlimited length packet format is selected when bit PacketFormat is set to '0' and PayloadLength is set to '0'.

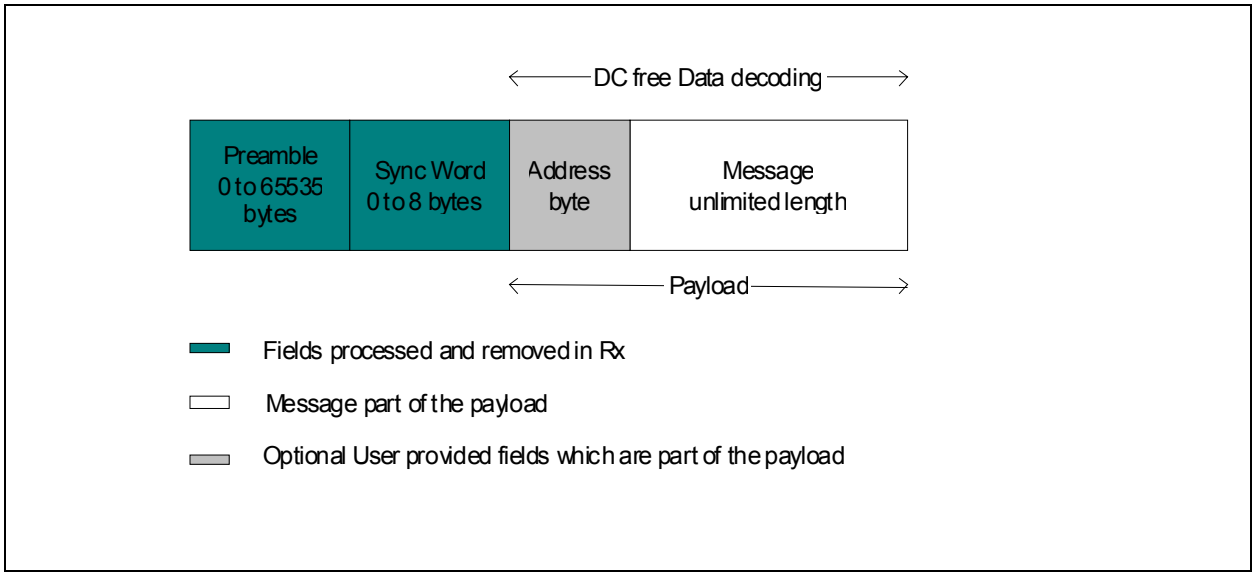
The user can receive packets of arbitrary length and PayloadLength register is not used in Rx modes for counting the length of the bytes received.

The data processing features such as address filtering, Manchester decoding and data de-whitening are unavailable if the sync pattern length is set to zero (SyncOn = '0'). The CRC detection is also not supported in this mode of the packet handler. Interrupts such as CrcOk and PayloadReady are unavailable either.

An unlimited length packet shown in Figure 4-11 contains the following fields:

- Preamble (1010...).
- Sync Word (Network ID).
- Optional Address Byte (Node ID).
- Message Data

FIGURE 4-11: UNLIMITED LENGTH PACKET FORMAT



4.5.3 PROCESSING (WITHOUT AES)

In Rx mode the packet handler extracts the user payload to the FIFO by performing the following operations:

- Receiving the preamble and stripping it off
- Detecting the sync word and stripping it off
- Optional DC-free decoding of data
- Optionally checking the address byte
- Optionally checking CRC and reflecting the result on CrcOk.

Only the payload (including optional address and length fields) is made available in the FIFO.

When the Rx mode is enabled the demodulator receives the preamble followed by the detection of sync word. If fixed length packet format is enabled, then the number of bytes received as the payload is given by the PayloadLength parameter.

In Variable Length mode, the first byte received after the sync word is interpreted as the length of the received packet. The internal length counter is initialized to this received length. The PayloadLength register is set to a value which is greater than the maximum expected length of the received packet. If the received length is greater than the maximum length stored in PayloadLength register, the packet is discarded; otherwise, the complete packet is received.

If the address check is enabled, then the second byte received in case of variable length and first byte in case of fixed length is the address byte. If the address matches the one in the NodeAddress field, reception of the data continues; otherwise, it is stopped. The CRC check is performed if CrcOn = `1` and the result is available in CrcOk, indicating that the CRC was successful. An interrupt (PayloadReady) is also generated on DIO0 as soon as the payload is available in the FIFO. The payload available in the FIFO can also be read in Sleep/Standby mode.

If the CRC fails, the PayloadReady interrupt is not generated and the FIFO is cleared. This function is overridden by setting CrcAutoClearOff = `1`, thus forcing the availability of the PayloadReady interrupt and the payload in the FIFO, even if the CRC fails.

4.5.4 AES

AES is the symmetric-key block cipher that provides the cryptographic capabilities to the receiver. The system proposed can work with 128-bit long fixed keys. The fixed key is stored in a 16-byte write-only user Configuration register, which retains its value in Sleep mode.

As shown in Figure 4-9 and Figure 4-10, the message part of the packet can be decrypted with the 128-cipher key stored in the Configuration registers.

4.5.4.1 Processing

The data received is stored in the FIFO. The address, CRC interrupts are generated as usual because these parameters were not encrypted.

As soon as the complete packet is received, the data is read from the FIFO, decrypted, and written back to FIFO. The PayloadReady interrupt is issued once the decrypted data is ready for reading in the FIFO via the SPI interface.

The AES decryption cannot be used on the fly (i.e., while receiving data). Thus, when AES decryption is enabled, the FIFO acts as a simple buffer. The decryption is only initiated when the complete packet is received in the buffer.

The decryption process takes approximately 7.0 µs per 16-byte block. For a maximum of four blocks (i.e., 64 bytes) it can take up to 28 µs for completing the cryptographic operations.

The receiver sees the AES decryption time as a sequential delay before the PayloadReady interrupt is available.

In Fixed Length mode, the message part of the payload that can be decrypted is 64-byte long. If the address filtering is enabled, the length of the payload must be at maximum 65 bytes in this case.

In Variable Length mode the maximum message size that can be decrypted is also 64 bytes whether address comparison is enabled or not. Thus, including length byte, the length of the payload is either 65 or 66 bytes maximum (the latter, when address comparison is enabled).

Crc check being performed on encrypted data, CrcOk interrupt occurs “decryption time” before *PayloadReady* interrupt.

4.5.5 HANDLING LARGE PACKETS

When Payload length exceeds FIFO size (66 bytes) whether in fixed, variable or unlimited length packet format, in addition to PayloadReady or CrcOk in Rx, the FIFO interrupts/flags can be used as follows:

FIFO must be unfilled on the fly during Rx to prevent FIFO overrun.

1. Start reading bytes from the FIFO when FifoNotEmpty or FifoThreshold becomes set.
2. Suspend reading from the FIFO if FifoNotEmpty clears before all bytes of the message have been read
3. Continue to step 1 until PayloadReady
4. Read all remaining bytes from the FIFO either in Rx or Sleep/Standby mode.

Note:	AES decryption is not feasible on large packets, since all Payload bytes need to be in the FIFO at the same time to perform decryption.

4.5.6 PACKET FILTERING

MRF39RA's packet handler offers several mechanisms for packet filtering, ensuring that only useful packets are made available to the uC, reducing significantly system power consumption and software complexity.

4.5.6.1 Sync Word-Based

Sync word filtering/recognition is used for identifying the start of the payload and also for network identification. As previously described, the sync word recognition block is configured (size, error tolerance, value) in RegSyncValue registers. This information is used to filter packets in Rx.

Every received packet which does not start with this locally configured sync word is automatically discarded and no interrupt is generated.

When the sync word is detected, payload reception automatically starts and SyncAddressMatch is asserted.

Note:	Sync word values containing 0x00 byte(s) are forbidden.

4.5.6.2 Address-Based

Address filtering can be enabled via the AddressFiltering bits. It adds another level of filtering above sync word (i.e., sync must match first), typically useful in a multi-node networks where a network ID is shared between all nodes (sync word) and each node has its own ID (address).

Two address-based filtering options are available:

1. AddressFiltering = `01`: Received address field is compared with internal register NodeAddress. If they match, then the packet is accepted and processed, otherwise it is discarded.
2. AddressFiltering = `10`: Received address field is compared with internal registers NodeAddress and BroadcastAddress. If either is a match, the received packet is accepted and processed, otherwise it is discarded. This additional check with a constant is useful for implementing broadcast in a multi-node networks.

As address filtering requires a sync word match, both features share the same interrupt flag SyncAddressMatch.

Note that the received address byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.

4.5.6.3 Length-Based

In variable length Packet mode, PayloadLength must be programmed with the maximum payload length permitted. If received length byte is smaller than this maximum, then the packet is accepted and processed, otherwise it is discarded.

Note that the received length byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.

To disable this function, the user must set the value of the PayloadLength to 255.

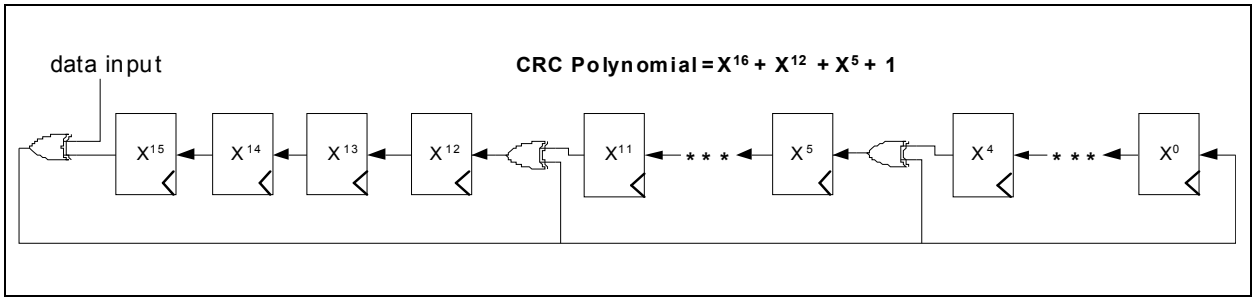
4.5.6.4 CRC-Based

The CRC check is enabled by setting bit CrcOn in RegPacketConfig1. It is used for checking the integrity of the message. The checksum is calculated on the received payload and compared with the two checksum bytes received. The result of the comparison is stored in bit CrcOk.

By default if the CRC check fails then the FIFO is automatically cleared and no interrupt is generated. This filtering function can be disabled via CrcAutoClearOff bit and in this case, even if CRC fails, the FIFO is not cleared and only PayloadReady interrupt goes high. Note that in both cases, the two CRC checksum bytes are stripped off by the packet handler and only the payload is made available in the FIFO.

The CRC is based on the CCITT polynomial, see Figure 4-12. This implementation also detects errors due to leading and trailing zeros.

FIGURE 4-12: CRC IMPLEMENTATION



4.5.7 DC-FREE DATA MECHANISMS

The received payload can be de-whitened or automatically Manchester-decoded in the MRF39RA packet handler.

Note:	Only one of the two methods must be enabled at a time.

4.5.7.1 Manchester Decoding

Manchester decoding is enabled if DcFree = `01` and it can only be used in Packet mode.

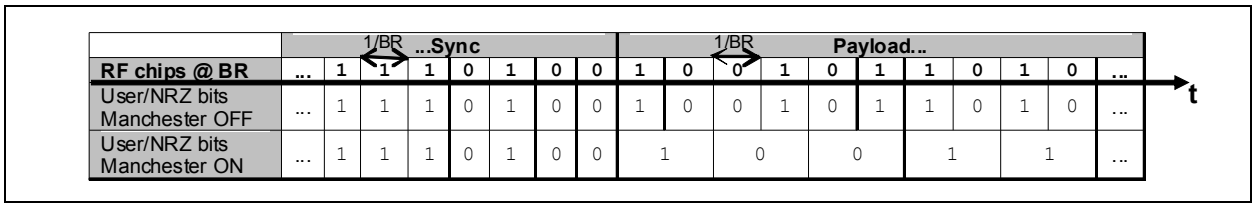
The Manchester data is decoded to NRZ code by decoding '`10`' as '`1`' and '`01`' as '`0`'.

In this case, the maximum chip rate is the maximum bit rate given in the specifications section, and the actual bit rate is half the chip rate.

Manchester decoding is only applied to the payload and CRC checksum while preamble and sync word are kept NRZ. However, the chip rate from preamble to CRC is the same and defined by BitRate in RegBitRate (Chip Rate = Bit Rate NRZ = 2 x Bit Rate Manchester).

Manchester decoding is thus made transparent for the user, who still retrieves NRZ data from the FIFO.

FIGURE 4-13: MANCHESTER DECODING



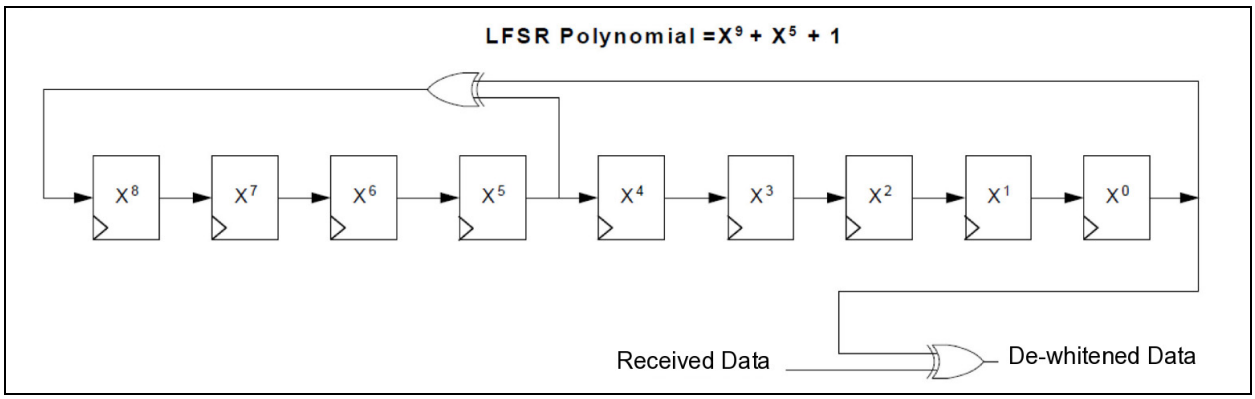
4.5.7.2 Data De-Whitening

Another technique called whitening or scrambling is widely used for randomizing the user data before radio transmission. The data is whitened using a random sequence on the Tx side and de-whitened on the Rx side using the same sequence. Compared to the Manchester technique it has the advantage of keeping the NRZ data rate (i.e., the actual bit rate is not halved).

The de-whitening process is enabled if DcFree = `10`. The data, including payload and 2-byte CRC checksum, is de-whitened by XORing it with a random sequence generated in a 9-bit LFSR as shown in Figure 4-14.

Payload de-whitening is thus made transparent for the user, who still retrieves NRZ data from the FIFO.

FIGURE 4-14: DATA DE-WHITENING



5.0 CONFIGURATION AND STATUS REGISTERS

5.1 General Description

TABLE 5-1: REGISTERS SUMMARY

Address	Register Name	Reset (Built-in)	Default (Recommended)	Description
0x00	RegFifo	0x00		FIFO read/write access
0x01	RegOpMode	0x04		Operating modes of the receiver
0x02	RegDataModul	0x00		Data Operation mode and modulation settings
0x03	RegBitrateMsb	0x1A		Bit rate setting; Most Significant bits
0x04	RegBitrateLsb	0x0B		Bit rate setting; Least Significant bits
0x05	Reserved05	0x00		—
0x06	Reserved06	0x52		—
0x07	RegFrfMsb	0xE4		RF carrier frequency; Most Significant bits
0x08	RegFrfMid	0xC0		RF carrier frequency; Intermediate bits
0x09	RegFrfLsb	0x00		RF carrier frequency; Least Significant bits
0x0A	RegOsc1	0x41		RC oscillators settings
0x0B	RegAfcCtrl	0x00		AFC control in low modulation index situations
0x0C	RegLowBat	0x02		Low battery indicator settings
0x0D	RegListen1	0x92		Listen mode settings
0x0E	RegListen2	0xF5		Listen mode Idle duration
0x0F	RegListen3	0x20		Listen mode Rx duration
0x10	RegVersion	0x23		Microchip ID relating the silicon revision
0x11	Reserved11	0x9F		—
0x12	Reserved12	0x09		—
0x13	Reserved13	0x1A		—
0x14	Reserved14	0x40		—
0x15	Reserved15	0xB0		—
0x16	Reserved16	0x7B		—
0x17	Reserved17	0x9B		—
0x18	RegLna	0x08	0x88	LNA settings
0x19	RegRxBw	0x86	0x55	Channel filter BW control
0x1A	RegAfcBw	0x8A	0x8B	Channel filter BW control during the AFC routine
0x1B	RegOokPeak	0x40		OOK demodulator selection and control in Peak mode
0x1C	RegOokAvg	0x80		Average threshold control of the OOK demodulator
0x1D	RegOokFix	0x06		Fixed threshold control of the OOK demodulator
0x1E	RegAfcFei	0x10		AFC and FEI control and status
0x1F	RegAfcMsb	0x00		MSB of the frequency correction of the AFC
0x20	RegAfcLsb	0x00		LSB of the frequency correction of the AFC
0x21	RegFeiMsb	0x00		MSB of the calculated frequency error
0x22	RegFeiLsb	0x00		LSB of the calculated frequency error
0x23	RegRssiConfig	0x02		RSSI-related settings
0x24	RegRssiValue	0xFF		RSSI value in dBm
0x25	RegDioMapping1	0x00		Mapping of pins DIO0 to DIO3
0x26	RegDioMapping2	0x05	0x07	Mapping of pins DIO4 and DIO5; ClkOut frequency

TABLE 5-1: REGISTERS SUMMARY (CONTINUED)

Address	Register Name	Reset (Built-in)	Default (Recommended)	Description
0x27	RegIrqFlags1	0x80		Status register: PLL lock state, time out, RSSI > Threshold
0x28	RegIrqFlags2	0x00		Status register: FIFO handling flags, low battery detection
0x29	RegRssiThresh	0xFF	0xE4	RSSI threshold control
0x2A	RegRxTimeout1	0x00		Time-out duration between Rx request and RSSI detection
0x2B	RegRxTimeout2	0x00		Time-out duration between RSSI detection and *PayloadReady*
0x2C	Reserved2C	0x00		—
0x2D	Reserved2D	0x03		—
0x2E	RegSyncConfig	0x98		Sync word recognition control
0x2F - 0x36	RegSyncValue1-8	0x00	0x01	Sync word bytes, 1 through 8
0x37	RegPacketConfig1	0x10		Packet mode settings
0x38	RegPayloadLength	0x40		Payload length setting
0x39	RegNodeAdrs	0x00		Node address
0x3A	RegBroadcastAdrs	0x00		Broadcast address
0x3B	RegAutoModes	0x00		Auto modes settings
0x3C	RegFifoThresh	0x0F	0x8F	FIFO threshold
0x3D	RegPacketConfig2	0x02		Packet mode settings
0x3E - 0x4D	RegAesKey1-16	0x00		16 bytes of the cypher key
0x4E	RegTemp1	0x01		Temperature Sensor control
0x4F	RegTemp2	0x00		Temperature readout
0x58	RegTestLna	0x1B		Sensitivity boost
0x59	RegTestTcxo	0x09		XTAL or TCXO input selection
0x5F	RegTestIlBw	0x08		PLL bandwidth setting
0x6F	RegTestDagc	0x00	0x30	Fading margin Improvement
0x71	RegTestAfc	0x00		AFC offset for low modulation index AFC
0x50 +	RegTest	—		Internal test registers

Note 1: Reset values are automatically refreshed in the chip at Power-on Reset.

2: Default values are the Microchip recommended register values, optimizing the device operation.

3: Registers for which the default value differs from the Reset value are denoted by an * in the tables of **Section 5.0 "Configuration and Status Registers"**.

5.2 Common Configuration Registers

TABLE 5-2: COMMON CONFIGURATION REGISTERS

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegFifo (0x00)	7-0	Fifo	rw	0x00	FIFO data output
RegOpMode (0x01)	7	SequencerOff	rw	0	Controls the automatic sequencer, see **Section 3.2 "Automatic Sequencer and Wake-up Times"**: 0 → Operating mode as selected with Mode bits in *RegOpMode* is automatically reached with the Sequencer 1 → Mode is forced by the user
	6	ListenOn	rw	0	Enables Listen mode; it must be enabled while in Standby mode: 0 → OFF (see **Section 3.3 "Listen Mode"**) 1 → ON
	5	ListenAbort	w	0	Aborts Listen mode when set together with *ListenOn* = 0 (see **Section 3.3.4 "Stopping Listen Mode"**) Always reads '0'
	4-2	Mode	rw	001	Receiver's operating modes: 000 → Sleep mode (SLEEP) 001 → Standby mode (STDBY) 010 → Frequency Synthesizer mode (FS) 100 → Receiver mode (RX) Others → Reserved Reads the value corresponding to the current chip mode
	1-0	—	r	00	Unused
RegDataModule (0x02)	7	—	r	0	Unused
	6-5	DataMode	rw	00	Data Processing mode: 00 → Packet mode 01 → Reserved 10 → Continuous mode with bit synchronizer 11 → Continuous mode without bit synchronizer
	4-3	ModulationType	rw	00	Modulation scheme: 00 → FSK 01 → OOK 10 - 11 → Reserved
	2-0	—	r	000	Unused
RegBitrateMsb (0x03)	7-0	BitRate(15:8)	rw	0X1A	MSB of bit rate (chip rate when Manchester encoding is enabled)
RegBitrateLsb (0x04)	7-0	BitRate(7:0)	rw	0X0B	LSB of bit rate (chip rate if Manchester encoding is enabled) $BitRate = \frac{FXOSC}{BitRate(15,0)}$ Default value: 4.8 kbps
Reserved05 (0x05)	7-0	—	r	0X00	Unused
Reserved06 (0x06)	7-0	—	r	0X52	Unused

TABLE 5-2: COMMON CONFIGURATION REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegFrfMsb (0x07)	7-0	Frf(23:16)	rw	0XE4	MSB of the RF local oscillator
RegFrfMid (0x08)	7-0	Frf(15:8)	rw	0XC0	Middle byte of the RF local oscillator
RegFrfLsb (0x09)	7-0	Frf(7:0)	rw	0x00	LSB of the RF local oscillator $Frf = Fstep \times Frf(23;0)$ Default value: Frf = 915 MHz (32 MHz XO)
RegOsc1 (0x0A)	7	RcCalStart	w	0	Triggers the calibration of the RC oscillator when set. Always reads '0'. RC calibration must be triggered in Standby mode.
	6	RcCalDone	r	1	0 → RC calibration in progress 1 → RC calibration is over
	5-0	—	r	000001	Unused
RegAfcCtrl (0x0B)	7-6	—	r	00	Unused
	5	AfcLowBetaOn	rw	0	Improved AFC routine for signals with modulation index lower than 2, see **Section 2.4.17 "Optimized Setup for Low Modulation Index Systems"**. 0 → Standard AFC routine 1 → Improved AFC routine
	4-0	—	r	00000	Unused
RegLowBat (0x0C)	7-5	—	r	000	Unused
	4	LowBatMonitor	rw	—	Real-time (not latched) output of the low battery detector, when enabled.
	3	LowBatOn	rw	0	Low Battery detector enable signal 0 → LowBat OFF 1 → LowBat ON
	2-0	LowBatTrim	rw	010	Trimming of the *LowBat* threshold: 000 → 1.695V 010 → 1.835V 100 → 1.976V 110 → 2.116V 001 → 1.764V 011 → 1.905V 101 → 2.045V 111 → 2.185V

TABLE 5-2: COMMON CONFIGURATION REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegListen1 (0x0D)	7-6	ListenResolIdle	rw	10	Resolution of Listen modes timings (calibrated RC osc): 0101 → 64 µs 1010 → 4.1 ms 1111 → 262 ms Others → Reserved
	5-4	ListenResolRx	rw	01	Resolution of Listen mode Rx time (calibrated RC osc): 00 → Reserved 01 → 64 µs 10 → 4.1 ms 11 → 262 ms
	3	ListenCriteria	rw	0	Criteria for packet acceptance in Listen mode: 0 → Signal strength is above *RssiThreshold* 1 → Signal strength is above *RssiThreshold* and *SyncAddress* matched
	2-1	ListenEnd	rw	01	Action taken after acceptance of a packet in Listen mode: 00 → Chip stays in Rx mode. Listen mode stops and must be disabled, see **Section 3.3 "Listen Mode"**. 01 → Chip stays in Rx mode until *PayloadReady* or *Time-out* interrupt occurs. It then goes to the mode defined by *Mode*. Listen mode stops and must be disabled, see **Section 3.3 "Listen Mode"**. 10 → Chip stays in Rx mode until *PayloadReady* or *Time-out* interrupt occurs. Listen mode then resumes in idle state. FIFO content is lost at next Rx wake-up. 11 → Reserved
	0	—	r	0	Unused
RegListen2 (0x0E)	7-0	ListenCoefIdle	rw	0xf5	Duration of the Idle phase in Listen mode. $t_{ListenIdle} = ListenCoefIdle \bullet ListenResolIdle$
RegListen3 (0x0F)	7-0	ListenCoefRx	rw	0x20	Duration of the Rx phase in Listen mode; start-up time included, see **Section 3.2.1 "Receiver Start-up Time"**. $t_{ListenRx} = ListenCoefRx \bullet ListenResolRx$
RegVersion (0x10)	7-0	Version	r	0x23	Version code of the chip. Bits 7-4 give the full revision number. Bits 3-0 give the metal mask revision number.

5.3 Receiver Registers

TABLE 5-3: RECEIVER REGISTERS

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
Reserved14 (0x14)	7-0	—	r	0x40	Unused
Reserved15 (0x15)	7-0	—	r	0xB0	Unused
Reserved16 (0x16)	7-0	—	r	0x7B	Unused
Reserved17 (0x17)	7-0	—	r	0x9B	Unused
RegLna (0x18)	7	LnaZin	rw	1*	LNA's input impedance 0 → 50 Ohms 1 → 200 Ohms
	6	—	r	0	Unused
	5-3	LnaCurrentGain	r	001	Current LNA gain set either manually or by the AGC
	2-0	LnaGainSelect	rw	000	LNA gain setting: 000 → Gain set by the internal AGC loop 001 → G1 = Highest gain 010 → G2 = Highest gain – 6 dB 011 → G3 = Highest gain – 12 dB 100 → G4 = Highest gain – 24 dB 101 → G5 = Highest gain – 36 dB 110 → G6 = Highest gain – 48 dB 111 → Reserved
RegRxBw (0x19)	7-5	DccFreq	rw	010*	Cut-off frequency of the DC offset canceler (DCC): $fc = \frac{4 \times RxBw}{2\pi \times 2^{DccFreq+2}}$ ~4% of the RxBw by default
	4-3	RxBwMant	rw	10 *	Channel filter bandwidth control: 00 → RxBwMant = 16 10 → RxBwMant = 24 01 → RxBwMant = 20 11 → Reserved
	2-0	RxBwExp	rw	101 *	Channel filter bandwidth control: FSK mode: $RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+2}}$ OOK mode: $RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+3}}$ See Table 2-3 for tabulated values.

TABLE 5-3: RECEIVER REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegAfcBw (0x1A)	7-5	DccFreqAfc	rw	100	*DccFreq* parameter used during the AFC
	4-3	RxBwMantAfc	rw	01	*RxBwMant* parameter used during the AFC
	2-0	RxBwExpAfc	rw	011*	*RxBwExp* parameter used during the AFC
RegOokPeak (0x1B)	7-6	OokThreshType	rw	01	Selects type of threshold in the OOK data slicer: 00 → Fixed 10 → Average 01 → Peak 11 → Reserved
	5-3	OokPeakTheshStep	rw	000	Size of each decrement of the RSSI threshold in the OOK demodulator: 000 → 0.5 dB 010 → 1.5 dB 100 → 3.0 dB 110 → 5.0 dB 001 → 1.0 dB 011 → 2.0 dB 101 → 4.0 dB 111 → 6.0 dB
	2-0	OokPeakThreshDec	rw	000	Period of decrement of the RSSI threshold in the OOK demodulator: 000 → Once per chip 001 → Once every two chips 010 → Once every four chips 011 → Once every eight chips 100 → Twice in each chip 101 → Four times in each chip 110 → Eight times in each chip 111 → 16 times in each chip
RegOokAvg (0x1C)	7-6	OokAverageThreshFilt	rw	10	Filter coefficients in Average mode of the OOK demodulator: 00 → f_C ≈ chip rate / 32.π 01 → f_C ≈ chip rate / 8.π 10 → f_C ≈ chip rate / 4.π 11 → f_C ≈ chip rate / 2.π
	5-0	—	r	000000	Unused
RegOokFix (0x1D)	7-0	OokFixedThresh	rw	0110 (6dB)	Fixed threshold value (in dB) in the OOK demodulator. Used when *OokThresType* = 00

TABLE 5-3: RECEIVER REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegAfcFei (0x1E)	7	—	r	0	Unused
	6	FeiDone	r	0	0 → FEI is on-going 1 → FEI finished
	5	FeiStart	w	0	Triggers a FEI measurement when set. Always reads '0'.
	4	AfcDone	r	1	0 → AFC is on-going 1 → AFC has finished
	3	AfcAutoclearOn	rw	0	Only valid if *AfcAutoOn* is set 0 → AFC register is not cleared before a new AFC phase 1 → AFC register is cleared before a new AFC phase
	2	AfcAutoOn	rw	0	0 → AFC is performed each time *AfcStart* is set 1 → AFC is performed each time Rx mode is entered
	1	AfcClear	w	0	Clears the *AfcValue* if set in Rx mode. Always reads '0'.
	0	AfcStart	w	0	Triggers an AFC when set. Always reads '0'.
RegAfcMsb (0x1F)	7-0	AfcValue(15:8)	r	0x00	MSB of the *AfcValue*, two's complement format
RegAfcLsb (0x20)	7-0	AfcValue(7:0)	r	0x00	LSB of the AfcValue, two's complement format *Frequency correction* = AfcValue x Fstep
RegFeiMsb (0x21)	7-0	FeiValue(15:8)	r	—	MSB of the measured frequency offset, two's complement
RegFeiLsb (0x22)	7-0	FeiValue(7:0)	r	—	LSB of the measured frequency offset, two's complement *Frequency error* = FeiValue x Fstep
RegRssiConfig (0x23)	7-2	—	r	000000	Unused
	1	RssiDone	r	1	0 → RSSI is on-going 1 → RSSI sampling is finished, result available
	0	RssiStart	w	0	Trigger a RSSI measurement when set. Always reads '0'.
RegRssiValue (0x24)	7-0	RssiValue	r	0xFF	Absolute value of the RSSI in dBm, 0.5 dB steps. RSSI = -RssiValue/2 [dBm]

5.4 IRQ and Pin Mapping Registers

TABLE 5-4: IRQ AND PIN MAPPING REGISTERS

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegDioMapping1 (0x25)	7-6	Dio0Mapping	rw	00	Mapping of pins DIO0 to DIO5 See Table 4-2 for mapping in Continuous mode See Table 4-3 for mapping in Packet mode
	5-4	Dio1Mapping	rw	00	
	3-2	Dio2Mapping	rw	00	
	1-0	Dio3Mapping	rw	00	
RegDioMapping2 (0x26)	7-6	Dio4Mapping	rw	00	
	5-4	Dio5Mapping	rw	00	
	3	—	r	0	Unused
	2-0	ClkOut	rw	111*	Selects CLKOUT frequency: 000 → FXOSC 001 → FXOSC/2 010 → FXOSC/4 011 → FXOSC/8 100 → FXOSC/16 101 → FXOSC/32 110 → RC (automatically enabled) 111 → OFF
RegIrqFlags1 (0x27)	7	ModeReady	r	1	Set when the operation mode requested in *Mode*, is ready - Sleep: Entering Sleep mode - Standby: XO is running - FS: PLL is locked - Rx: RSSI sampling starts Cleared when changing operating mode.
	6	RxReady	r	0	Set in Rx mode, after RSSI, AGC and AFC. Cleared when leaving Rx.
	5	—	r	0	Unused
	4	PllLock	r	0	Set (in FS and Rx) when the PLL is locked. Cleared when it is not.
	3	Rssi	rwc	0	Set in Rx when the *RssiValue* exceeds *RssiThreshold*. Cleared when leaving Rx.
	2	Timeout	r	0	Set when a time-out occurs (see *TimeoutRxStart* and *TimeoutRssiThresh*) Cleared when leaving Rx or FIFO is emptied.
	1	AutoMode	r	0	Set when entering Intermediate mode. Cleared when exiting Intermediate mode. Note that in Sleep mode a small delay can be observed between *AutoMode* interrupt and the corresponding Enter/Exit condition.
	0	SyncAddressMatch	r/rwc	0	Set when sync and address (if enabled) are detected. Cleared when leaving Rx or FIFO is emptied. This bit is read-only in Packet mode, rwc in Continuous mode.

TABLE 5-4: IRQ AND PIN MAPPING REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegIrqFlags2 (0x28)	7	FifoFull	r	0	Set when FIFO is full (i.e., contains 66 bytes), else cleared.
	6	FifoNotEmpty	r	0	Set when FIFO contains at least one byte, else cleared
	5	FifoLevel	r	0	Set when the number of bytes in the FIFO strictly exceeds *FifoThreshold*, else cleared.
	4	FifoOverrun	rwc	0	Set when FIFO overrun occurs. (except in Sleep mode) Flag(s) and FIFO are cleared when this bit is set. The FIFO then becomes immediately available for the next reception.
	3	—	r	0	Unused
	2	PayloadReady	r	0	Set in Rx when the payload is ready (i.e., last byte received and CRC is OK if enabled and *CrcAutoClearOff* is cleared). Cleared when FIFO is empty.
	1	CrcOk	r	0	Set in Rx when the CRC of the payload is OK. Cleared when FIFO is empty.
	0	LowBat	rwc	—	Set when the battery voltage drops below the low battery threshold. Only cleared when set by the user.
RegRssiThresh (0x29)	7-0	RssiThreshold	rw	0xE4*	RSSI trigger level for *Rssi* interrupt: - *RssiThreshold* / 2 [dBm]
RegRxTimeout1 (0x2A)	7-0	TimeoutRxStart	rw	0x00	*Time-out* interrupt is generated *TimeoutRxStart**16*T_{bit} after switching to Rx mode if *Rssi* interrupt does not occur (i.e., *RssiValue > RssiThreshold)* 0x00: *TimeoutRxStart* is disabled
RegRxTimeout2 (0x2B)	7-0	TimeoutRssiThresh	rw	0x00	*Time-out* interrupt is generated *TimeoutRssiThresh**16*T_{bit} after *Rssi* interrupt if *PayloadReady* interrupt does not occur. 0x00: *TimeoutRssiThresh* is disabled

5.5 Packet Engine Registers

TABLE 5-5: PACKET ENGINE REGISTERS

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
Reserved2C (0x2c)	7-0	—	rw	0x00	Unused
Reserved2D (0x2d)	7-0	—	rw	0x03	Unused
RegSyncConfig (0x2e)	7	SyncOn	rw	1	Enables the sync word detection: 0 → OFF 1 → ON
	6	FifoFillCondition	rw	0	FIFO filling condition: 0 → If *SyncAddress* interrupt occurs 1 → As long as *FifoFillCondition* is set
	5-3	SyncSize	rw	011	Size of the sync word: (*SyncSize* + 1) bytes
	2-0	SyncTol	rw	000	Number of tolerated bit errors in sync word
RegSyncValue1 (0x2f)	7-0	SyncValue(63:56)	rw	0x01*	First byte of sync word (MSB byte) Used if *SyncOn* is set.
RegSyncValue2 (0x30)	7-0	SyncValue(55:48)	rw	0x01*	Second byte of sync word Used if *SyncOn* is set and *(SyncSize +1)* >= 2.
RegSyncValue3 (0x31)	7-0	SyncValue(47:40)	rw	0x01*	Third byte of sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 3.
RegSyncValue4 (0x32)	7-0	SyncValue(39:32)	rw	0x01*	Forth byte of sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 4.
RegSyncValue5 (0x33)	7-0	SyncValue(31:24)	rw	0x01*	Fifth byte of sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 5.
RegSyncValue6 (0x34)	7-0	SyncValue(23:16)	rw	0x01*	Sixth byte of sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 6.
RegSyncValue7 (0x35)	7-0	SyncValue(15:8)	rw	0x01*	Seventh byte of sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 7.
RegSyncValue8 (0x36)	7-0	SyncValue(7:0)	rw	0x01*	Eighth byte of sync word. Used if *SyncOn* is set and *(SyncSize +1)* = 8.

TABLE 5-5: PACKET ENGINE REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegPacketConfig1 (0x37)	7	PacketFormat	rw	0	Defines the packet format used: 0 → Fixed length 1 → Variable length
	6-5	DcFree	rw	00	Defines DC-free decoding performed: 00 → None (OFF) 01 → Manchester 10 → Whitening 11 → Reserved
	4	CrcOn	rw	1	Enables CRC check: 0 → OFF 1 → ON
	3	CrcAutoClearOff	rw	0	Defines the behavior of the packet handler when CRC check fails: 0 → Clear FIFO and restart new packet reception. No *PayloadReady* interrupt issued. 1 → Do not clear FIFO. *PayloadReady* interrupt issued.
	2-1	AddressFiltering	rw	00	Defines address based filtering in Rx: 00 → None (OFF) 01 → Address field must match *NodeAddress* 10 → Must match *NodeAddress or BroadcastAddress* 11 → Reserved
	0	—	rw	0	Unused
RegPayloadLength (0x38)	7-0	PayloadLength	rw	0x40	If PacketFormat = 0 (fixed), payload length If PacketFormat = 1 (variable), max length in Rx
RegNodeAdrs (0x39)	7-0	NodeAddress	rw	0x00	Node address used in address filtering.
RegBroadcastAdrs (0x3A)	7-0	BroadcastAddress	rw	0x00	Broadcast address used in address filtering.

TABLE 5-5: PACKET ENGINE REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegAutoModes (0x3B)	7-5	EnterCondition	rw	000	Interrupt condition for entering the Intermediate mode: 000 → None (AutoModes OFF) 001 → Rising edge of *FifoNotEmpty* 010 → Rising edge of *FifoLevel* 011 → Rising edge of *CrcOk* 100 → Rising edge of *PayloadReady* 101 → Rising edge of *SyncAddress* 110 → Reserved 111 → Falling edge of *FifoNotEmpty* (i.e., FIFO empty)
	4-2	ExitCondition	rw	000	Interrupt condition for exiting the Intermediate mode: 000 → None (AutoModes OFF) 001 → Falling edge of *FifoNotEmpty* (i.e., FIFO empty) 010 → Rising edge of *FifoLevel* or *Timeout* 011 → Rising edge of *CrcOk* or *Timeout* 100 → Rising edge of *PayloadReady* or *Timeout* 101 → Rising edge of *SyncAddress* or *Timeout* 110 → Reserved 111 → Rising edge of *Timeout*
	1-0	IntermediateMode	rw	00	Intermediate mode: 00 → Sleep mode (SLEEP) 01 → Standby mode (STDBY) 10 → Receiver mode (RX) 11 → Reserved
RegFifoThresh (0x3C)	7	—	rw	1*	Unused
	6-0	FifoThreshold	rw	0001111	Used to trigger *FifoLevel* interrupt.
RegPacketConfig2 (0x3D)	7-4	InterPacketRxDelay	rw	0000	After *PayloadReady* occurred, defines the delay between FIFO empty and the start of a new RSSI phase for next packet. Must match the transmitter's PA ramp-down time. - Tdelay = 0 if *InterpacketRxDelay* >= 12 - Tdelay = $(2^{InterpacketRxDelay})/BitRate$ otherwise
	3	—	rw	0	Unused
	2	RestartRx	w	0	Forces the receiver in Wait mode, in Continuous Rx mode. Always reads '0'.
	1	AutoRxRestartOn	rw	1	Enables automatic Rx restart (RSSI phase) after *PayloadReady* occurred and packet is completely read from FIFO: 0 → OFF. *RestartRx* can be used. 1 → ON. Rx auto. restart after *InterPacketRxDelay*.
	0	AesOn	rw	0	Enable the AES decryption: 0 → OFF 1 → ON (payload limited to 66 bytes maximum)
RegAesKey1 (0x3E)	7-0	AesKey(127:120)	w	0x00	First byte of cipher key (MSB byte)
RegAesKey2 (0x3F)	7-0	AesKey(119:112)	w	0x00	Second byte of cipher key
RegAesKey3 (0x40)	7-0	AesKey(111:104)	w	0x00	Third byte of cipher key

TABLE 5-5: PACKET ENGINE REGISTERS (CONTINUED)

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegAesKey4 (0x41)	7-0	AesKey(103:96)	w	0x00	Forth byte of cipher key
RegAesKey5 (0x42)	7-0	AesKey(95:88)	w	0x00	Fifth byte of cipher key
RegAesKey6 (0x43)	7-0	AesKey(87:80)	w	0x00	Sixth byte of cipher key
RegAesKey7 (0x44)	7-0	AesKey(79:72)	w	0x00	Seventh byte of cipher key
RegAesKey8 (0x45)	7-0	AesKey(71:64)	w	0x00	Eighth byte of cipher key
RegAesKey9 (0x46)	7-0	AesKey(63:56)	w	0x00	Ninth byte of cipher key
RegAesKey10 (0x47)	7-0	AesKey(55:48)	w	0x00	Tenth byte of cipher key
RegAesKey11 (0x48)	7-0	AesKey(47:40)	w	0x00	Eleventh byte of cipher key
RegAesKey12 (0x49)	7-0	AesKey(39:32)	w	0x00	Twelfth byte of cipher key
RegAesKey13 (0x4A)	7-0	AesKey(31:24)	w	0x00	Thirteenth byte of cipher key
RegAesKey14 (0x4B)	7-0	AesKey(23:16)	w	0x00	Fourteenth byte of cipher key
RegAesKey15 (0x4C)	7-0	AesKey(15:8)	w	0x00	Fifteenth byte of cipher key
RegAesKey16 (0x4D)	7-0	AesKey(7:0)	w	0x00	Sixteenth byte of cipher key (LSB byte)

5.6 Temperature Sensor Registers

TABLE 5-6: TEMPERATURE SENSOR REGISTERS

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegTemp1 (0x4E)	7-4	—	r	0000	Unused
	3	TempMeasStart	w	0	Triggers the temperature measurement when set. Always reads '0'.
	2	TempMeasRunning	r	0	Set to '1' while the temperature measurement is running. Toggles back to '0' when the measurement is completed. The receiver cannot be used while measuring temperature
	1-0	—	r	01	Unused
RegTemp2 (0x4F)	7-0	TempValue	r	—	Measured temperature -1°C per Lsb Needs calibration for accuracy

5.7 Test Registers

TABLE 5-7: TEST REGISTERS

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegTestLna (0x58)	7-0	SensitivityBoost	rw	0x1B	High Sensitivity or Normal Sensitivity mode: 0x1B → Normal mode 0x2D → High Sensitivity mode
RegTestTcxo (0x59)	7-5	Reserved	rw	0x00	Reserved
	4	TcxoInputOn	rw	0x00	Controls the crystal oscillator 0 → Crystal oscillator with external crystal 1 → External clipped sine TCXO ac coupled to XTA pin
	3-0	Reserved	rw	0x09	Reserved
RegTestPIIBW (0x5F)	3-2	PIIBW	rw	0x02	PLL 3 dB BW setting 0x00 →75 kHz 0x01 →150 kHz 0x10 →300 kHz 0x11 →600 kHz
RegTestDagc (0x6F)	7-0	ContinuousDagc	rw	0x30 *	Fading Margin Improvement (see **Section 2.4.3 "Continuous-Time DAGC"**). 0x00 → Normal mode 0x20 → Improved margin, use if *AfcLowBetaOn=1* 0x30 → Improved margin, use if *AfcLowBetaOn=0*
RegTestAfc (0x71)	7-0	LowBetaAfcOffset	rw	0x00	AFC offset set for low modulation index systems, used if *AfcLowBetaOn* = 1. Offset = LowBetaAfcOffset x 488 Hz

6.0 APPLICATION INFORMATION

6.1 Crystal Resonator Specification

Table 6-1 shows the crystal resonator specification for the crystal reference oscillator circuit of the MRF39RA. This specification covers the full range of operation of the MRF39RA and is employed in the reference design.

TABLE 6-1: CRYSTAL SPECIFICATION

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
FXOSC	XTAL Frequency	—	26	—	32	MHz
RS	XTAL Serial Resistance	—	—	30	140	Ohms
C0	XTAL Shunt Capacitance	—	—	2.8	7	pF
CLOAD	External Foot Capacitance	On each pin XTA and XTB	8	16	22	pF

Note 1: The initial frequency tolerance, temperature stability and aging performance must be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.

2: The loading capacitance must be applied externally and adapted to the actual CLOAD specification of the XTAL.

3: A minimum XTAL frequency of 28 MHz is required to cover the 863-870 MHz band, 29 MHz for the 902-928 MHz band.

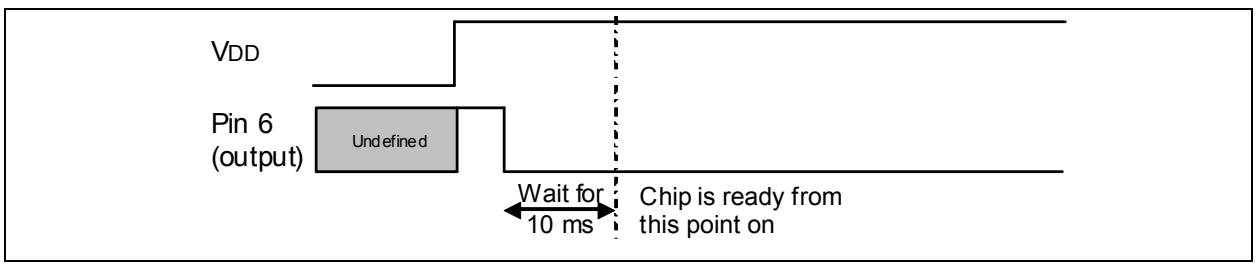
6.2 Reset of the Chip

A Power-on Reset of the MRF39RA is triggered at power-up. Additionally, a manual Reset can be issued by controlling pin 6.

6.2.1 POR

If the application requires the disconnection of V_{DD} from the MRF39RA, despite the extremely low Sleep mode current, the user must wait for 10 ms from the end of the POR cycle before commencing communications over the SPI bus. Pin 6 ($\overline{RESET}$) must be left floating during the POR sequence.

FIGURE 6-1: POR TIMING DIAGRAM

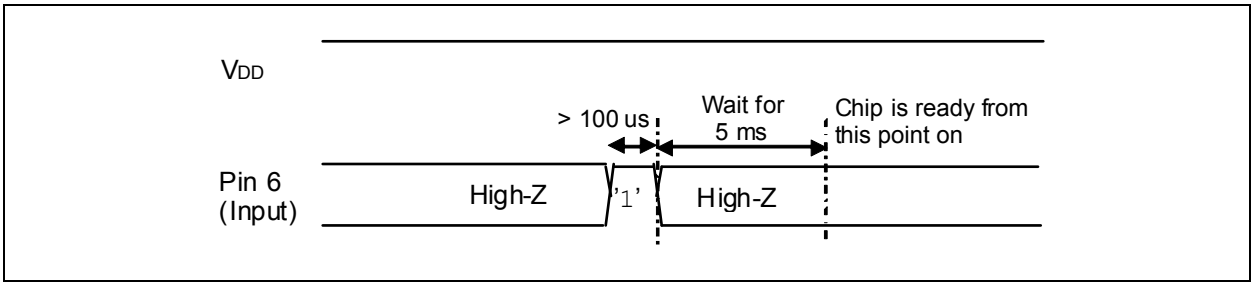


Note that any CLKOUT activity is also used to detect that the chip is ready.

6.2.2 MANUAL RESET

A manual Reset of the MRF39RA is possible even for applications in which VDD cannot be physically disconnected. Pin 6 must be pulled high for 100 µs and then released. The user must wait for 5 ms before using the chip.

FIGURE 6-2: MANUAL RESET TIMING DIAGRAM



Note:	While pin 6 is driven high, an overcurrent consumption of up to 10 mA can be seen on VDD.

6.3 Reference Design

Contact the Microchip representative for evaluation tools, reference designs and design assistance. Note that all schematics shown in this section are full schematics, listing all required components, including decoupling capacitors.

FIGURE 6-3: APPLICATION SCHEMATIC

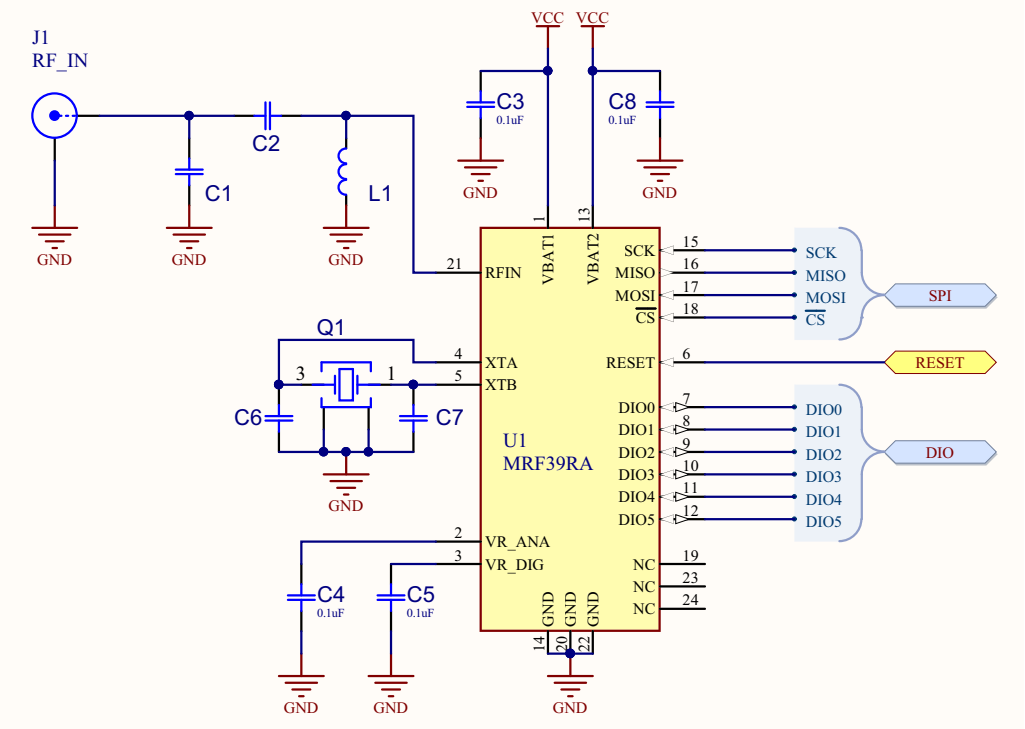


TABLE 6-2: REFERENCE BILL OF MATERIALS

Designator	315 MHz	433 MHz	868 MHz	915 MHz	Type
C3, C4, C5, C8	100 nF				X7R
C6, C7	15 pF				COG
L1	39 nH	33 nH	120 nH	120 nH	Wirewound air core or multilayer (1)
C1	—	—	5.6 pF	5.6 pF	COG
C2	12 pF	12 pF	6.8 nH (2)	5.6 nH (2)	See above (L or C)

Note 1: Inductor values may change when using multilayer type components.

2: An additional DC-cut capacitor (typ. 47 pF) may be required with this matching topology and DC grounded antennas.

7.0 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings(†)

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

TABLE 7-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Max.	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	°C
Tj	Junction temperature	—	+125	°C
Pmr	RF Input Level	—	+6	dBm

7.2 Operating Range

Table 7-2 shows the operating range.

TABLE 7-2: OPERATING RANGE

Symbol	Description	Min.	Max.	Unit
VDDop	Supply voltage	1.8	3.6	V
Top	Operational temperature range	-40	+85	°C
Clop	Load capacitance on digital ports	—	25	pF
ML	RF Input Level	—	0	dBm

7.3 ESD Notice

MRF39RA is a high-performance radio frequency device:

- Class 2 of the JEDEC® standard JESD22-A114-B (Human Body Model) on all pins
- Class B of the JEDEC standard JESD22-A115-A (Machine Model) on all pins
- Class IV of the JEDEC standard JESD22-C101C (Charged Device Model) on pins 2, 3, 21, 23, 24, Class III on all other pins.

It must be handled with all the necessary ESD precautions to avoid any permanent damage.

7.4 Device Specification

The tables below give the electrical specifications of the receiver under the following conditions:

- Supply voltage VBAT1 = VBAT2 = V_{DD} = 3.3V
- Temperature = 25°C
- FXOSC = 32 MHz
- FRF = 915 MHz
- 2-level FSK modulation without pre-filtering
- Bit Rate = 4.8 kbps and terminated in a matched 50-Ohm impedance, unless otherwise specified.

Note: Unless otherwise specified, the performance in the other frequency bands is similar or better.

7.4.1 POWER CONSUMPTION

Table 7-3 shows the power consumption specification.

TABLE 7-3: POWER CONSUMPTION SPECIFICATION

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
IDDSL	Supply current in Sleep mode	—	—	0.1	1	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	—	1.2	—	uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	—	1.25	1.5	mA
IDDFS	Supply current in Synthesizer mode	—	—	9	—	mA
IDDR	Supply current in Receive mode	—	—	16	—	mA

7.4.2 FREQUENCY SYNTHESIS

Table 7-4 shows the frequency synthesizer specification.

TABLE 7-4: FREQUENCY SYNTHESIZER SPECIFICATION

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
FR	Synthesizer frequency range	Programmable	290 424 862	— — —	340 510 1020	MHz MHz MHz
FXOSC	Crystal oscillator frequency	See **Section 6.1 "Crystal Resonator Specification"**	—	32	—	MHz
TS_OSC	Crystal oscillator wake-up time		—	250	500	µs
TS_FS	Frequency synthesizer wake-up time to PllLock signal	From Standby mode	—	80	150	µs
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	— — — — — — —	20 20 50 50 80 80 80	— — — — — — —	µs µs µs µs µs µs µs
FSTEP	Frequency synthesizer step	FSTEP = FXOSC/2^{19}	—	61.0	—	Hz
FRC	RC Oscillator frequency	After calibration	—	62.5	—	kHz
BRF	Bit rate, FSK	Programmable	1.2	—	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	—	32.768	kbps

7.4.3 RECEIVER

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in RegRxBw, receiving a PN15 sequence with a BER of 0.1% (bit synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, by setting bit LnaZin in RegLna to '1'. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the blocking immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level. Table 7-5 shows the receiver specification.

TABLE 7-5: RECEIVER SPECIFICATION

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
RFS_F	FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kbps FDA = 5 kHz, BR = 4.8 kbps FDA = 40 kHz, BR = 38.4 kbps	— — —	-118 -114 -105	— — —	dBm dBm dBm
		FDA = 5 kHz, BR = 1.2 kbps(1)	—	-120	—	dBm
RFS_O	OOK sensitivity, highest LNA gain	BR = 4.8 kbps	—	-112	-109	dBm
CCR	Co-channel rejection	—	-13	-10	—	dB
ACR	Adjacent channel rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	— 37	42 42	— —	dB dB
BI	Blocking immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	— — —	66 71 79	— — —	dB dB dB
	Blocking immunity Wanted signal at sensitivity +16 dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	— — —	62 65 73	— — —	dB dB dB
AMR	AM Rejection, AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	— — —	66 71 79	— — —	dB dB dB
IIP2	Second order input intercept point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	— —	+75 +35	— —	dBm dBm
IIP3	Third order input intercept point Unwanted tones are 1 MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	— -23	+20 -18	— —	dBm dBm
BW_SSB	Single side channel filter BW	Programmable	2.6	—	500	kHz
IMR_OOK	Image rejection in OOK mode	Wanted signal level = -106 dBm	27	30	—	dB
TS_RE	Receiver wake-up time, from PLL locked state to *RxReady*	RxBw = 10 kHz, BR = 4.8 kbps RxBw = 200 kHz, BR = 100 kbps	— —	1.7 96	— —	ms µs
TS_RE_AGC	Receiver wake-up time, from PLL locked state, AGC enabled	RxBw= 10 kHz, BR = 4.8 kbps RxBw = 200 kHz, BR = 100 kbps	—	3.0 163	—	ms µs
TS_RE_AGC&AFC	Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw= 10 kHz, BR = 4.8 kbs RxBw = 200 kHz, BR = 100 kbs	—	4.8 265	—	ms µs

Note 1: Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver.

TABLE 7-5: RECEIVER SPECIFICATION (CONTINUED)

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
TS_FEI	FEI sampling time	Receiver is ready	—	$4.T_{bit}$	—	—
TS_AFC	AFC response time	Receiver is ready	—	$4.T_{bit}$	—	—
TS_RSSI	RSSI response time	Receiver is ready	—	$2.T_{bit}$	—	—
DR_RSSI	RSSI dynamic range	AGC enabled Min. Max.	 — —	 -115 0	 — —	 dBm dBm

Note 1: Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver.

7.4.4 DIGITAL SPECIFICATION

Table 7-6 shows the digital specification.

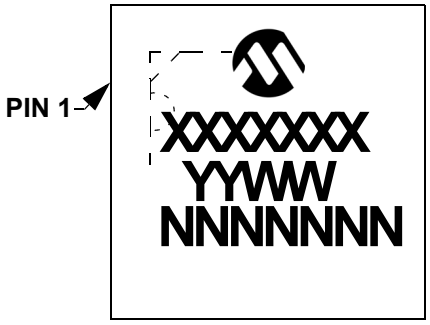
TABLE 7-6: DIGITAL SPECIFICATION

Operating Conditions (unless otherwise specified) Temperature: 25°C, V_{DD} = 3.3V, FXOSC = 32 MHz						
Symbol	**Description**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
V_{IH}	Digital input level high	—	0.8	—	—	V_{DD}
V_{IL}	Digital input level low	—	—	—	0.2	V_{DD}
V_{OH}	Digital output level high	I_{MAX} = 1 mA	0.9	—	—	V_{DD}
V_{OL}	Digital output level low	I_{MAX} = -1 mA	—	—	0.1	V_{DD}
F_{SCK}	SCK frequency	—	—	—	10	MHz
t_{ch}	SCK high time	—	50	—	—	ns
t_{cl}	SCK low time	—	50	—	—	ns
t_{rise}	SCK rise time	—	—	5	—	ns
t_{fall}	SCK fall time	—	—	5	—	ns
t_{setup}	MOSI setup time	From MOSI change to SCK rising edge	30	—	—	ns
t_{hold}	MOSI hold time	From SCK rising edge to MOSI change	60	—	—	ns
t_{nsetup}	NSS setup time	From NSS falling edge to SCK rising edge	30	—	—	ns
t_{nhold}	NSS hold time	From SCK falling edge to NSS rising edge, Normal mode	100	—	—	ns
t_{nhigh}	NSS high time between SPI accesses	—	20	—	—	ns
T_DATA	DATA hold and setup time	—	250	—	—	ns

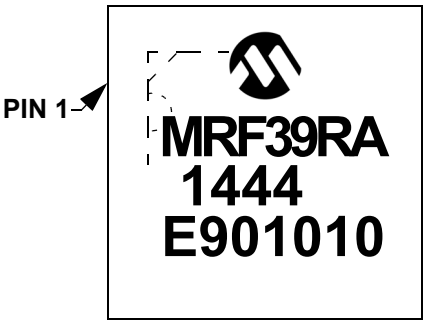
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

24-Lead QFN (5x5x0.9 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

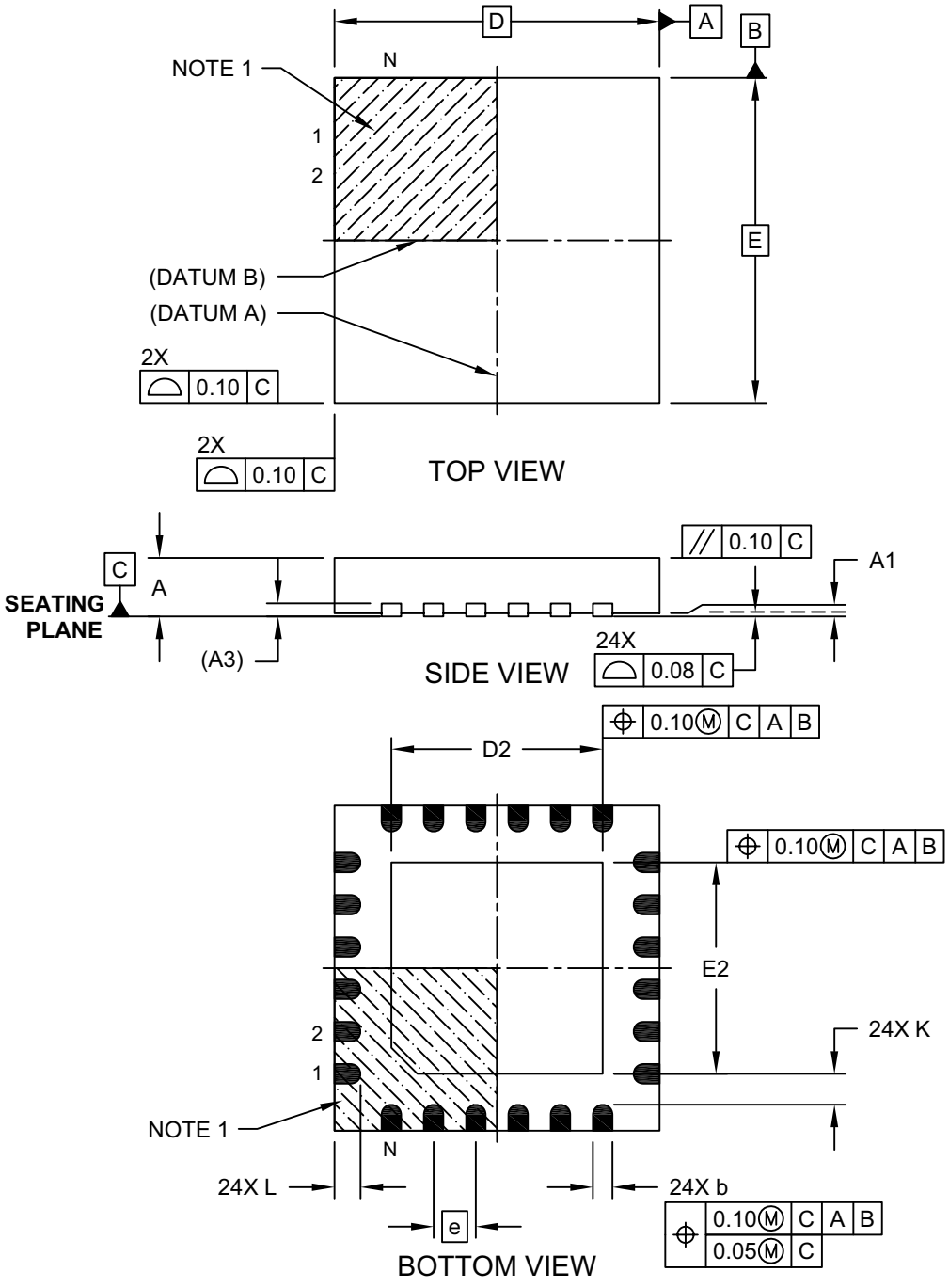
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8.2 Package Details

The following sections give the technical details of the packages.

24-Lead Plastic Quad Flat, No Lead Package (LY) – 5x5x1.0 mm Body [QFN or VQFN]

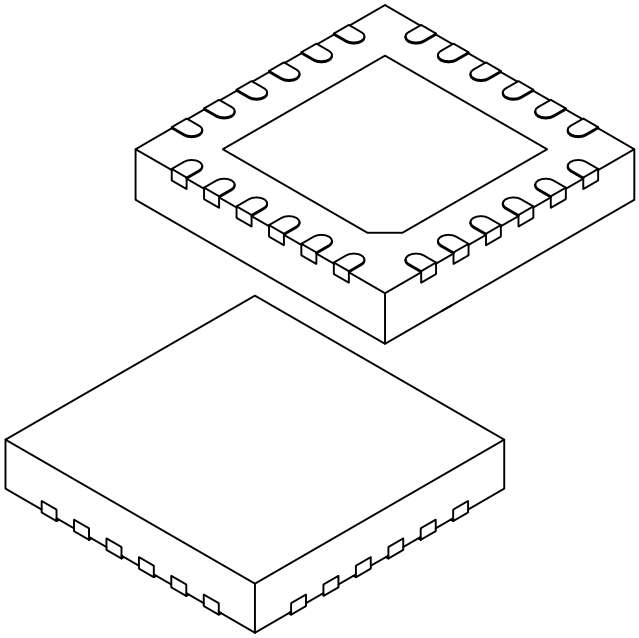
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-364A Sheet 1 of 2

24-Lead Plastic Quad Flat, No Lead Package (LY) – 5x5x1.0 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.20	3.25	3.30
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.20	3.25	3.30
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

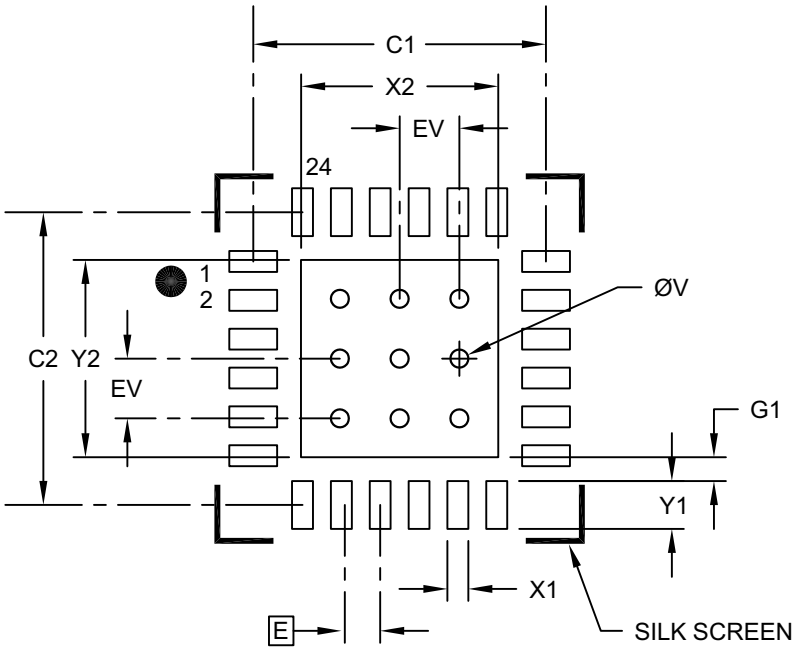
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-364A Sheet 2 of 2

24-Lead Plastic Quad Flat, No Lead Package (LY) – 5x5x1.0 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Center Pad Width	X2			3.30
Center Pad Length	Y2			3.30
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X24)	X1			0.35
Contact Pad Length (X24)	Y1			0.80
Contact Pad to Center Pad (X24)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2364A

8.3 Thermal Impedance

The thermal impedance of this package is: Theta ja = 23.8°C/W typ., calculated from a package in still air, on a 4-layer FR4 PCB as per the JEDEC® standard.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision A (December 2014)

Initial release of this document.

Revision B (June 2015)

- Updated Figure 4-14 and renamed title from Data Whitening to "Data De-Whitening"
- Updated Figure 6-3 Application Schematic
- Corrected Product Identification System table to update the example part number from MRF39RA-I/LY to “MRF39RAT-I/LY”
- Removed Section 8.4 “Ordering Information”.

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PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	MRF39RA	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I	= -40°C to +85°C (Industrial)
Package:(2)	LY	= QFN
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) MRF39RAT - I/LY
Industrial temperature,
QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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