Quad, 16-Bit DAC with 5 ppm/°C On-Chip Reference in 14-Lead TSSOP

AD5666-EP

FEATURES

Enhanced product features
- **Supports defense and aerospace applications (AQEC)**
- **Military temperature range (−55°C to +125°C)**
- **Controlled manufacturing baseline**
- **One assembly/test site**
- **One fabrication site**
- **Enhanced product change notification**
- **Qualification data available on request**

Low power, quad 16-bit DAC
14-lead TSSOP
On-chip 1.25 V/2.5 V, 5 ppm/°C reference
Power down to 400 nA at 5 V, 200 nA at 3 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on reset to zero scale or midscale
3 power-down functions
Hardware $\overline{\text{LDAC}}$ with $\overline{\text{LDAC}}$ override function
$\overline{\text{CLR}}$ function to programmable code
SDO daisy-chaining option
Rail-to-rail operation

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

GENERAL DESCRIPTION

The AD5666-EP is a low power, quad 16-bit, buffered voltage-output DAC. The part operates from a single 2.7 V to 5.5 V supply and is guaranteed monotonic by design.

The AD5666-EP has an on-chip reference with an internal gain of 2. The AD5666-EP-2 has a 2.5 V, 5 ppm/°C reference, giving a full-scale output of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is turned on by writing to the DAC.

The part incorporates a power-on reset circuit that ensures that the DAC output powers up to 0 V (POR pin low) or to midscale (POR pin high) and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode for any or all DAC channels.

The outputs of all DACs can be updated simultaneously using the $\overline{\text{LDAC}}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{\text{CLR}}$ that clears all DACs to a software-selectable code—0 V, midscale, or full scale.

The AD5666-EP uses a versatile 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI, MICROWIRE, and DSP interface standards. The on-chip precision output amplifier enables rail-to-rail output swing.

Additional application and technical information can be found in the AD5666 data sheet.

PRODUCT HIGHLIGHTS

1. Quad, 16-bit DAC.
2. On-chip 2.5 V, 5 ppm/°C reference.
3. Available in 14-lead TSSOP.
4. Selectable power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 200 nA at 3 V and 400 nA at 5 V.

FUNCTIONAL BLOCK DIAGRAM

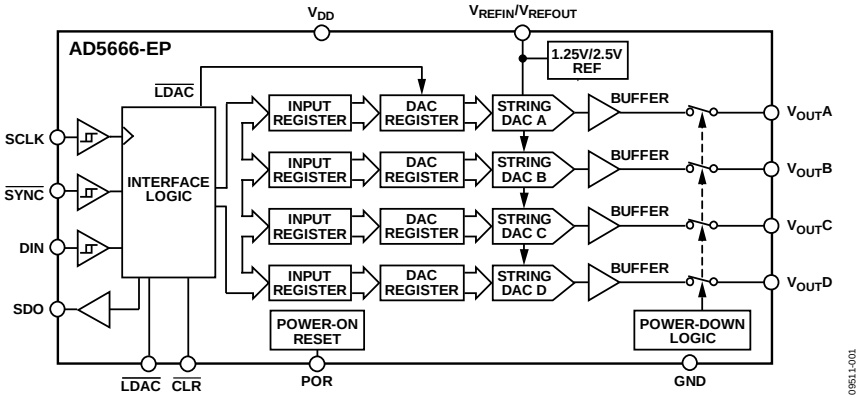

Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

11/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	B Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE[2]					
Resolution	16			Bits	
Relative Accuracy			±21	LSB	See Figure 6
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design (see Figure 7)
Zero-Code Error		1	14	mV	All 0s loaded to DAC register (see Figure 13)
Zero-Code Error Drift		±2		µV/°C	
Full-Scale Error		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 12)
Gain Error			±1	% FSR	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
Offset Error		±1	±14	mV	
DC Power Supply Rejection Ratio		–80		dB	V_{DD} ± 10%
DC Crosstalk (External Reference)		10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5		µV/mA	Due to load current change
		10		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 5 V
Power-Up Time		4		µs	Coming out of power-down mode V_{DD} = 5 V
REFERENCE INPUTS					
Reference Input Voltage		V_{DD}		V	
Reference Current		20	55	µA	$V_{REF} = V_{DD}$ = 5.5 V
Reference Input Range	0		V_{DD}	V	
Reference Input Impedance		14.6		kΩ	Per DAC channel
REFERENCE OUTPUT					
Output Voltage	2.495		2.505	V	At ambient
Reference Temperature Coefficient[3]		±5		ppm/°C	
Reference Output Impedance		7.5		kΩ	
LOGIC INPUTS[3]					
Input Current			±3	µA	All digital inputs
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 5 V
Input High Voltage, V_{INH}	2			V	V_{DD} = 5 V
Pin Capacitance		3		pF	
LOGIC OUTPUTS (SDO)[3]					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} − 1				I_{SOURCE} = 2 mA
High Impedance Leakage Current			±0.25	µA	
High Impedance Output Capacitance		2		pF	

Parameter	B Grade[1] Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	4.5		5.5	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[4]					$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.7	0.9	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		1.3	1.6	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]					
V_{DD} = 4.5 V to 5.5 V		0.4	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Temperature range is −55°C to +125°C, typical at 25°C. Linearity calculated using a reduced code range of 512 to 65,024. Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All four DACs powered down.

AC CHARACTERISTICS

V_{DD} =2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
Output Voltage Settling Time		6	10	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.5		V/µs	
Digital-to-Analog Glitch Impulse		4		nV-sec	1 LSB change around major carry (see Figure 29)
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 Hz to 20 MHz
SDO Feedthrough		3		nV-sec	Daisy-chain mode; SDO load is 10 pF
Digital Feedthrough		0.1		nV-sec	
Digital Crosstalk		0.5		nV-sec	
Analog Crosstalk		2.5		nV-sec	
DAC-to-DAC Crosstalk		3		nV-sec	
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.2 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = 0x8400, 1 kHz
		100		nV/√Hz	DAC code = 0x8400, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] Temperature range is −55°C to + 125°C, typical at 25°C.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 3 and Figure 4. V_{DD} = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX} V_{DD} = 2.7 V to 5.5 V	Unit	Test Conditions/Comments
t_1[1]	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	13	ns min	$\overline{\text{SYNC}}$-to-SCLK falling edge setup time
t_5	4	ns min	Data setup time
t_6	4	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	15	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	13	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK fall ignore
t_{10}	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ fall ignore
t_{11}	10	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{12}	15	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ rising edge
t_{13}	5	ns min	$\overline{\text{CLR}}$ pulse width low
t_{14}	0	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ falling edge
t_{15}	300	ns typ	$\overline{\text{CLR}}$ pulse activation time
t_{16}[2]	22	ns max	SCLK rising edge to SDO valid
t_{17}[2]	5	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_{18}[2]	8	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK rising edge
t_{19}[2]	0	ns min	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.
[2] Daisy-chain mode only.

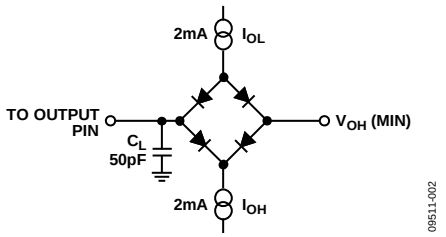

Figure 2. Load Circuit for Digital Output (SDO) Timing Specifications

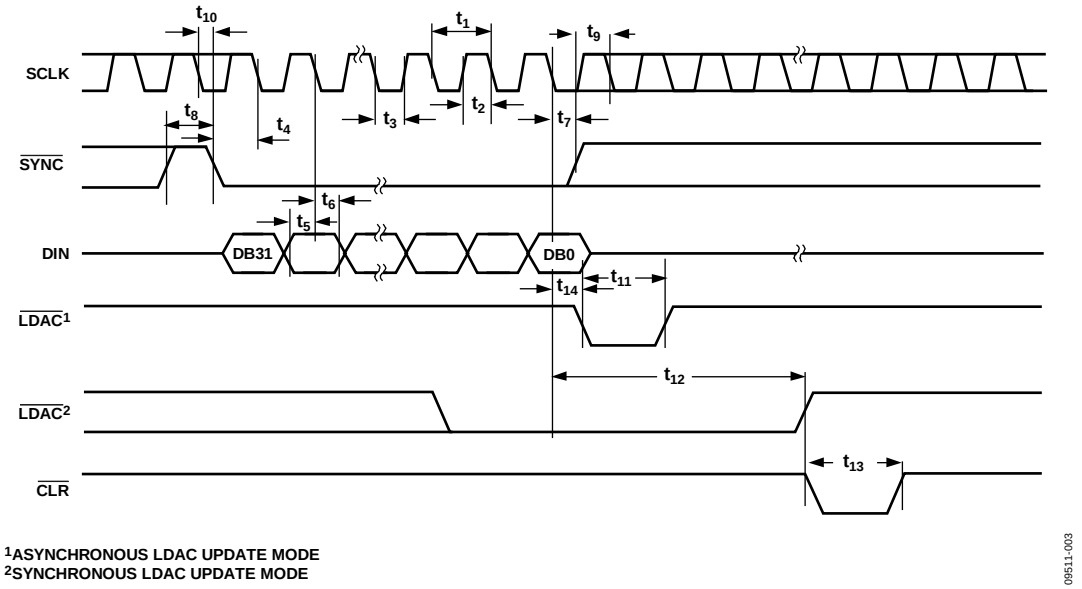

Figure 3. Serial Write Operation

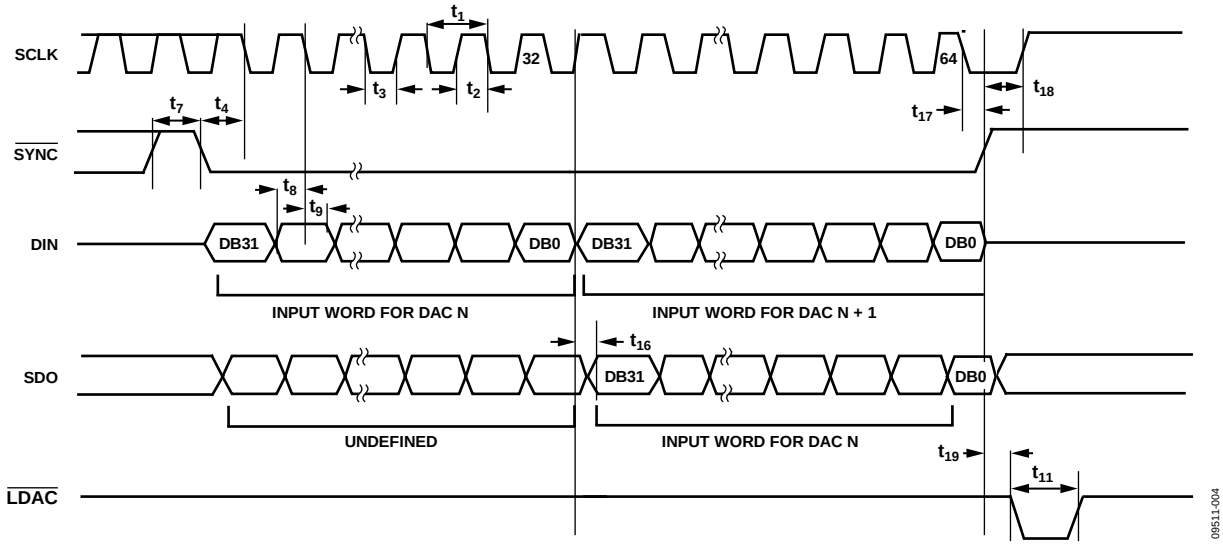

Figure 4. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
TSSOP Package	
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb Free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

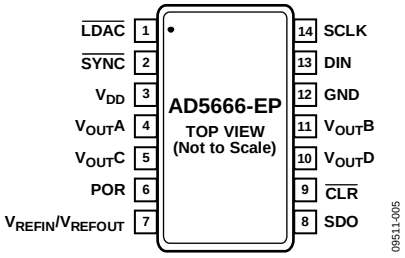

Figure 5. 14-Lead TSSOP (RU-14) Pin Configuration

Table 5. 14-Lead TSSOP (RU-14) Pin Function Descriptions

Pin No.	Mnemonic
1	$\overline{\text{LDAC}}$
2	$\overline{\text{SYNC}}$
3	V_{DD}
4	$V_{OUT}A$
5	$V_{OUT}C$
6	POR
7	V_{REFIN}/V_{REFOUT}
8	SDO
9	$\overline{\text{CLR}}$
10	$V_{OUT}D$
11	$V_{OUT}B$
12	GND
13	DIN
14	SCLK

TYPICAL PERFORMANCE CHARACTERISTICS

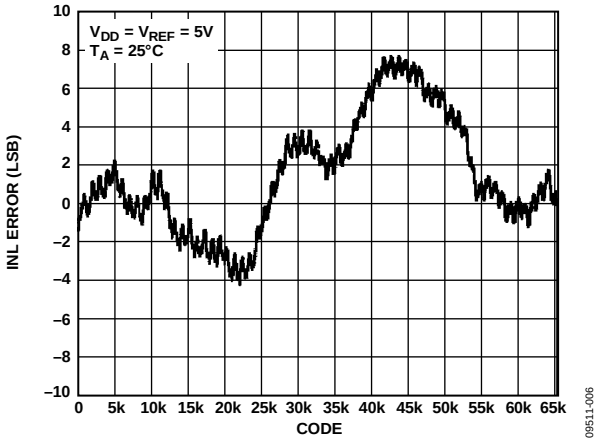

Figure 6. INL

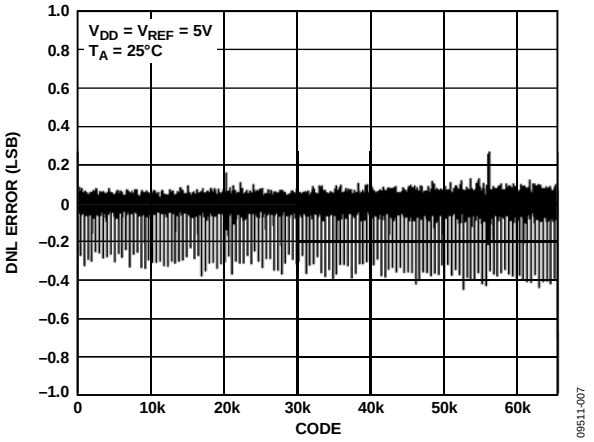

Figure 7. DNL

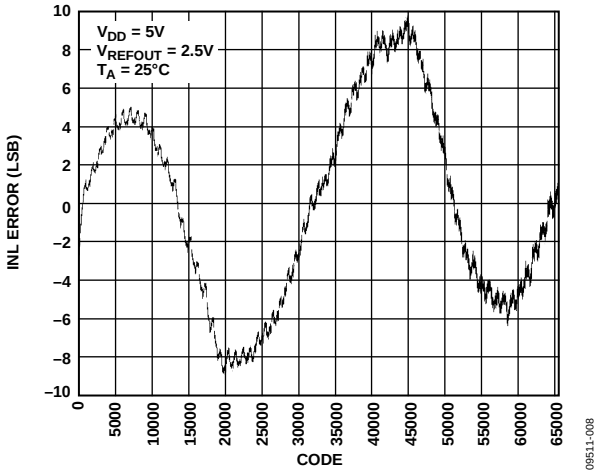

Figure 8. INL—AD5666-EP-2

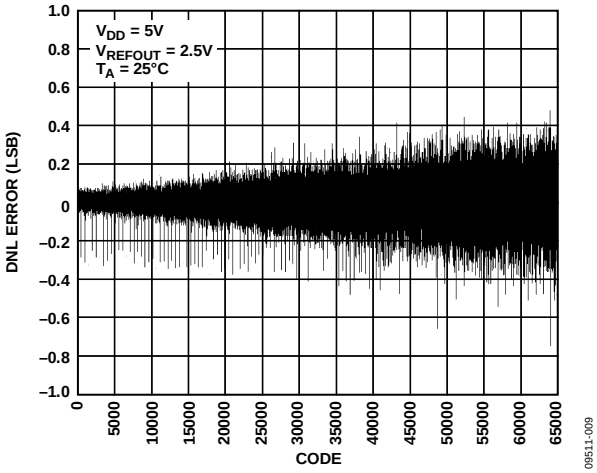

Figure 9. DNL—AD5666-EP-2

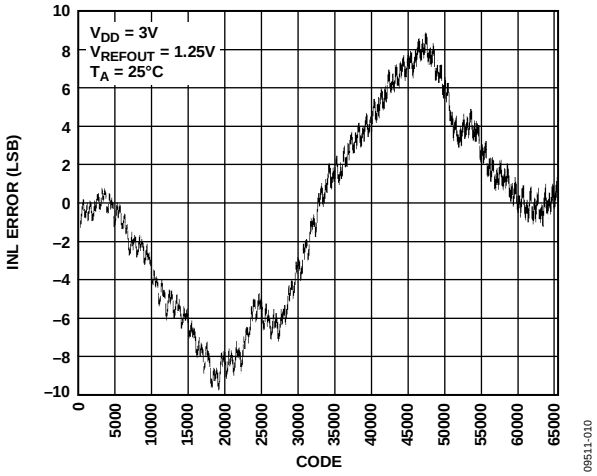

Figure 10. INL—AD5666-EP-1

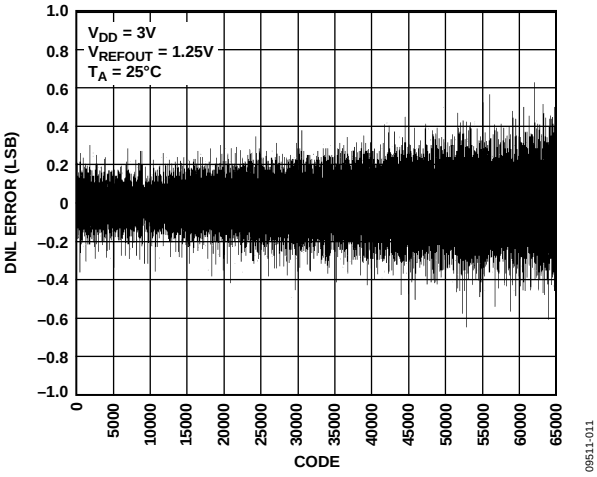

Figure 11. DNL—AD5666-EP-1

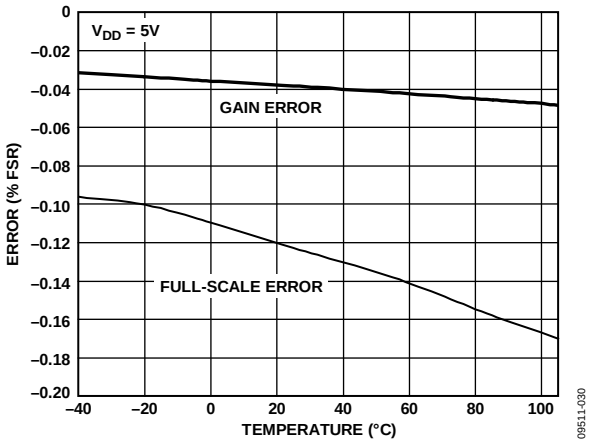

Figure 12. Gain Error and Full-Scale Error vs. Temperature

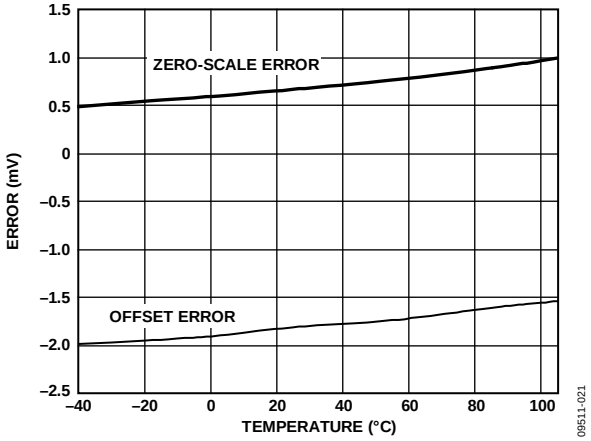

Figure 13. Zero-Scale Error and Offset Error vs. Temperature

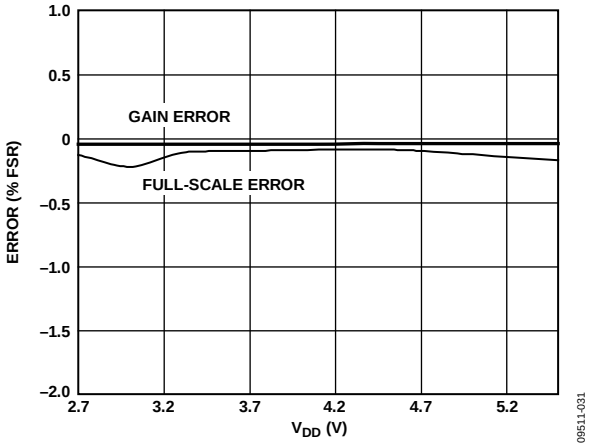

Figure 14. Gain Error and Full-Scale Error vs. Supply Voltage

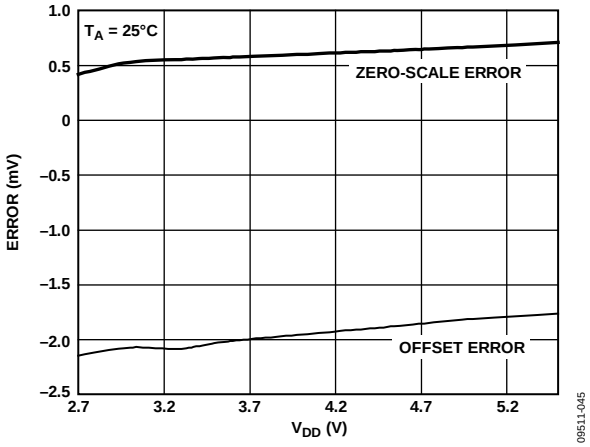

Figure 15. Zero-Scale Error and Offset Error vs. Supply Voltage

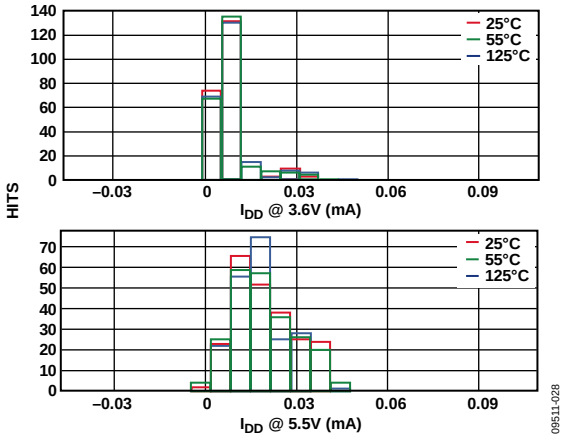

Figure 16. I_{DD} Histogram with External Reference

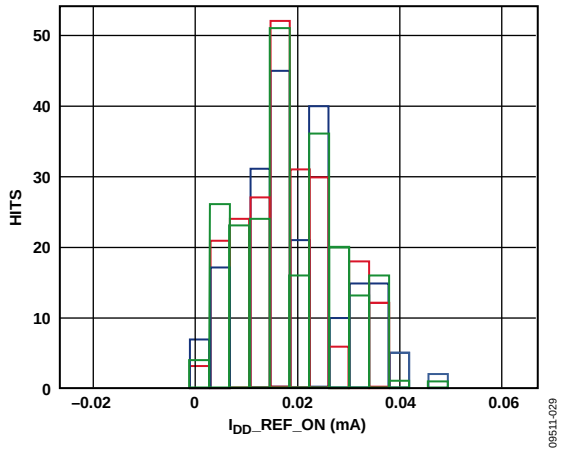

Figure 17. I_{DD} Histogram with Internal Reference

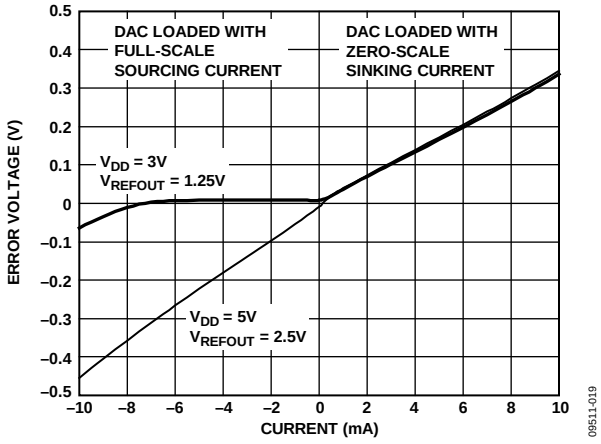

Figure 18. Headroom at Rails vs. Source and Sink

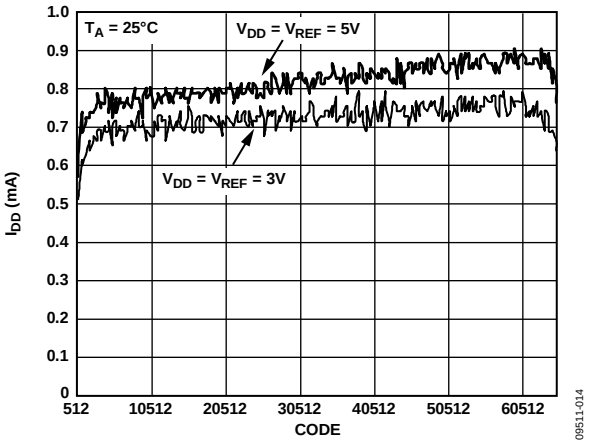

Figure 21. Supply Current vs. Code

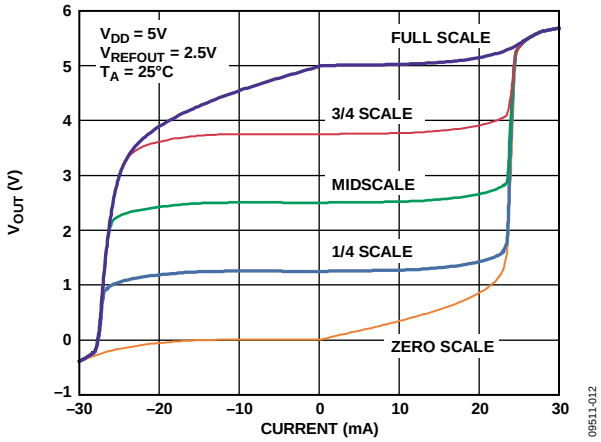

Figure 19. Source and Sink Current Capability with V_{DD} = 5 V

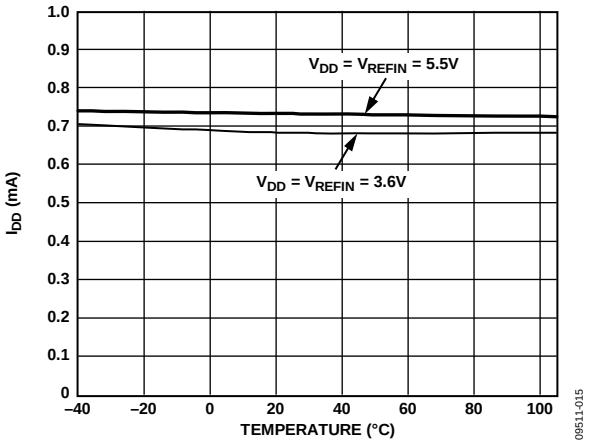

Figure 22. Supply Current vs. Temperature

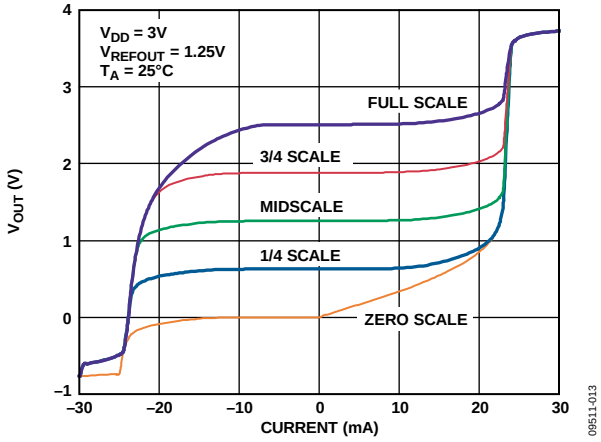

Figure 20. Source and Sink Current Capability with V_{DD} = 3 V

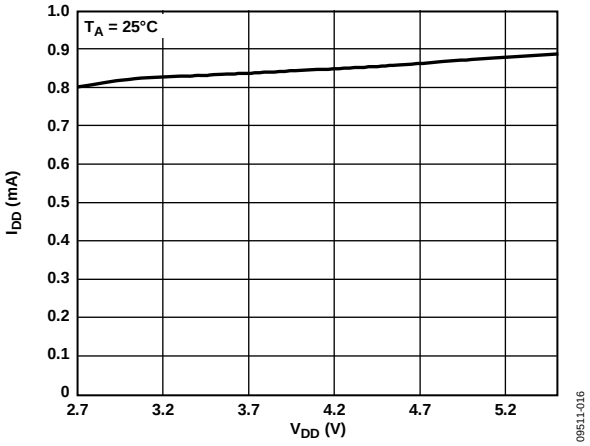

Figure 23. Supply Current vs. Supply Voltage

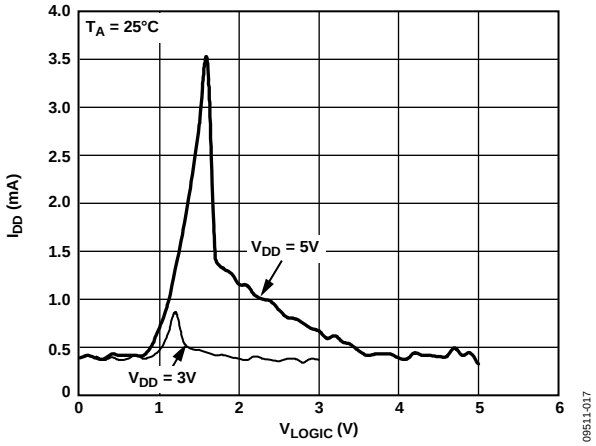

Figure 24. Supply Current vs. Logic Input Voltage

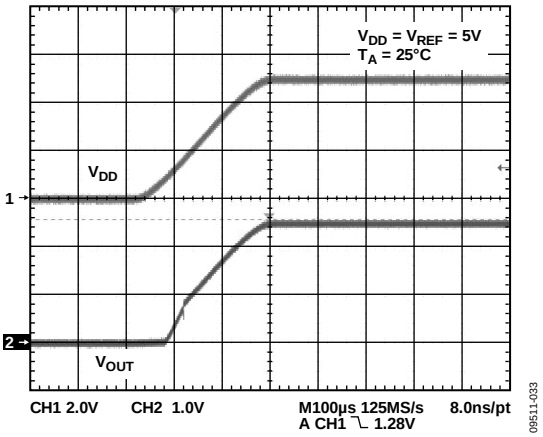

Figure 27. Power-On Reset to Midscale

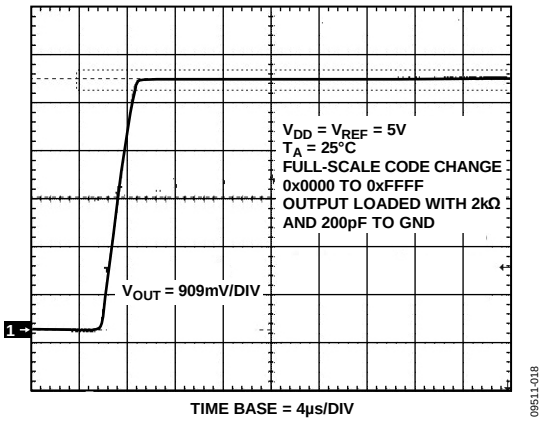

Figure 25. Full-Scale Settling Time

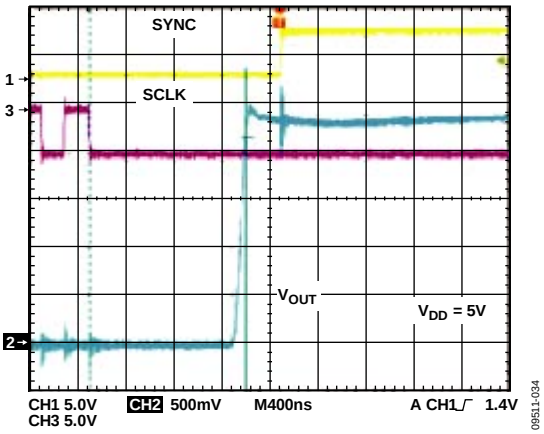

Figure 28. Exiting Power-Down to Midscale

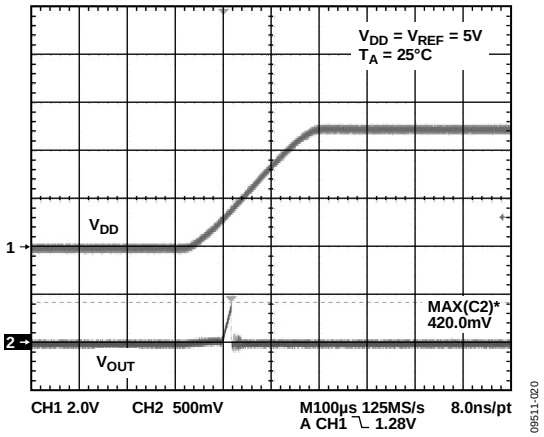

Figure 26. Power-On Reset to 0 V

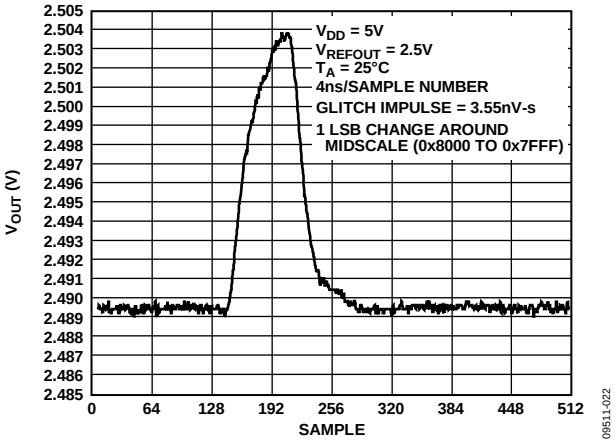

Figure 29. Digital-to-Analog Glitch Impulse

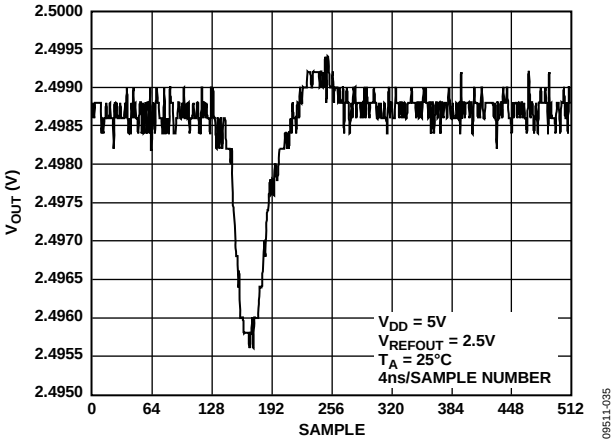

Figure 30. Analog Crosstalk

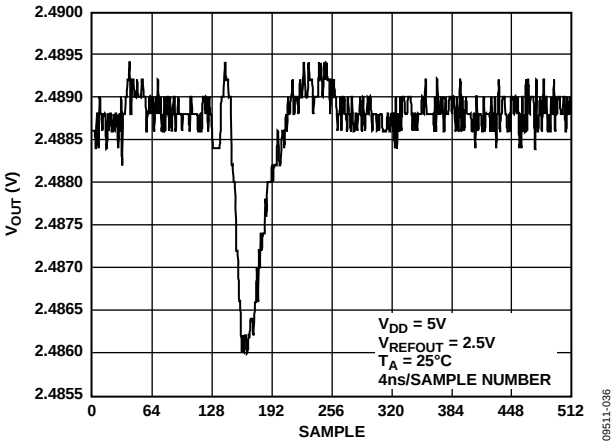

Figure 31. DAC-to-DAC Crosstalk

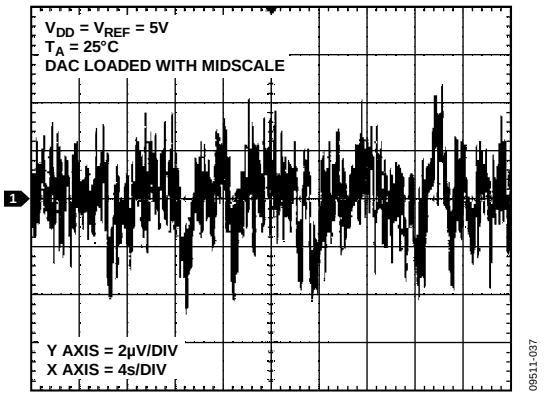

Figure 32. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

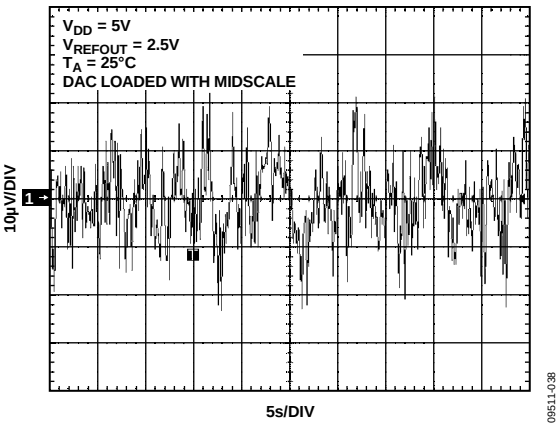

Figure 33. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

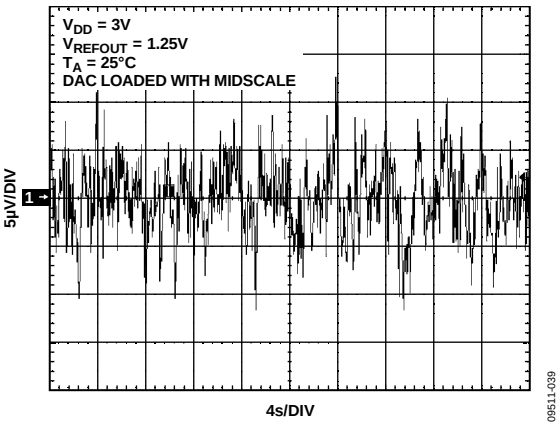

Figure 34. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

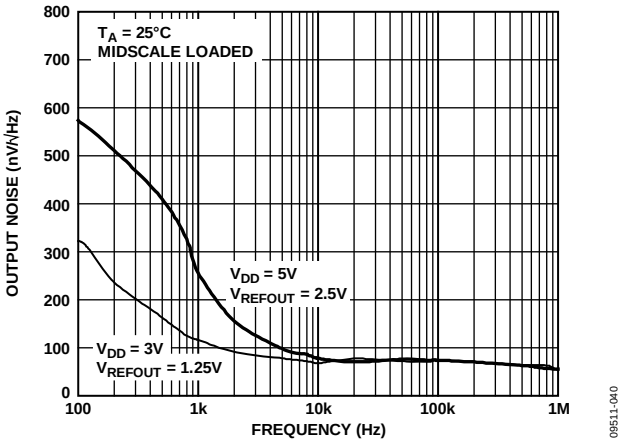

Figure 35. Noise Spectral Density, Internal Reference

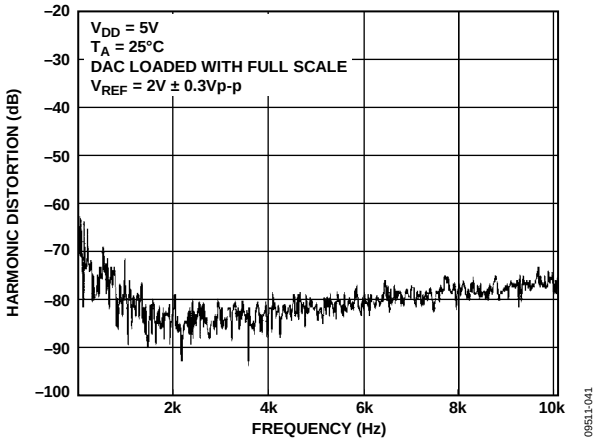

Figure 36. Total Harmonic Distortion

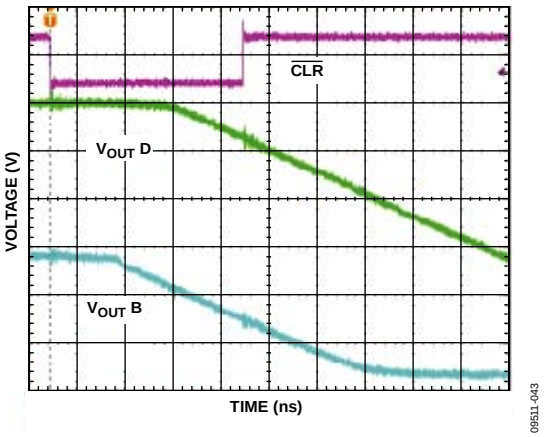

Figure 38. Hardware $\overline{CLR}$

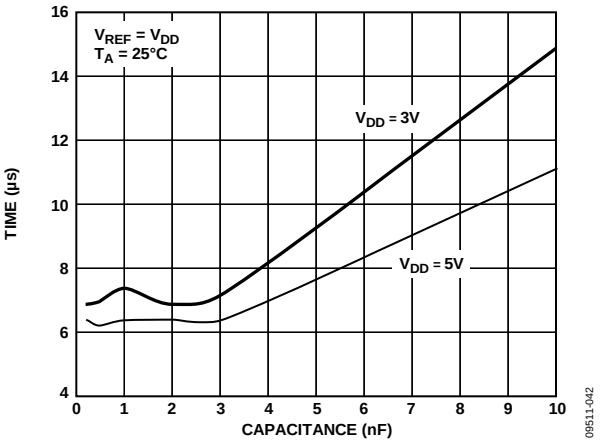

Figure 37. Settling Time vs. Capacitive Load

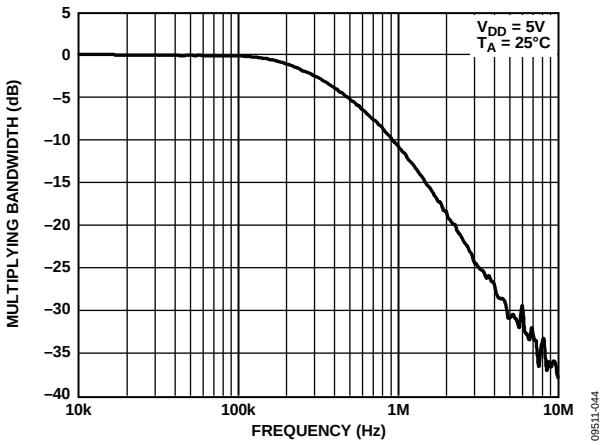

Figure 39. Multiplying Bandwidth

OUTLINE DIMENSIONS

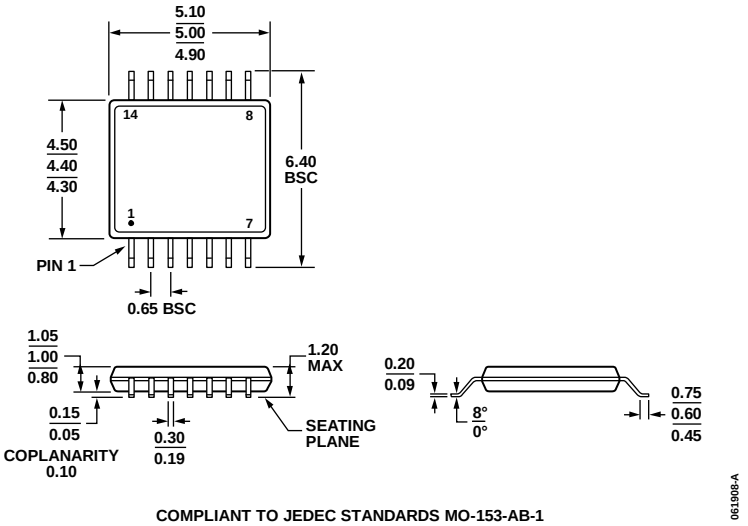

Figure 40. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Power-On Reset to Code	Accuracy	Internal Reference	Temperature Range	Package Description	Package Option
AD5666SRU-EP-2RL7	Zero	±21 LSB INL	2.5 V	−55°C to +125°C	14-Lead TSSOP	RU-14

[1] Z = RoHS Compliant Part.

D09511-0-11/10(0)