

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultralow Power Consumption  
Active Mode: 220  $\mu$ A at 1 MHz, 2.2 V  
Standby Mode: 0.9  $\mu$ A  
Off Mode (RAM Retention): 0.1  $\mu$ A
- Five Power-Saving Modes
- Wake-Up From Standby Mode in Less Than 6  $\mu$ s
  - Internal Very Low Power, Low-Frequency Oscillator
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- 16-Bit Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer\_A With Five Capture/Compare Registers
- Two Universal Serial Communication Interfaces (USCIs)
  - USCI\_A0
    - Enhanced UART Supporting Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI\_B0
    - I<sup>2</sup>C
    - Synchronous SPI
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Integrated LCD Driver With Contrast Control for Up to 144 Segments
- Basic Timer With Real Time Clock Feature
- Brownout detector
- On-Chip Comparator for Analog Signal Compare Function or Slope A/D
- 10-Bit 200-kps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, Autoscan, and Data Transfer Controller
- Serial Onboard Programming, No External Programming Voltage Needed  
Programmable Code Protection by Security Fuse
- Bootstrap Loader
- On-Chip Emulation Module
- Family Members Include:
  - MSP430F4152: 16KB+256B Flash Memory  
512B RAM
  - MSP430F4132: 8KB+256B Flash Memory  
512B RAM
- Available in 64-Pin QFP Package and 48-Pin QFN Package (See Available Options)
- For Complete Module Descriptions, See *The MSP430x4xx Family User's Guide*, Literature Number SLAU056

## description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generator that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6  $\mu$ s.

The MSP430F41x2 is a microcontroller configuration with two 16-bit timers, a basic timer with a real-time clock, a 10-bit A/D converter, a versatile analog comparator, two universal serial communication interfaces, up to 48 I/O pins, and a liquid crystal display driver.

Typical applications for this device include analog and digital sensor systems, remote controls, thermostats, digital timers, hand-held meters, etc.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# MSP430F41x2

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### AVAILABLE OPTIONS<sup>†</sup>

| T <sub>A</sub> | PACKAGED DEVICES <sup>‡</sup>    |                                    |
|----------------|----------------------------------|------------------------------------|
|                | PLASTIC 64-PIN QFP (PM)          | PLASTIC 48-PIN QFN (RGZ)           |
| -40°C to 85°C  | MSP430F4152IPM<br>MSP430F4132IPM | MSP430F4152IRGZ<br>MSP430F4132IRGZ |

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

<sup>‡</sup> Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

## DEVELOPMENT TOOL SUPPORT

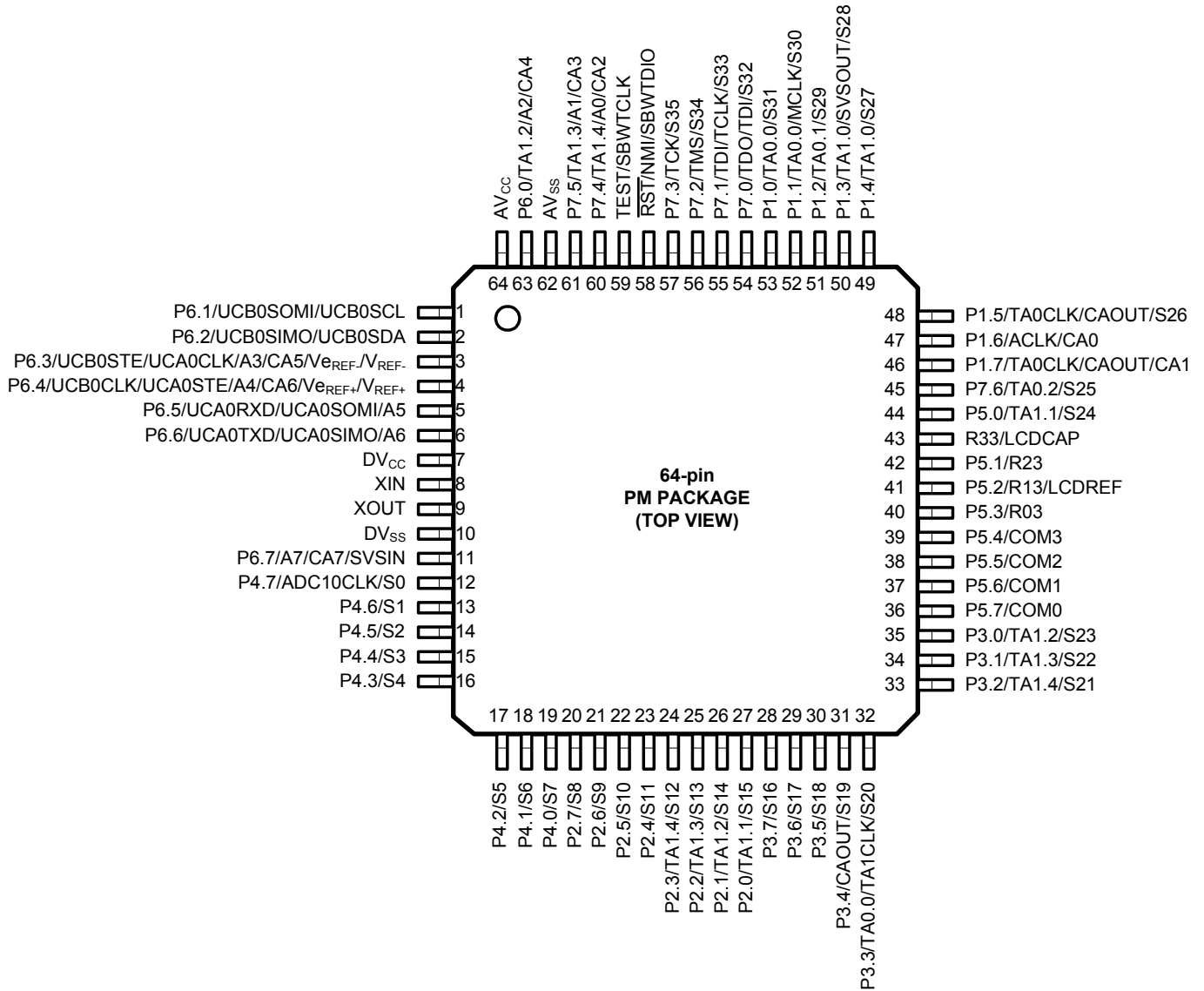
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U64A (PM package)
- Production Programmer
  - MSP-GANG430



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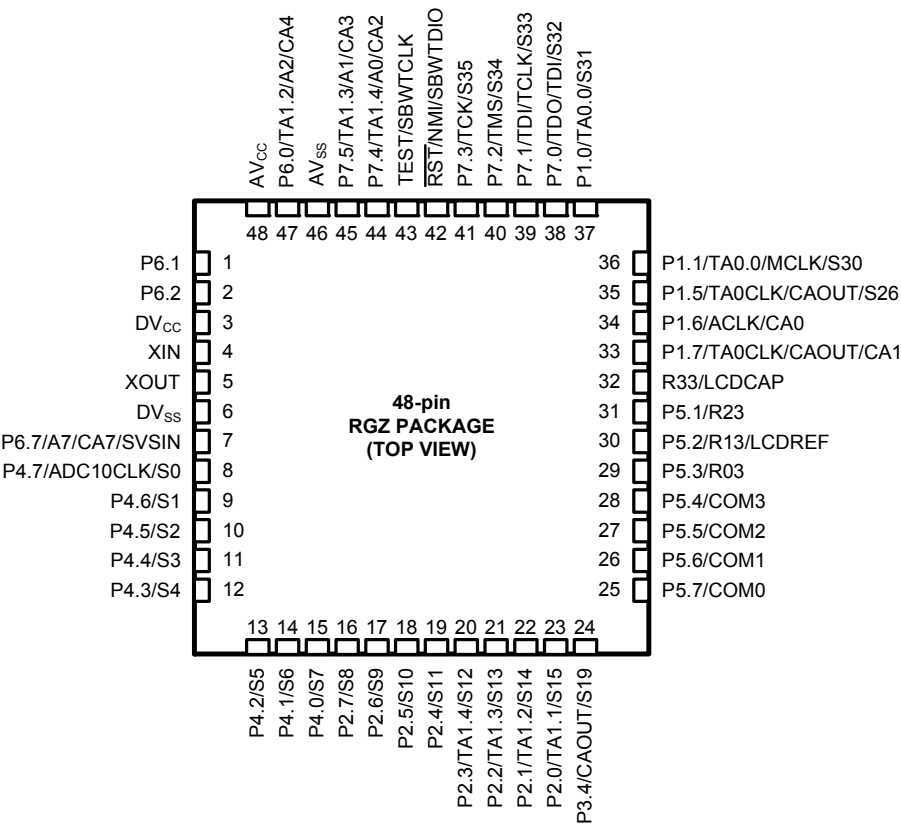
**pin designation, MSP430F41x2IPM (QFP)**



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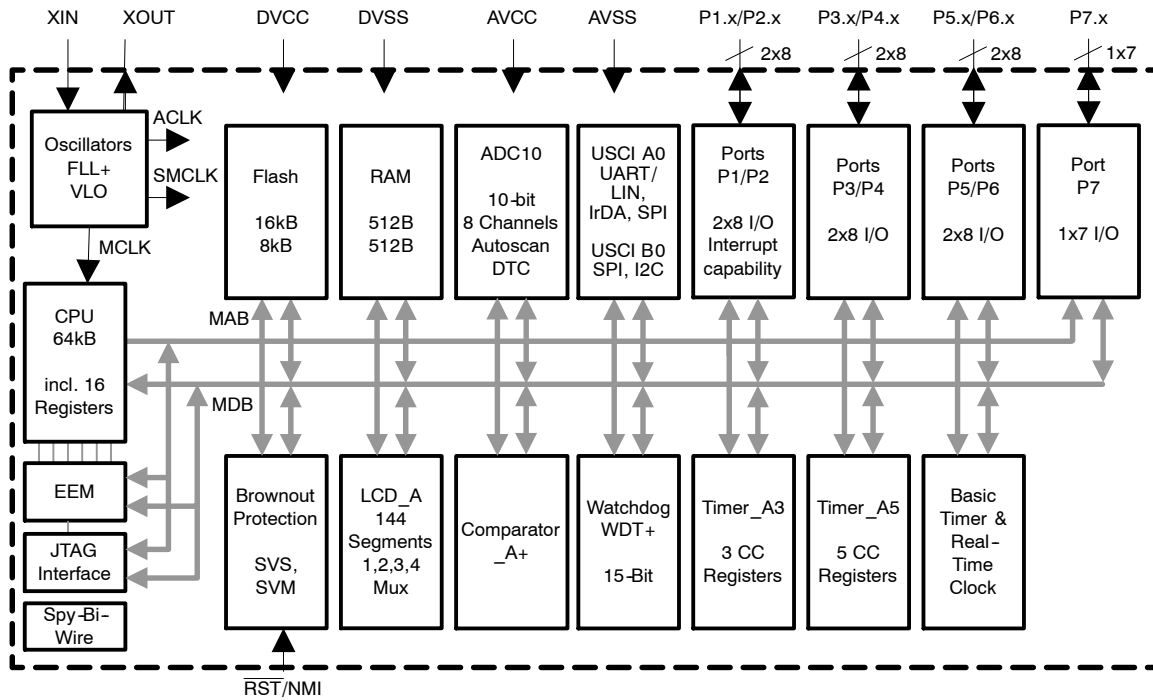
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pin designation, MSP430F41x2IRGZ (QFN)<sup>†</sup>



<sup>†</sup> "Not available" pins in the 48-pin package should be initialized to output direction.

**functional block diagram**



NOTE: The USCI A0 and USCI B0 cannot be used in the 48-pin package options (RGZ).

# MSP430F41x2

## MIXED SIGNAL MICROCONTROLLER

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### Terminal Functions

| TERMINAL                  |        |        | I/O | DESCRIPTION                                                                                                           |
|---------------------------|--------|--------|-----|-----------------------------------------------------------------------------------------------------------------------|
| NAME                      | NO.    |        |     |                                                                                                                       |
|                           | 64 PIN | 48 PIN |     |                                                                                                                       |
| P1.0/TA0.0/S31            | 53     | 37     | I/O | General-purpose digital I/O pin<br>Timer0_A3, capture: CCI0A input, compare: Out0 output<br>LCD segment output        |
| P1.1/TA0.0/<br>MCLK/S30   | 52     | 36     | I/O | General-purpose digital I/O pin<br>Timer0_A3, capture: CCI0B input<br>MCLK signal output<br>LCD segment output        |
| P1.2/TA0.1/S29            | 51     | -      | I/O | General-purpose digital I/O pin<br>Timer0_A3, capture: CCI1A input, compare: Out1 output<br>LCD segment output        |
| P1.3/TA1.0/<br>SVSOUT/S28 | 50     | -      | I/O | General-purpose digital I/O pin<br>Timer1_A5, capture: CCI0B input<br>SVS comparator output<br>LCD segment output     |
| P1.4/TA1.0/S27            | 49     | -      | I/O | General-purpose digital I/O pin/<br>Timer1_A5, capture: CCI0A input, compare: Out0 output<br>LCD segment output       |
| P1.5/TA0CLK/<br>CAOUT/S26 | 48     | 35     | I/O | General-purpose digital I/O pin<br>Timer0_A3, clock signal TACLK input<br>Comparator_A output<br>LCD segment output   |
| P1.6/ACLK/CA0             | 47     | 34     | I/O | General-purpose digital I/O pin<br>Comparator_A input 0<br>ACLK signal output                                         |
| P1.7/TA0CLK<br>CAOUT/CA1  | 46     | 33     | I/O | General-purpose digital I/O pin<br>Timer0_A3, clock signal TACLK input<br>Comparator_A output<br>Comparator_A input 1 |
| P2.0/TA1.1/S15            | 27     | 23     | I/O | General-purpose digital I/O pin<br>Timer1_A5, compare: Out1 Output<br>LCD segment output                              |
| P2.1/TA1.2/S14            | 26     | 22     | I/O | General-purpose digital I/O pin<br>Timer1_A5, compare: Out2 Output<br>LCD segment output                              |
| P2.2/TA1.3/S13            | 25     | 21     | I/O | General-purpose digital I/O pin<br>Timer1_A5, compare: Out3 Output<br>LCD segment output                              |
| P2.3/TA1.4/S12            | 24     | 20     | I/O | General-purpose digital I/O pin<br>Timer1_A5, compare: Out4 output<br>LCD segment output                              |
| P2.4/S11                  | 23     | 19     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                 |
| P2.5/S10                  | 22     | 18     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                 |
| P2.6/S9                   | 21     | 17     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                 |
| P2.7/S8                   | 20     | 16     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                 |



### Terminal Functions (continued)

| TERMINAL                  |        |        | I/O | DESCRIPTION                                                                                                                                  |
|---------------------------|--------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                      | NO.    |        |     |                                                                                                                                              |
|                           | 64 PIN | 48 PIN |     |                                                                                                                                              |
| P3.0/TA1.2/S23            | 35     | -      | I/O | General-purpose digital I/O pin<br>Timer1_A5, capture: CCI2A input, compare: Out2 output<br>LCD segment output                               |
| P3.1/TA1.3/S22            | 34     | -      | I/O | General-purpose digital I/O pin<br>Timer1_A5, capture: CCI3A input, compare: Out3 output<br>LCD segment output                               |
| P3.2/TA1.4/S21            | 33     | -      | I/O | General-purpose digital I/O pin<br>Timer1_A5, capture: CCI4A input, compare: Out4 output<br>LCD segment output                               |
| P3.3/TA0.0/<br>TA1CLK/S20 | 32     | -      | I/O | General-purpose digital I/O pin<br>Timer0_A3, compare: Out0 output<br>Timer1_A5, clock signal TACLK input<br>LCD segment output              |
| P3.4/CAOUT/S19            | 31     | 24     | I/O | General-purpose digital I/O pin<br>Comparator_A output<br>LCD segment output                                                                 |
| P3.5/S18                  | 30     | -      | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P3.6/S17                  | 29     | -      | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P3.7/S16                  | 28     | -      | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.0/S7                   | 19     | 15     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.1/S6                   | 18     | 14     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.2/S5                   | 17     | 13     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.3/S4                   | 16     | 12     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.4/S3                   | 15     | 11     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.5/S2                   | 14     | 10     | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.6/S1                   | 13     | 9      | I/O | General-purpose digital I/O pin<br>LCD segment output                                                                                        |
| P4.7/ADC10CLK/<br>S0      | 12     | 8      | I/O | General-purpose digital I/O pin<br>ADC10, conversion clock<br>LCD segment output                                                             |
| P5.0/TA1.1/S24            | 44     | -      | I/O | General-purpose digital I/O pin<br>Timer1_A5, capture: CCI1A input, compare: Out1 output<br>LCD segment output                               |
| LCDCAP/R33                | 43     | 32     | I/O | Capacitor connection for LCD charge pump<br>input port of the most positive analog LCD level (V4)                                            |
| P5.1/R23                  | 42     | 31     | I/O | General-purpose digital I/O pin<br>input port of the second most positive analog LCD level (V3)                                              |
| P5.2/LCDREF/<br>R13       | 41     | 30     | I/O | General-purpose digital I/O pin<br>External LCD reference voltage input<br>input port of the third most positive analog LCD level (V3 or V2) |

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## MIXED SIGNAL MICROCONTROLLER

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### Terminal Functions (continued)

| TERMINAL                                                                  |           |           | I/O | DESCRIPTION                                                                                                                                                       |
|---------------------------------------------------------------------------|-----------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                                      | NO.       |           |     |                                                                                                                                                                   |
|                                                                           | 64<br>PIN | 48<br>PIN |     |                                                                                                                                                                   |
| P5.3/R03                                                                  | 40        | 29        | I/O | General-purpose digital I/O pin<br>input port of the fourth most positive analog LCD level (V1)                                                                   |
| P5.4/COM3                                                                 | 39        | 28        | I/O | General-purpose digital I/O pin<br>common output, COM0–3 are used for LCD backplanes                                                                              |
| P5.5/COM2                                                                 | 38        | 27        | I/O | General-purpose digital I/O pin<br>common output, COM0–3 are used for LCD backplanes                                                                              |
| P5.6/COM1                                                                 | 37        | 26        | I/O | General-purpose digital I/O pin<br>common output, COM0–3 are used for LCD backplanes                                                                              |
| P5.7/COM0                                                                 | 36        | 25        | I/O | General-purpose digital I/O pin<br>common output, COM0–3 are used for LCD backplanes                                                                              |
| P6.0/TA1.2/A2 <sup>†</sup> /<br>CA4                                       | 63        | 47        | I/O | General-purpose digital I/O pin<br>Timer1_A5, compare: Out2 output<br>ADC10 analog input A2 <sup>†</sup><br>Comparator_A input 4                                  |
| P6.1/<br>UCB0SOMI <sup>†</sup> /<br>UCB0SCL <sup>†</sup>                  | 1         | 1         | I/O | General-purpose digital I/O pin<br>USCI B0 slave out/master in in SPI mode, SCL I <sup>2</sup> C clock in I <sup>2</sup> C mode <sup>†</sup>                      |
| P6.2/<br>UCB0SIMO <sup>†</sup> /<br>UCB0SDA <sup>†</sup>                  | 2         | 2         | I/O | General-purpose digital I/O pin<br>USCI B0 slave in/master out in SPI mode, SDA I <sup>2</sup> C data in I <sup>2</sup> C mode <sup>†</sup>                       |
| P6.3/UCB0STE/<br>UCA0CLK/A3/<br>CA5/V <sub>eref-</sub> /V <sub>ref-</sub> | 3         | -         | I/O | General-purpose digital I/O pin<br>USCI B0 slave transmit enable/USCI A0 clock input/output<br>ADC10 analog input A3 / negative reference<br>Comparator_A input 5 |
| P6.4/UCB0CLK/<br>UCA0STE/A4/<br>CA6/V <sub>eref+</sub> /V <sub>ref+</sub> | 4         | -         | I/O | General-purpose digital I/O pin<br>USCI B0 clock input/output, USCI A0 slave transmit enable<br>ADC10 analog input A4/ positive reference<br>Comparator_A input 6 |
| P6.5/UCA0RXD/<br>UCA0SOMI/A5                                              | 5         | -         | I/O | General-purpose digital I/O pin<br>USCI A0 receive data input in UART mode, slave data out/master in in SPI mode<br>ADC10 analog input A5                         |
| P6.6/UCA0TXD/<br>UCA0SIMO/A6                                              | 6         | -         | I/O | General-purpose digital I/O pin<br>USCI A0 transmit data output in UART mode, slave data in/master out SPI mode<br>ADC10 analog input A6                          |
| P6.7/A7/CA7/<br>SVSIN                                                     | 11        | 7         | I/O | General-purpose digital I/O pin<br>ADC10 analog input A7<br>Comparator_A input 7<br>SVS input                                                                     |
| P7.0/TDO/TDI/<br>S32                                                      | 54        | 38        | I/O | General-purpose digital I/O pin<br>JTAG test data output terminal or test data input in programming an test<br>LCD segment output                                 |
| P7.1/TDI/TCLK/<br>S33                                                     | 55        | 39        | I/O | General-purpose digital I/O pin<br>JTAG test data input or test clock input in programming an test<br>LCD segment output                                          |
| P7.2/TMS/S34                                                              | 56        | 40        | I/O | General-purpose digital I/O pin<br>JTAG test mode select, input terminal for device programming and test<br>LCD segment output                                    |

<sup>†</sup> 64-pin package devices only



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### Terminal Functions (continued)

| TERMINAL              |           |           | I/O | DESCRIPTION                                                                                                                               |
|-----------------------|-----------|-----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                  | NO.       |           |     |                                                                                                                                           |
|                       | 64<br>PIN | 48<br>PIN |     |                                                                                                                                           |
| P7.3/TCK/S35          | 57        | 41        | I/O | General-purpose digital I/O pin<br>Test clock input for device programming and test<br>LCD segment output                                 |
| P7.4/TA1.4/<br>A0/CA2 | 60        | 44        | I/O | General-purpose digital I/O pin<br>Timer1_A5, capture: CCI4B input, compare: Out4 output<br>ADC10 analog input A0<br>Comparator_A input 2 |
| P7.5/TA1.3/<br>A1/CA3 | 61        | 45        | I/O | General-purpose digital I/O pin<br>Timer1_A5, capture: CCI3B input, compare: Out3 output<br>ADC10 analog input A1<br>Comparator_A input 3 |
| P7.6/TA0.2/S25        | 45        | -         | I/O | General-purpose digital I/O pin<br>Timer0_A3, capture: CCI2A input, compare: Out2 output<br>LCD segment output                            |
| AV <sub>CC</sub>      | 64        | 48        |     | Analog supply voltage, positive terminal                                                                                                  |
| AV <sub>SS</sub>      | 62        | 46        |     | Analog supply voltage, negative terminal                                                                                                  |
| DV <sub>CC</sub>      | 7         | 3         |     | Digital supply voltage, positive terminal. Supplies all digital parts.                                                                    |
| DV <sub>SS</sub>      | 10        | 6         |     | Digital supply voltage, negative terminal. Supplies all digital parts.                                                                    |
| XOUT                  | 9         | 5         | O   | Output port for crystal oscillator XT1. Standard or watch crystals can be connected.                                                      |
| XIN                   | 8         | 4         | I   | Input port for crystal oscillator XT1. Standard or watch crystals can be connected.                                                       |
| RST/NMI/<br>SBWTDIO   | 58        | 42        | I   | Reset or nonmaskable interrupt input<br>Spy-Bi-Wire test data input/output during programming and test                                    |
| TEST/SBWTCLK          | 59        | 43        | I   | Selects test mode for JTAG pins on Port7. The device protection fuse is connected to TEST.                                                |
| Thermal Pad           | NA        | NA        | NA  | QFN package pad (RGZ package only). Connection to DV <sub>SS</sub> is recommended.                                                        |

# MSP430F41x2 MIXED SIGNAL MICROCONTROLLER

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## short-form description

### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

### instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 1. Instruction Word Formats**

|                                   |                 |                       |
|-----------------------------------|-----------------|-----------------------|
| Dual operands, source-destination | e.g., ADD R4,R5 | R4 + R5 ---> R5       |
| Single operands, destination only | e.g., CALL R8   | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional     | e.g., JNE       | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE           | S | D | SYNTAX             | EXAMPLE          | OPERATION                     |
|------------------------|---|---|--------------------|------------------|-------------------------------|
| Register               | ● | ● | MOV Rs,Rd          | MOV R10,R11      | R10 → R11                     |
| Indexed                | ● | ● | MOV X(Rn),Y(Rm)    | MOV 2(R5),6(R6)  | M(2+R5) → M(6+R6)             |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI       |                  | M(EDE) → M(TONI)              |
| Absolute               | ● | ● | MOV & MEM, & TCDAT |                  | M(MEM) → M(TCDAT)             |
| Indirect               | ● |   | MOV @Rn,Y(Rm)      | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6)            |
| Indirect autoincrement | ● |   | MOV @Rn+,Rm        | MOV @R10+,R11    | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate              | ● |   | MOV #X,TONI        | MOV #45,TONI     | #45 → M(TONI)                 |

NOTE: S = source, D = destination



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## **operating modes**

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

# MSP430F41x2

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### interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

If the reset vector (located at address 0xFFFFE) contains 0xFFFF (e.g., flash is not programmed), the CPU goes into LPM4 immediately after power-up.

| INTERRUPT SOURCE                                                                       | INTERRUPT FLAG                                                                                                                       | SYSTEM INTERRUPT                                | WORD ADDRESS | PRIORITY    |
|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------|--------------|-------------|
| Power-Up<br>External Reset<br>Watchdog<br>Flash Memory<br>PC Out-of-Range (see Note 4) | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV<br>(see Note 1)                                                                                   | Reset                                           | 0xFFFFE      | 15, highest |
| NMI<br>Oscillator Fault<br>Flash Memory Access Violation                               | NMIIFG (see Notes 1 and 3)<br>OFIFG (see Notes 1 and 3)<br>ACCVIFG (see Notes 1, 2, and 4)                                           | (Non)maskable<br>(Non)maskable<br>(Non)maskable | 0xFFFFC      | 14          |
| Timer_A5                                                                               | TA1CCR0 CCIFG0 (see Note 2)                                                                                                          | Maskable                                        | 0xFFFFA      | 13          |
| Timer_A5                                                                               | TA1CCR1 to TACCR4 CCIFGs,<br>and TAIFG (see Notes 1 and 2)                                                                           | Maskable                                        | 0xFFFF8      | 12          |
| Comparator_A+                                                                          | CAIFG                                                                                                                                | Maskable                                        | 0xFFFF6      | 11          |
| Watchdog Timer+                                                                        | WDTIFG                                                                                                                               | Maskable                                        | 0xFFFF4      | 10          |
| USCI_A0/B0 Receive                                                                     | UCA0RXIFG (see Note 1),<br>UCB0RXIFG (SPI mode), or<br>UCB0STAT UCALIFG, UCNACKIFG, UCSTTIFG,<br>UCSTPIFG (I2C mode)<br>(see Note 1) | Maskable                                        | 0xFFFF2      | 9           |
| USCI_A0/B0 Transmit                                                                    | UCA0TXIFG (see Note 1),<br>UCB0TXIFG (SPI mode), or<br>UCB0RXIFG and UCB0TXIFG (I2C mode)<br>(see Note 1)                            | Maskable                                        | 0xFFFF0      | 8           |
| ADC10                                                                                  | ADC10IFG (see Note 2)                                                                                                                | Maskable                                        | 0xFFEE       | 7           |
| Timer_A3                                                                               | TACCR0 CCIFG0 (see Note 2)                                                                                                           | Maskable                                        | 0xFFEC       | 6           |
| Timer_A3                                                                               | TACCR1 CCIFG1 and TACCR2 CCIFG2,<br>TAIFG (see Notes 1 and 2)                                                                        | Maskable                                        | 0xFFEA       | 5           |
| I/O Port P1 (Eight Flags)                                                              | P1IFG.0 to P1IFG.7 (see Notes 1 and 2)                                                                                               | Maskable                                        | 0xFFE8       | 4           |
|                                                                                        |                                                                                                                                      |                                                 | 0xFFE6       | 3           |
|                                                                                        |                                                                                                                                      |                                                 | 0xFFE4       | 2           |
| I/O Port P2 (Eight Flags)                                                              | P2IFG.0 to P2IFG.7 (see Notes 1 and 2)                                                                                               | Maskable                                        | 0xFFE2       | 1           |
| Basic Timer1/RTC                                                                       | BTIFG                                                                                                                                | Maskable                                        | 0xFFE0       | 0, lowest   |

- NOTES:
- Multiple source flags
  - Interrupt flags are located in the module.
  - A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
  - Access and key violations, KEYV and ACCVIFG.



## special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

### interrupt enable 1 and 2

| Address | 7 | 6 | 5      | 4     | 3 | 2 | 1    | 0     |
|---------|---|---|--------|-------|---|---|------|-------|
| 00h     |   |   | ACCVIE | NMIIE |   |   | OFIE | WDTIE |
|         |   |   | rw-0   | rw-0  |   |   | rw-0 | rw-0  |

WDTIE      Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE      Oscillator fault enable

NMIIE      (Non)maskable interrupt enable

ACCVIE      Flash access violation interrupt enable

| Address | 7    | 6 | 5 | 4 | 3        | 2        | 1        | 0        |
|---------|------|---|---|---|----------|----------|----------|----------|
| 01h     | BTIE |   |   |   | UCB0TXIE | UCB0RXIE | UCA0TXIE | UCA0RXIE |
|         | rw-0 |   |   |   | rw-0     | rw-0     | rw-0     | rw-0     |

UCA0RXIE      USCI\_A0 receive interrupt enable

UCA0TXIE      USCI\_A0 transmit interrupt enable

UCB0RXIE      USCI\_B0 receive interrupt enable

UCB0TXIE      USCI\_B0 transmit interrupt enable

BTIE      Basic timer interrupt enable

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### interrupt flag register 1 and 2

| Address | 7 | 6 | 5 | 4      | 3      | 2      | 1     | 0      |
|---------|---|---|---|--------|--------|--------|-------|--------|
| 02h     |   |   |   | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
|         |   |   |   | rw-0   | rw-(0) | rw-(1) | rw-1  | rw-(0) |

- WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on  $V_{CC}$  power-up or a reset condition at  $\overline{RST}$ /NMI pin in reset mode.
- OFIFG Flag set on oscillator fault
- RSTIFG External reset interrupt flag. Set on a reset condition at  $\overline{RST}$ /NMI pin in reset mode. Reset on  $V_{CC}$  power-up.
- PORIFG Power-on interrupt flag. Set on  $V_{CC}$  power-up.
- NMIIFG Set via  $\overline{RST}$ /NMI-pin

| Address | 7     | 6 | 5 | 4 | 3          | 2          | 1          | 0          |
|---------|-------|---|---|---|------------|------------|------------|------------|
| 03h     | BTIFG |   |   |   | UCB0 TXIFG | UCB0 RXIFG | UCA0 TXIFG | UCA0 RXIFG |
|         | rw-0  |   |   |   | rw-1       | rw-0       | rw-1       | rw-0       |

- UCA0RXIFG USCI\_A0 receive interrupt flag
- UCA0TXIFG USCI\_A0 transmit interrupt flag
- UCB0RXIFG USCI\_B0 receive interrupt flag
- UCB0TXIFG USCI\_B0 transmit interrupt flag
- BTIFG Basic Timer1 interrupt flag

- Legend**
- rw:** Bit can be read and written.
- rw-0,1:** Bit can be read and written. It is Reset or set by PUC.
- rw-(0,1):** Bit can be read and written. It is Reset or set by POR.

|  |                                  |
|--|----------------------------------|
|  | SFR bit is not present in device |
|--|----------------------------------|

## memory organization

|                        |           | MSP430F4152     | MSP430F4132     |
|------------------------|-----------|-----------------|-----------------|
| Memory                 | Size      | 16KB            | 8KB             |
| Main: interrupt vector | Flash     | 0FFFFh - 0FFE0h | 0FFFFh - 0FFE0h |
| Main: code memory      | Flash     | 0FFFFh - 0C000h | 0FFFFh - 0E000h |
| Information memory     | Size      | 256 Byte        | 256 Byte        |
|                        | Flash     | 010FFh - 01000h | 010FFh - 01000h |
| Boot memory            | Size      | 1KB             | 1KB             |
|                        | ROM       | 0FFFh - 0C00h   | 0FFFh - 0C00h   |
| RAM                    | Size      | 512B            | 512B            |
|                        |           | 03FFh - 0200h   | 03FFh - 0200h   |
| Peripherals            | 16-bit    | 01FFh - 0100h   | 01FFh - 0100h   |
|                        | 8-bit     | 0FFh - 010h     | 0FFh - 010h     |
|                        | 8-bit SFR | 0Fh - 00h       | 0Fh - 00h       |

## bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide*, literature number SLAU265.

| BSL FUNCTION  | PM PACKAGE PINS | RGZ PACKAGE PINS |
|---------------|-----------------|------------------|
| Data transmit | 53 - P1.0       | 37 - P1.0        |
| Data receive  | 52 - P1.1       | 36 - P1.1        |

## flash memory (Flash)

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.

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### peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*, literature number SLAU056.

### oscillator and system clock

The clock system in the MSP430F41x2 is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal very low-power low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and an 8-MHz high-frequency crystal oscillator (XT1). The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6  $\mu$ s. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or a very low-power LF oscillator
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

### brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However,  $V_{CC}$  may not have ramped to  $V_{CC(min)}$  at that time. The user must insure the default FLL+ settings are not changed until  $V_{CC}$  reaches  $V_{CC(min)}$ . If desired, the SVS circuit can be used to determine when  $V_{CC}$  reaches  $V_{CC(min)}$ .

### digital I/O

There are seven 8-bit I/O ports implemented—ports P1 through P7. Port P7 is a 7-bit I/O port.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

## watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

## Basic Timer1 and Real-Time Clock (RTC)

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for month with less than 31 days and includes leap year correction.

## LCD\_A driver with regulated charge pump

The LCD\_A driver generates the segment and common signals required to drive an LCD display. The LCD\_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and thus contrast in software.

## Timer0\_A3

Timer\_A3 is a 16-bit timer/counter with three capture/compare registers. Timer\_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_A3 SIGNAL CONNECTIONS |                        |                     |                   |              |                      |                   |                  |
|-----------------------------|------------------------|---------------------|-------------------|--------------|----------------------|-------------------|------------------|
| INPUT PIN NUMBER            |                        | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |                  |
| PM                          | RGZ                    |                     |                   |              |                      | PM                | RGZ              |
| 48 - P1.5<br>46 - P1.7      | 35 - P1.5<br>33 - P1.7 | TA0CLK              | TACLK             | Timer        | NA                   |                   |                  |
|                             |                        | ACLK                | ACLK              |              |                      |                   |                  |
|                             |                        | SMCLK               | SMCLK             |              |                      |                   |                  |
| 48 - P1.5                   | 35 - P1.5              | TA0CLK              | TACLK             | CCR0         | TA0                  |                   |                  |
| 53 - P1.0                   | 37 - P1.0              | TA0.0               | CCI0A             |              |                      | 53 - P1.0         | 37 - P1.0        |
| 52 - P1.1                   | 36 - P1.1              | TA0.0               | CCI0B             |              |                      | 32 - P3.3         | -                |
|                             |                        | DV <sub>SS</sub>    | GND               |              |                      |                   |                  |
|                             |                        | DV <sub>CC</sub>    | V <sub>CC</sub>   | CCR1         | TA1                  |                   |                  |
| 51 - P1.2                   | -                      | TA0.1               | CCI1A             |              |                      | 51 - P1.2         |                  |
|                             |                        | CAOUT (internal)    | CCI1B             |              |                      | ADC10 (internal)  | ADC10 (internal) |
|                             |                        | DV <sub>SS</sub>    | GND               |              |                      |                   |                  |
|                             |                        | DV <sub>CC</sub>    | V <sub>CC</sub>   | CCR2         | TA2                  |                   |                  |
| 45 - P7.6                   | -                      | TA0.2               | CCI2A             |              |                      | 45 - P7.6         | -                |
|                             |                        | ACLK (internal)     | CCI2B             |              |                      |                   |                  |
|                             |                        | DV <sub>SS</sub>    | GND               |              |                      |                   |                  |
|                             |                        | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |                  |

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## Timer1\_A5

Timer\_A5 is a 16-bit timer/counter with five capture/compare registers. Timer\_A5 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A5 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_A5 SIGNAL CONNECTIONS |           |                     |                   |              |                      |                   |                  |
|-----------------------------|-----------|---------------------|-------------------|--------------|----------------------|-------------------|------------------|
| INPUT PIN NUMBER            |           | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |                  |
| PM                          | RGZ       |                     |                   |              |                      | PM                | RGZ              |
| 32 – P3.3                   | -         | TA1CLK              | TACLK             | Timer        | NA                   |                   |                  |
|                             |           | ACLK                | ACLK              |              |                      |                   |                  |
|                             |           | SMCLK               | SMCLK             |              |                      |                   |                  |
| 32 – P3.3                   | -         | TA1CLK              | TACLK             |              |                      |                   |                  |
| 49 – P1.4                   | -         | TA1.0               | CCI0A             | CCR0         | TA0                  | 49 – P1.4         | -                |
| 50 – P1.3                   | -         | TA1.0               | CCI0B             |              |                      | ADC10 (internal)  | ADC10 (internal) |
|                             |           | DV <sub>SS</sub>    | GND               |              |                      |                   |                  |
|                             |           | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |                  |
| 44 – P5.0                   | -         | TA1.1               | CCI1A             | CCR1         | TA1                  | 44 – P5.0         | -                |
|                             |           | CAOUT (internal)    | CCI1B             |              |                      | 27 – P2.0         | 23 – P2.0        |
|                             |           | DV <sub>SS</sub>    | GND               |              |                      | ADC10 (internal)  | ADC10 (internal) |
|                             |           | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |                  |
| 35 – P3.0                   | -         | TA1.2               | CCI2A             | CCR2         | TA2                  | 35 – P3.0         | -                |
|                             |           | ACLK (internal)     | CCI2B             |              |                      | 26 – P2.1         | 22 – P2.1        |
|                             |           | DV <sub>SS</sub>    | GND               |              |                      | 63 – P6.0         | 47 – P6.0        |
|                             |           | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |                  |
| 34 – P3.1                   | -         | TA1.3               | CCI3A             | CCR3         | TA3                  | 34 – P3.1         | -                |
| 61 – P7.5                   | 45 – P7.5 | TA1.3               | CCI3B             |              |                      | 25 – P2.2         | 21 – P2.2        |
|                             |           | DV <sub>SS</sub>    | GND               |              |                      | 61 – P7.5         | 45 – P7.5        |
|                             |           | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |                  |
| 33 – P3.2                   | -         | TA1.4               | CCI4A             | CCR4         | TA4                  | 33 – P3.2         | -                |
| 60 – P7.4                   | 44 – P7.4 | TA1.4               | CCI4B             |              |                      | 24 – P2.3         | 20 – P2.3        |
|                             |           | DV <sub>SS</sub>    | GND               |              |                      | 60 – P7.4         | 44 – P7.4        |
|                             |           | DV <sub>CC</sub>    | V <sub>CC</sub>   |              |                      |                   |                  |

## universal serial communication interface (USCI) (USCI\_A0, USCI\_B0)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI\_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI\_B0 provides support for SPI (3 or 4 pin) and I2C.

## Comparator\_A+

The primary function of the comparator\_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.



## ADC10

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

### peripheral file map

| PERIPHERALS WITH WORD ACCESS |                                      |           |       |
|------------------------------|--------------------------------------|-----------|-------|
| <b>Watchdog</b>              | Watchdog timer control               | WDTCTL    | 0120h |
| <b>Timer0_A3</b>             | Capture/compare register 2           | TA0CCR2   | 0176h |
|                              | Capture/compare register 1           | TA0CCR1   | 0174h |
|                              | Capture/compare register 0           | TA0CCR0   | 0172h |
|                              | Timer_A register                     | TA0R      | 0170h |
|                              | Capture/compare control 2            | TA0CCTL2  | 0166h |
|                              | Capture/compare control 1            | TA0CCTL1  | 0164h |
|                              | Capture/compare control 0            | TA0CCTL0  | 0162h |
|                              | Timer_A control                      | TA0CTL    | 0160h |
|                              | Timer_A interrupt vector             | TA0IV     | 012Eh |
| <b>Timer1_A5</b>             | Capture/compare register 4           | TA1CCR4   | 019A  |
|                              | Capture/compare register 3           | TA1CCR3   | 0198  |
|                              | Capture/compare register 2           | TA1CCR2   | 0196h |
|                              | Capture/compare register 1           | TA1CCR1   | 0194h |
|                              | Capture/compare register 0           | TA1CCR0   | 0192h |
|                              | Timer_A register                     | TA1R      | 0190h |
|                              | Capture/compare control 4            | TA1CCTL4  | 018A  |
|                              | Capture/compare control 3            | TA1CCTL3  | 0188  |
|                              | Capture/compare control 2            | TA1CCTL2  | 0186h |
|                              | Capture/compare control 1            | TA1CCTL1  | 0184h |
|                              | Capture/compare control 0            | TA1CCTL0  | 0182h |
|                              | Timer_A control                      | TA1CTL    | 0180h |
|                              | Timer_A interrupt vector             | TA1IV     | 011Eh |
| <b>Flash</b>                 | Flash control 3                      | FCTL3     | 012Ch |
|                              | Flash control 2                      | FCTL2     | 012Ah |
|                              | Flash control 1                      | FCTL1     | 0128h |
| <b>ADC10</b>                 | ADC data transfer start address      | ADC10SA   | 01BCh |
|                              | ADC memory                           | ADC10MEM  | 01B4h |
|                              | ADC control register 1               | ADC10CTL1 | 01B2h |
|                              | ADC control register 0               | ADC10CTL0 | 01B0h |
|                              | ADC analog enable 0                  | ADC10AE0  | 004Ah |
|                              | ADC analog enable 1                  | ADC10AE1  | 004Bh |
|                              | ADC data transfer control register 1 | ADC10DTC1 | 0049h |
|                              | ADC data transfer control register 0 | ADC10DTC0 | 0048h |

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### peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS |                                                 |            |        |
|------------------------------|-------------------------------------------------|------------|--------|
| <b>LCD_A</b>                 | LCD Voltage Control 1                           | LCDVCTL1   | 0AFh   |
|                              | LCD Voltage Control 0                           | LCDVCTL0   | 0AEh   |
|                              | LCD Voltage Port Control 1                      | LCDAPCTL1  | 0ADh   |
|                              | LCD Voltage Port Control 0                      | LCDAPCTL0  | 0ACh   |
|                              | LCD memory 20                                   | LCDM20     | 0A4h   |
|                              | :                                               | :          | :      |
|                              | LCD memory 16                                   | LCDM16     | 0A0h   |
|                              | LCD memory 15                                   | LCDM15     | 09Fh   |
|                              | :                                               | :          | :      |
|                              | LCD memory 1                                    | LCDM1      | 091h   |
|                              | LCD control and mode                            | LCDACTL    | 090h   |
| <b>USCI A0/B0</b>            | USCI A0 auto baud rate control                  | UCA0ABCTL  | 0x005D |
|                              | USCI A0 transmit buffer                         | UCA0TXBUF  | 0x0067 |
|                              | USCI A0 receive buffer                          | UCA0RXBUF  | 0x0066 |
|                              | USCI A0 status                                  | UCA0STAT   | 0x0065 |
|                              | USCI A0 modulation control                      | UCA0MCTL   | 0x0064 |
|                              | USCI A0 baud rate control 1                     | UCA0BR1    | 0x0063 |
|                              | USCI A0 baud rate control 0                     | UCA0BR0    | 0x0062 |
|                              | USCI A0 control 1                               | UCA0CTL1   | 0x0061 |
|                              | USCI A0 control 0                               | UCA0CTL0   | 0x0060 |
|                              | USCI A0 IrDA receive control                    | UCA0IRRCTL | 0x005F |
|                              | USCI A0 IrDA transmit control                   | UCA0IRTCTL | 0x005E |
|                              | USCI B0 transmit buffer                         | UCB0TXBUF  | 0x006F |
|                              | USCI B0 receive buffer                          | UCB0RXBUF  | 0x006E |
|                              | USCI B0 status                                  | UCB0STAT   | 0x006D |
|                              | USCI B0 I2C Interrupt enable                    | UCB0CIE    | 0x006C |
|                              | USCI B0 baud rate control 1                     | UCB0BR1    | 0x006B |
|                              | USCI B0 baud rate control 0                     | UCB0BR0    | 0x006A |
|                              | USCI B0 control 1                               | UCB0CTL1   | 0x0069 |
|                              | USCI B0 control 0                               | UCB0CTL0   | 0x0068 |
|                              | USCI B0 I2C slave address                       | UCB0SA     | 0x011A |
|                              | USCI B0 I2C own address                         | UCB0OA     | 0x0118 |
| <b>Comparator_A+</b>         | Comparator_A port disable                       | CAPD       | 05Bh   |
|                              | Comparator_A control2                           | CACTL2     | 05Ah   |
|                              | Comparator_A control1                           | CACTL1     | 059h   |
| <b>Brownout, SVS</b>         | SVS control register (Reset by brownout signal) | SVSCTL     | 056h   |
| <b>FLL+ Clock</b>            | FLL+ Control 2                                  | FLL_CTL2   | 055h   |
|                              | FLL+ Control 1                                  | FLL_CTL1   | 054h   |
|                              | FLL+ Control 0                                  | FLL_CTL0   | 053h   |
|                              | System clock frequency control                  | SCFQCTL    | 052h   |
|                              | System clock frequency integrator               | SCFI1      | 051h   |
|                              | System clock frequency integrator               | SCFI0      | 050h   |



**peripheral file map (continued)**

| <b>PERIPHERALS WITH BYTE ACCESS</b> |                                |           |      |
|-------------------------------------|--------------------------------|-----------|------|
| <b>RTC<br/>(Basic Timer1)</b>       | Real Time Clock Year High Byte | RTCYEARH  | 04Fh |
|                                     | Real Time Clock Year Low Byte  | RTCYEARL  | 04Eh |
|                                     | Real Time Clock Month          | RTCMON    | 04Dh |
|                                     | Real Time Clock Day of Month   | RTCDAY    | 04Ch |
|                                     | Basic Timer1 Counter           | BTCNT2    | 047h |
|                                     | Basic Timer1 Counter           | BTCNT1    | 046h |
|                                     | Real Time Counter 4            | RTCNT4    | 045h |
|                                     | (Real Time Clock Day of Week)  | (RTCDOW)  |      |
|                                     | Real Time Counter 3            | RTCNT3    | 044h |
|                                     | (Real Time Clock Hour)         | (RTCHOUR) |      |
|                                     | Real Time Counter 2            | RTCNT2    | 043h |
|                                     | (Real Time Clock Minute)       | (RTCMIN)  |      |
|                                     | Real Time Counter 1            | RTCNT1    | 042h |
|                                     | (Real Time Clock Second)       | (RTCSEC)  |      |
|                                     | Real Time Clock Control        | RTCCTL    | 041h |
|                                     | Basic Timer1 Control           | BTCTL     | 040h |
| <b>Port P7</b>                      | Port P7 selection              | P7SEL     | 03Bh |
|                                     | Port P7 direction              | P7DIR     | 03Ah |
|                                     | Port P7 output                 | P7OUT     | 039h |
|                                     | Port P7 input                  | P7IN      | 038h |
| <b>Port P6</b>                      | Port P6 selection              | P6SEL     | 037h |
|                                     | Port P6 direction              | P6DIR     | 036h |
|                                     | Port P6 output                 | P6OUT     | 035h |
|                                     | Port P6 input                  | P6IN      | 034h |
| <b>Port P5</b>                      | Port P5 selection              | P5SEL     | 033h |
|                                     | Port P5 direction              | P5DIR     | 032h |
|                                     | Port P5 output                 | P5OUT     | 031h |
|                                     | Port P5 input                  | P5IN      | 030h |
| <b>Port P4</b>                      | Port P4 selection              | P4SEL     | 01Fh |
|                                     | Port P4 direction              | P4DIR     | 01Eh |
|                                     | Port P4 output                 | P4OUT     | 01Dh |
|                                     | Port P4 input                  | P4IN      | 01Ch |
| <b>Port P3</b>                      | Port P3 selection              | P3SEL     | 01Bh |
|                                     | Port P3 direction              | P3DIR     | 01Ah |
|                                     | Port P3 output                 | P3OUT     | 019h |
|                                     | Port P3 input                  | P3IN      | 018h |
| <b>Port P2</b>                      | Port P2 selection              | P2SEL     | 02Eh |
|                                     | Port P2 interrupt enable       | P2IE      | 02Dh |
|                                     | Port P2 interrupt-edge select  | P2IES     | 02Ch |
|                                     | Port P2 interrupt flag         | P2IFG     | 02Bh |
|                                     | Port P2 direction              | P2DIR     | 02Ah |
|                                     | Port P2 output                 | P2OUT     | 029h |
|                                     | Port P2 input                  | P2IN      | 028h |

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## MIXED SIGNAL MICROCONTROLLER

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### peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) |                               |       |      |
|------------------------------------------|-------------------------------|-------|------|
| <b>Port P1</b>                           | Port P1 selection register    | P1SEL | 026h |
|                                          | Port P1 interrupt enable      | P1IE  | 025h |
|                                          | Port P1 interrupt-edge select | P1IES | 024h |
|                                          | Port P1 interrupt flag        | P1IFG | 023h |
|                                          | Port P1 direction             | P1DIR | 022h |
|                                          | Port P1 output                | P1OUT | 021h |
|                                          | Port P1 input                 | P1IN  | 020h |
| <b>Special functions</b>                 | SFR interrupt flag 2          | IFG2  | 003h |
|                                          | SFR interrupt flag 1          | IFG1  | 002h |
|                                          | SFR interrupt enable 2        | IE2   | 001h |
|                                          | SFR interrupt enable 1        | IE1   | 000h |

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**

|                                                      |                            |
|------------------------------------------------------|----------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$              | -0.3 V to 4.1 V            |
| Voltage applied to any pin (see Note 1)              | -0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device terminal                 | $\pm 2$ mA                 |
| Storage temperature, $T_{stg}$ : Unprogrammed device | -55°C to 150°C             |
| Programmed device                                    | -55°C to 85°C              |

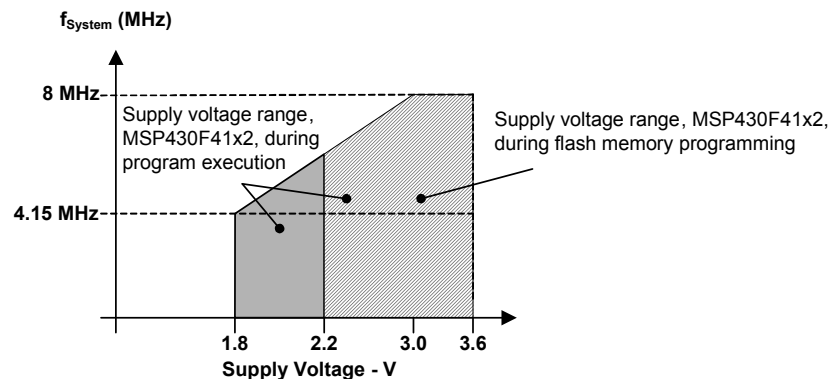
<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

**recommended operating conditions**

|                                                                                           |                                 |                   | MIN              | NOM | MAX  | UNIT |
|-------------------------------------------------------------------------------------------|---------------------------------|-------------------|------------------|-----|------|------|
| Supply voltage during program execution, $V_{CC}$ ( $AV_{CC} = DV_{CC} = V_{CC}$ )        |                                 |                   | 1.8              |     | 3.6  | V    |
| Supply voltage during flash memory programming, $V_{CC}$ ( $AV_{CC} = DV_{CC} = V_{CC}$ ) |                                 |                   | 2.2              |     | 3.6  | V    |
| Supply voltage, $V_{SS}$ ( $AV_{SS} = DV_{SS} = V_{SS}$ )                                 |                                 |                   | 0                |     | 0    | V    |
| Operating free-air temperature range, $T_A$                                               |                                 |                   | -40              |     | 85   | °C   |
| LFXT1 crystal frequency, $f_{(LFXT1)}$<br>(see Note 1)                                    | LF selected,<br>$XTS\_FLL = 0$  | Watch crystal     | 32.768           |     |      | kHz  |
|                                                                                           | XT1 selected,<br>$XTS\_FLL = 1$ | Ceramic resonator | 0.45             |     | 6    | MHz  |
|                                                                                           | XT1 selected,<br>$XTS\_FLL = 1$ | Crystal           | 1                |     | 6    | MHz  |
| Processor frequency (signal MCLK), $f_{(System)}$                                         |                                 |                   | $V_{CC} = 1.8$ V | dc  | 4.15 | MHz  |
|                                                                                           |                                 |                   | $V_{CC} = 3.0$ V | dc  | 8    |      |

NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.



**Figure 1. Frequency vs Supply Voltage**

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## MIXED SIGNAL MICROCONTROLLER

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**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**supply current into  $AV_{CC}$  +  $DV_{CC}$  excluding external current**

| PARAMETER    |                                                                                                                                                                                                                                                                      | $T_A$                                     | $V_{CC}$ | MIN | TYP  | MAX | UNIT          |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|----------|-----|------|-----|---------------|
| $I_{(AM)}$   | Active mode (see Note 1),<br>$f_{(MCLK)} = f_{(SMCLK)} = 1 \text{ MHz}$ ,<br>$f_{(ACLK)} = 32768 \text{ Hz}$ ,<br>$XTS=0$ , $SELM=(0,1)$                                                                                                                             | $-40^\circ\text{C}$ to $85^\circ\text{C}$ | 2.2 V    |     | 220  | 295 | $\mu\text{A}$ |
|              |                                                                                                                                                                                                                                                                      |                                           | 3 V      |     | 350  | 398 |               |
| $I_{(LPM0)}$ | Low-power mode 0 (LPM0) (see Note 1)                                                                                                                                                                                                                                 | $-40^\circ\text{C}$ to $85^\circ\text{C}$ | 2.2 V    |     | 33   | 60  | $\mu\text{A}$ |
|              |                                                                                                                                                                                                                                                                      |                                           | 3 V      |     | 50   | 92  |               |
| $I_{(LPM2)}$ | Low-power mode 2 (LPM2),<br>$f_{(MCLK)} = f_{(SMCLK)} = 0 \text{ MHz}$ ,<br>$f_{(ACLK)} = 32768 \text{ Hz}$ , $SCG0 = 0$ (see Note 2)                                                                                                                                | $-40^\circ\text{C}$ to $85^\circ\text{C}$ | 2.2 V    |     | 6    | 13  | $\mu\text{A}$ |
|              |                                                                                                                                                                                                                                                                      |                                           | 3 V      |     | 7    | 15  |               |
| $I_{(LPM3)}$ | Low-power mode 3 (LPM3),<br>$f_{(MCLK)} = f_{(SMCLK)} = 0 \text{ MHz}$ ,<br>$f_{(ACLK)} = 32768 \text{ Hz}$ , $SCG0 = 1$ ,<br>Basic Timer1 enabled, ACLK selected,<br>LCD_A enabled, LCDPEN = 0,<br>(static mode, $f_{LCD} = f_{(ACLK)}/32$ )<br>(see Notes 2 and 3) | $-40^\circ\text{C}$                       | 2.2 V    |     | 0.85 | 1.4 | $\mu\text{A}$ |
|              |                                                                                                                                                                                                                                                                      | $25^\circ\text{C}$                        |          |     | 0.90 | 1.2 |               |
|              |                                                                                                                                                                                                                                                                      | $60^\circ\text{C}$                        |          |     | 1.15 | 1.4 |               |
|              |                                                                                                                                                                                                                                                                      | $85^\circ\text{C}$                        |          |     | 2.15 | 3.0 |               |
|              |                                                                                                                                                                                                                                                                      | $-40^\circ\text{C}$                       | 3 V      |     | 1.0  | 1.5 |               |
|              |                                                                                                                                                                                                                                                                      | $25^\circ\text{C}$                        |          |     | 1.1  | 1.5 |               |
|              |                                                                                                                                                                                                                                                                      | $60^\circ\text{C}$                        |          |     | 1.4  | 1.9 |               |
|              |                                                                                                                                                                                                                                                                      | $85^\circ\text{C}$                        |          |     | 2.5  | 3.5 |               |
| $I_{(LPM3)}$ | Low-power mode 3 (LPM3),<br>$f_{(MCLK)} = f_{(SMCLK)} = 0 \text{ MHz}$ ,<br>$f_{(ACLK)} = 32768 \text{ Hz}$ , $SCG0 = 1$ ,<br>Basic Timer1 enabled, ACLK selected,<br>LCD_A enabled, LCDPEN = 0,<br>(4-mux mode, $f_{LCD} = f_{(ACLK)}/32$ )<br>(see Notes 2 and 3)  | $-40^\circ\text{C}$                       | 2.2 V    |     | 1.8  | 3.3 | $\mu\text{A}$ |
|              |                                                                                                                                                                                                                                                                      | $25^\circ\text{C}$                        |          |     | 2.1  | 3.2 |               |
|              |                                                                                                                                                                                                                                                                      | $85^\circ\text{C}$                        |          |     | 3.6  | 5.0 |               |
|              |                                                                                                                                                                                                                                                                      | $-40^\circ\text{C}$                       | 3 V      |     | 2.1  | 3.6 |               |
|              |                                                                                                                                                                                                                                                                      | $25^\circ\text{C}$                        |          |     | 2.3  | 3.6 |               |
|              |                                                                                                                                                                                                                                                                      | $85^\circ\text{C}$                        |          |     | 4.1  | 5.5 |               |
| $I_{(LPM4)}$ | Low-power mode 4 (LPM4),<br>$f_{(MCLK)} = 0 \text{ MHz}$ , $f_{(SMCLK)} = 0 \text{ MHz}$ ,<br>$f_{(ACLK)} = 0 \text{ Hz}$ , $SCG0 = 1$ (see Note 2)                                                                                                                  | $-40^\circ\text{C}$                       | 2.2 V    |     | 0.1  | 0.5 | $\mu\text{A}$ |
|              |                                                                                                                                                                                                                                                                      | $25^\circ\text{C}$                        |          |     | 0.1  | 0.5 |               |
|              |                                                                                                                                                                                                                                                                      | $60^\circ\text{C}$                        |          |     | 0.35 | 0.9 |               |
|              |                                                                                                                                                                                                                                                                      | $85^\circ\text{C}$                        |          |     | 1.1  | 2.5 |               |
|              |                                                                                                                                                                                                                                                                      | $-40^\circ\text{C}$                       | 3 V      |     | 0.1  | 0.8 |               |
|              |                                                                                                                                                                                                                                                                      | $25^\circ\text{C}$                        |          |     | 0.1  | 0.8 |               |
|              |                                                                                                                                                                                                                                                                      | $60^\circ\text{C}$                        |          |     | 0.8  | 1.2 |               |
|              |                                                                                                                                                                                                                                                                      | $85^\circ\text{C}$                        |          |     | 1.9  | 3.5 |               |

NOTES: 1. Timer\_A is clocked by  $f_{(DCOCLK)} = 1 \text{ MHz}$ . All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.  
2. All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.  
3. The LPM3 currents are characterized with a Micro Crystal CC4V-T1A (9 pF) crystal and OSCCAPx = 01h.

typical characteristics - LPM4 current

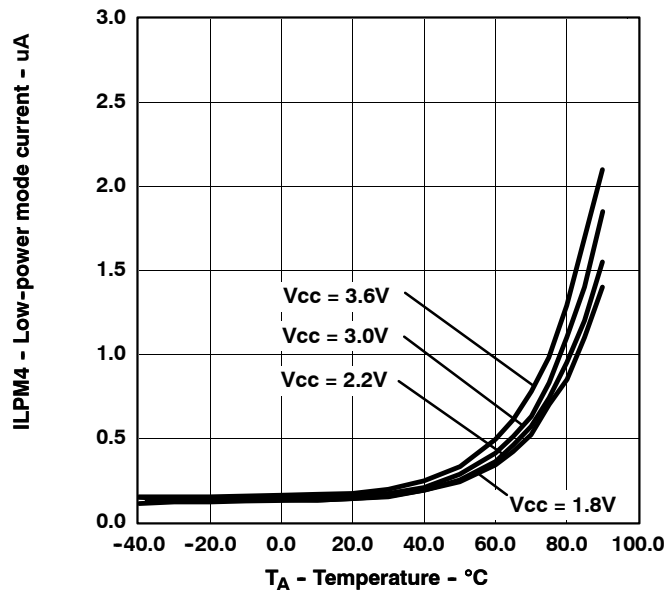


Figure 2.  $I_{LPM4}$  - LPM4 Current vs Temperature

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## MIXED SIGNAL MICROCONTROLLER

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**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**Schmitt-trigger inputs - ports P1, P2, P3, P4, P5, P6, and P7,  $\overline{\text{RST}}$ /NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)**

| PARAMETER        |                                                                 | V <sub>CC</sub> | MIN | MAX  | UNIT |
|------------------|-----------------------------------------------------------------|-----------------|-----|------|------|
| V <sub>IT+</sub> | Positive-going input threshold voltage                          | 2.2 V           | 1.1 | 1.55 | V    |
|                  |                                                                 | 3 V             | 1.5 | 1.98 |      |
| V <sub>IT-</sub> | Negative-going input threshold voltage                          | 2.2 V           | 0.4 | 0.9  | V    |
|                  |                                                                 | 3 V             | 0.9 | 1.3  |      |
| V <sub>hys</sub> | Input voltage hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> ) | 2.2 V           | 0.3 | 1.1  | V    |
|                  |                                                                 | 3 V             | 0.5 | 1    |      |

**inputs Px.y, TA<sub>x</sub>**

| PARAMETER            |                                                   | TEST CONDITIONS                                                                        | V <sub>CC</sub> | MIN | MAX | UNIT |
|----------------------|---------------------------------------------------|----------------------------------------------------------------------------------------|-----------------|-----|-----|------|
| t <sub>(int)</sub>   | External interrupt timing                         | Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag (see Note 1) | 2.2 V           | 62  |     | ns   |
|                      |                                                   |                                                                                        | 3 V             | 50  |     |      |
| t <sub>(cap)</sub>   | Timer_A capture timing                            | TA0, TA1, TA2                                                                          | 2.2 V           | 62  |     | ns   |
|                      |                                                   |                                                                                        | 3 V             | 50  |     |      |
| f <sub>(TAext)</sub> | Timer_A clock frequency externally applied to pin | TACLK, INCLK: t <sub>(H)</sub> = t <sub>(L)</sub>                                      | 2.2 V           |     | 8   | MHz  |
|                      |                                                   |                                                                                        | 3 V             |     | 10  |      |
| f <sub>(TAint)</sub> | Timer_A, clock frequency                          | SMCLK or ACLK signal selected                                                          | 2.2 V           |     | 8   | MHz  |
|                      |                                                   |                                                                                        | 3 V             |     | 10  |      |

NOTES: 1. The external signal sets the interrupt flag every time the minimum t<sub>(int)</sub> parameters are met. It may be set even with trigger signals shorter than t<sub>(int)</sub>.

**leakage current - ports P1, P2, P3, P4, P5, P6, and P7 (see Note 1)**

| PARAMETER              |                 | TEST CONDITIONS                          | V <sub>CC</sub> | MIN | MAX | UNIT |
|------------------------|-----------------|------------------------------------------|-----------------|-----|-----|------|
| I <sub>lkg(Px.y)</sub> | Leakage current | Port Px V <sub>(Px.y)</sub> (see Note 2) | 2.2 V/3 V       |     | ±50 | nA   |

NOTES: 1. The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.  
2. The port pin must be selected as input.



**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**outputs - ports P1, P2, P3, P4, P5, P6, and P7**

| PARAMETER                                 | TEST CONDITIONS                                                      | MIN                   | MAX                   | UNIT |
|-------------------------------------------|----------------------------------------------------------------------|-----------------------|-----------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>OH(max)</sub> = -1.5 mA, V <sub>CC</sub> = 2.2 V (see Note 1) | V <sub>CC</sub> -0.25 | V <sub>CC</sub>       | V    |
|                                           | I <sub>OH(max)</sub> = -6 mA, V <sub>CC</sub> = 2.2 V (see Note 2)   | V <sub>CC</sub> -0.6  | V <sub>CC</sub>       |      |
|                                           | I <sub>OH(max)</sub> = -1.5 mA, V <sub>CC</sub> = 3 V (see Note 1)   | V <sub>CC</sub> -0.25 | V <sub>CC</sub>       |      |
|                                           | I <sub>OH(max)</sub> = -6 mA, V <sub>CC</sub> = 3 V (see Note 2)     | V <sub>CC</sub> -0.6  | V <sub>CC</sub>       |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>OL(max)</sub> = 1.5 mA, V <sub>CC</sub> = 2.2 V (see Note 1)  | V <sub>SS</sub>       | V <sub>SS</sub> +0.25 | V    |
|                                           | I <sub>OL(max)</sub> = 6 mA, V <sub>CC</sub> = 2.2 V (see Note 2)    | V <sub>SS</sub>       | V <sub>SS</sub> +0.6  |      |
|                                           | I <sub>OL(max)</sub> = 1.5 mA, V <sub>CC</sub> = 3 V (see Note 1)    | V <sub>SS</sub>       | V <sub>SS</sub> +0.25 |      |
|                                           | I <sub>OL(max)</sub> = 6 mA, V <sub>CC</sub> = 3 V (see Note 2)      | V <sub>SS</sub>       | V <sub>SS</sub> +0.6  |      |

NOTES: 1. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.  
2. The maximum total current, I<sub>OH(max)</sub> and I<sub>OL(max)</sub>, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

**output frequency**

| PARAMETER                                                | TEST CONDITIONS                                                                  | MIN                                         | TYP | MAX                 | UNIT                 |
|----------------------------------------------------------|----------------------------------------------------------------------------------|---------------------------------------------|-----|---------------------|----------------------|
| f <sub>(Px.y)</sub> (x = 1, 2, 3, 4, 5, 6, 7, 0 ≤ y ≤ 7) | C <sub>L</sub> = 20 pF, I <sub>L</sub> = ±1.5 mA V <sub>CC</sub> = 2.2 V / 3 V   | dc                                          |     | f <sub>System</sub> | MHz                  |
| f <sub>(MCLK)</sub> P1.1/TA0.0/MCLK/S30                  | C <sub>L</sub> = 20 pF                                                           |                                             |     | f <sub>System</sub> | MHz                  |
| t <sub>(Xdc)</sub> Duty cycle of output frequency        | P1.1/TA0.0/MCLK/S30,<br>C <sub>L</sub> = 20 pF,<br>V <sub>CC</sub> = 2.2 V / 3 V | f <sub>(MCLK)</sub> = f <sub>(XT1)</sub>    |     | 40%                 | 60%                  |
|                                                          |                                                                                  | f <sub>(MCLK)</sub> = f <sub>(DCOCLK)</sub> |     | 50%-<br>15 ns       | 50%<br>50%+<br>15 ns |

# MSP430F41x2 MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs - ports Px (continued)

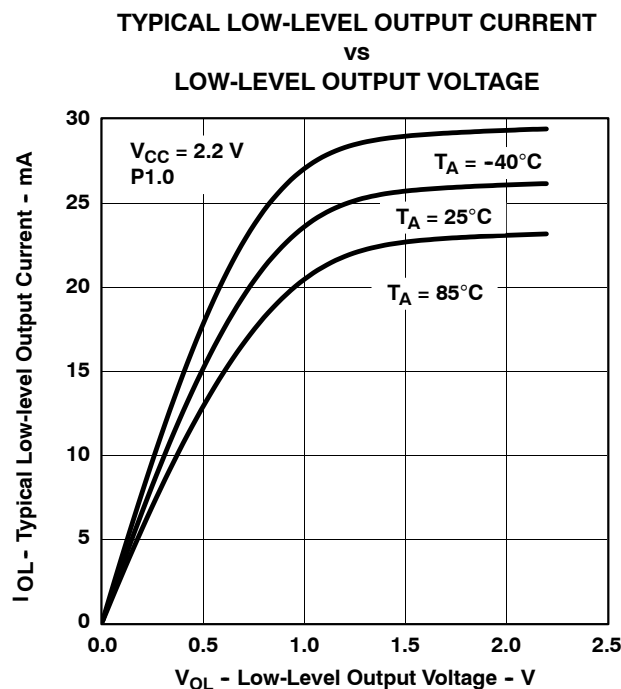


Figure 3

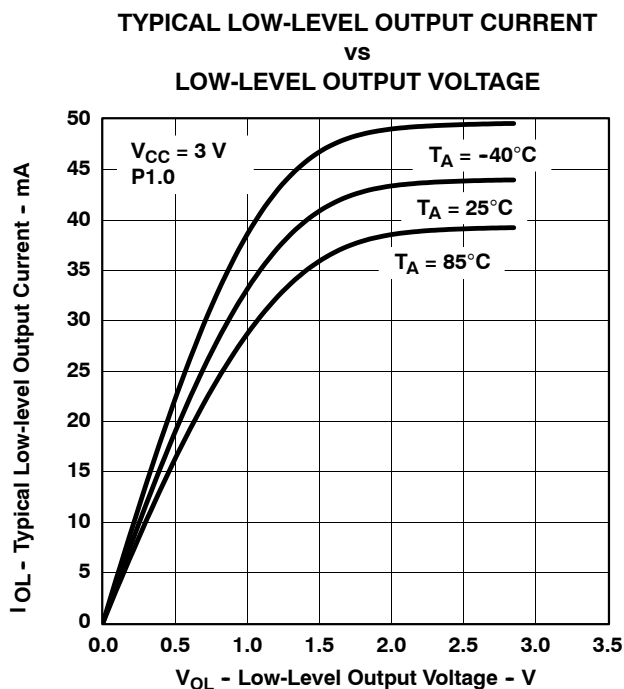


Figure 4

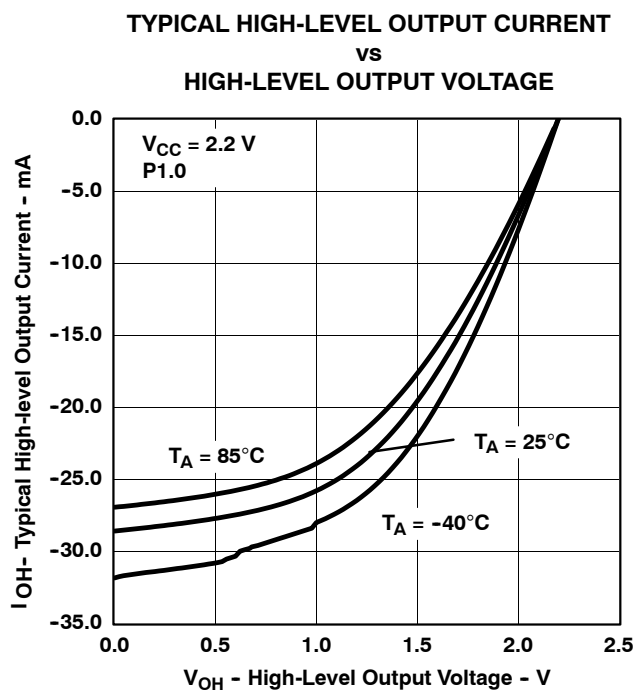


Figure 5

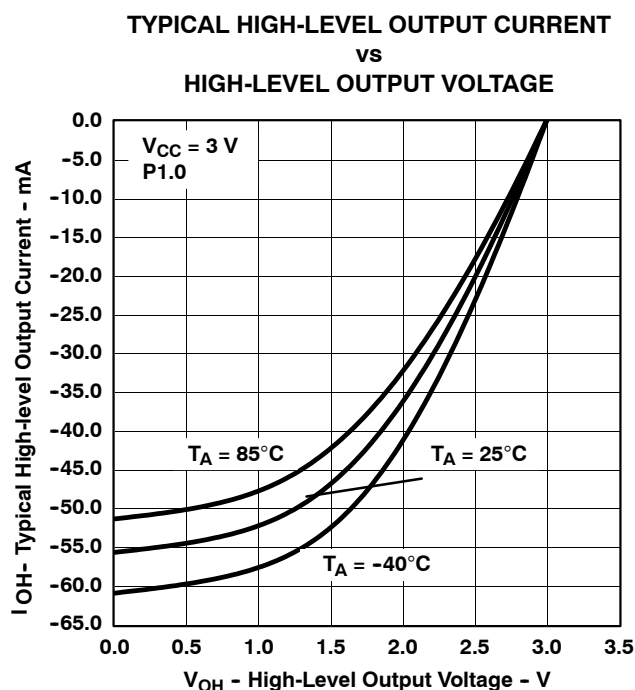


Figure 6

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**wake-up LPM3**

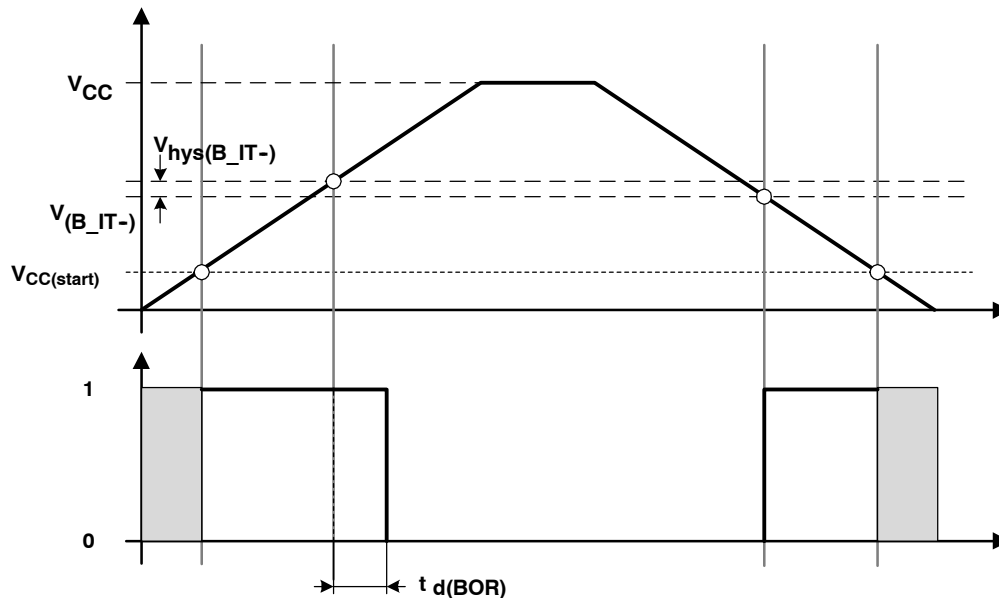
| PARAMETER     |            | TEST CONDITIONS     |                                      | MIN | MAX | UNIT          |
|---------------|------------|---------------------|--------------------------------------|-----|-----|---------------|
| $t_{d(LPM3)}$ | Delay time | $f = 1 \text{ MHz}$ | $V_{CC} = 2.2 \text{ V}/3 \text{ V}$ |     | 6   | $\mu\text{s}$ |
|               |            | $f = 2 \text{ MHz}$ |                                      |     | 6   |               |
|               |            | $f = 3 \text{ MHz}$ |                                      |     | 6   |               |

**POR/brownout reset (BOR) (see Note 1)**

| PARAMETER         |                          | TEST CONDITIONS                                                                                          | MIN | TYP                       | MAX  | UNIT          |
|-------------------|--------------------------|----------------------------------------------------------------------------------------------------------|-----|---------------------------|------|---------------|
| $t_{d(BOR)}$      | Brownout<br>(see Note 2) |                                                                                                          |     |                           | 2000 | $\mu\text{s}$ |
| $V_{CC(start)}$   |                          | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 7)                                                           |     | $0.7 \times V_{(B\_IT-)}$ |      | V             |
| $V_{(B\_IT-)}$    |                          | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 7)                                                           |     |                           | 1.71 | V             |
| $V_{hys(B\_IT-)}$ |                          | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 7)                                                           |     |                           |      | mV            |
| $t_{(reset)}$     |                          | Pulse length needed at RST/NMI pin to accepted reset internally,<br>$V_{CC} = 2.2 \text{ V}/3 \text{ V}$ | 2   |                           |      | $\mu\text{s}$ |

- NOTES: 1. The current consumption of the brownout module is already included in the  $I_{CC}$  current consumption data. The voltage level  $V_{(B\_IT-)} + V_{hys(B\_IT-)} \leq 1.8\text{V}$ .
2. During power up, the CPU begins code execution following a period of  $t_{d(BOR)}$  after  $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$ . The default FLL+ settings must not be changed until  $V_{CC} \geq V_{CC(min)}$ , where  $V_{CC(min)}$  is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout.

**typical characteristics**



**Figure 7. POR/Brownout Reset (BOR) vs Supply Voltage**

# MSP430F41x2 MIXED SIGNAL MICROCONTROLLER

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics (continued)

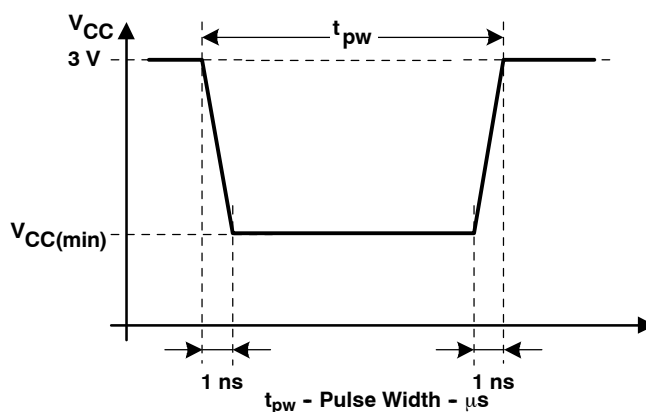
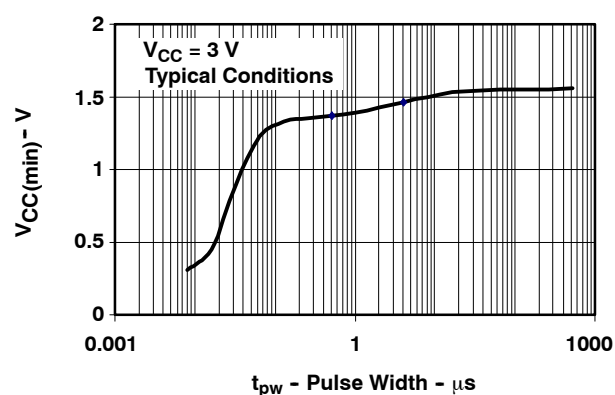


Figure 8.  $V_{CC(min)}$  Level With a Square Voltage Drop to Generate a POR/Brownout Signal

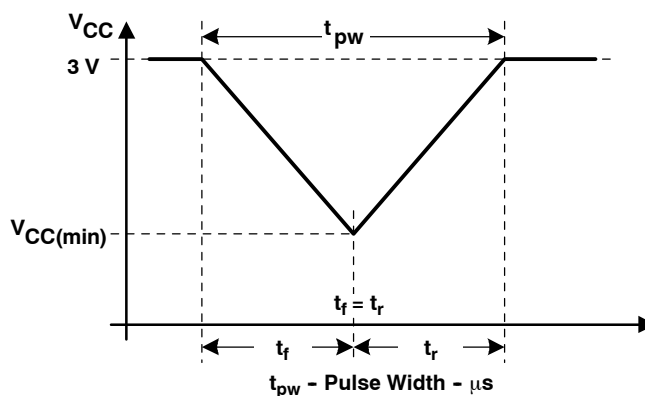
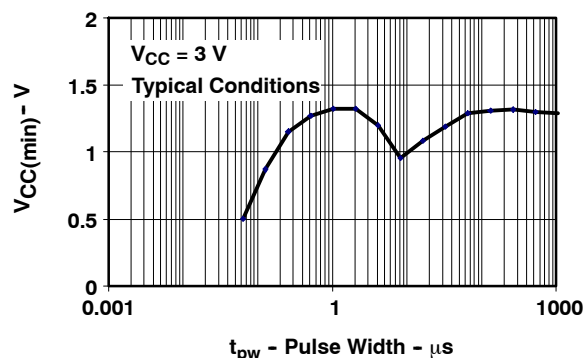


Figure 9.  $V_{CC(min)}$  Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**SVS (supply voltage supervisor/monitor)**

| PARAMETER                     | TEST CONDITIONS                                                                                 |               | MIN                           | TYP              | MAX                           | UNIT          |
|-------------------------------|-------------------------------------------------------------------------------------------------|---------------|-------------------------------|------------------|-------------------------------|---------------|
| $t_{(SVSR)}$                  | $dV_{CC}/dt > 30 \text{ V/ms}$ (see Figure 10)                                                  |               | 5                             |                  | 150                           | $\mu\text{s}$ |
|                               | $dV_{CC}/dt \leq 30 \text{ V/ms}$                                                               |               |                               |                  | 2000                          | $\mu\text{s}$ |
| $t_{d(SVSON)}$                | SVSON, switch from VLD = 0 to VLD $\neq$ 0, $V_{CC} = 3 \text{ V}$                              |               |                               | 150              | 300                           | $\mu\text{s}$ |
| $t_{\text{settle}}$           | VLD $\neq$ 0 <sup>†</sup>                                                                       |               |                               |                  | 12                            | $\mu\text{s}$ |
| $V_{(SVSstart)}$              | VLD $\neq$ 0, $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10)                                    |               |                               | 1.55             | 1.7                           | V             |
| $V_{\text{hys}(SVS\_IT-)}$    | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10)                                                  | VLD = 1       | 70                            | 120              | 210                           | mV            |
|                               |                                                                                                 | VLD = 2 to 14 | $V_{(SVS\_IT-)} \times 0.001$ |                  | $V_{(SVS\_IT-)} \times 0.016$ |               |
|                               | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10),<br>External voltage applied on A7               | VLD = 15      | 4.4                           |                  | 20                            | mV            |
| $V_{(SVS\_IT-)}$              | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10 and Figure 11)                                    | VLD = 1       | 1.8                           | 1.9              | 2.05                          | V             |
|                               |                                                                                                 | VLD = 2       | 1.94                          | 2.1              | 2.25                          |               |
|                               |                                                                                                 | VLD = 3       | 2.05                          | 2.2              | 2.37                          |               |
|                               |                                                                                                 | VLD = 4       | 2.14                          | 2.3              | 2.48                          |               |
|                               |                                                                                                 | VLD = 5       | 2.24                          | 2.4              | 2.6                           |               |
|                               |                                                                                                 | VLD = 6       | 2.33                          | 2.5              | 2.71                          |               |
|                               |                                                                                                 | VLD = 7       | 2.46                          | 2.65             | 2.86                          |               |
|                               |                                                                                                 | VLD = 8       | 2.58                          | 2.8              | 3                             |               |
|                               |                                                                                                 | VLD = 9       | 2.69                          | 2.9              | 3.13                          |               |
|                               |                                                                                                 | VLD = 10      | 2.83                          | 3.05             | 3.29                          |               |
|                               |                                                                                                 | VLD = 11      | 2.94                          | 3.2              | 3.42                          |               |
|                               |                                                                                                 | VLD = 12      | 3.11                          | 3.35             | 3.61 <sup>†</sup>             |               |
|                               |                                                                                                 | VLD = 13      | 3.24                          | 3.5              | 3.76 <sup>†</sup>             |               |
|                               |                                                                                                 | VLD = 14      | 3.43                          | 3.7 <sup>†</sup> | 3.99 <sup>†</sup>             |               |
|                               | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 10 and Figure 11),<br>External voltage applied on A7 | VLD = 15      | 1.1                           | 1.2              | 1.3                           |               |
| $I_{CC(SVS)}$<br>(see Note 1) | VLD $\neq$ 0, $V_{CC} = 2.2 \text{ V}/3 \text{ V}$                                              |               |                               | 10               | 15                            | $\mu\text{A}$ |

<sup>†</sup> The recommended operating voltage range is limited to 3.6 V.

<sup>‡</sup>  $t_{\text{settle}}$  is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD  $\neq$  0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be  $> 50 \text{ mV}$ .

NOTE 1: The current consumption of the SVS module is not included in the  $I_{CC}$  current consumption data.

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## typical characteristics

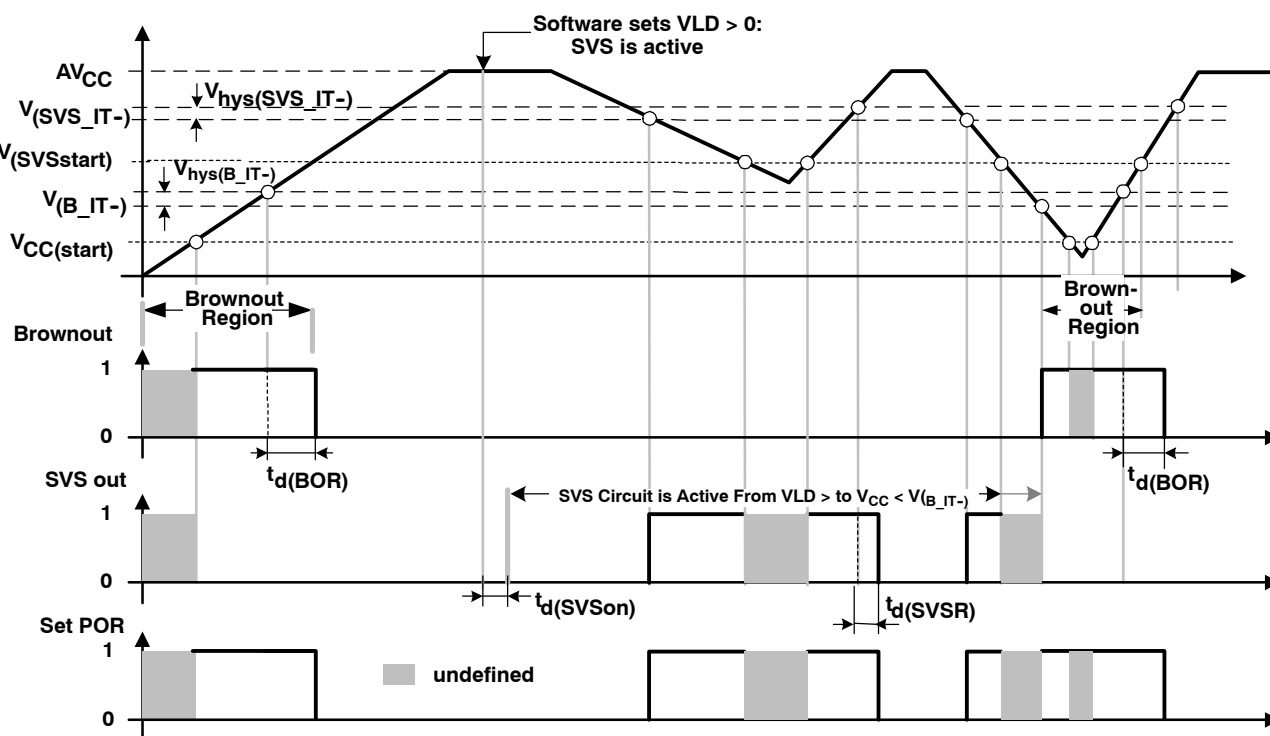


Figure 10. SVS Reset (SVSR) vs Supply Voltage

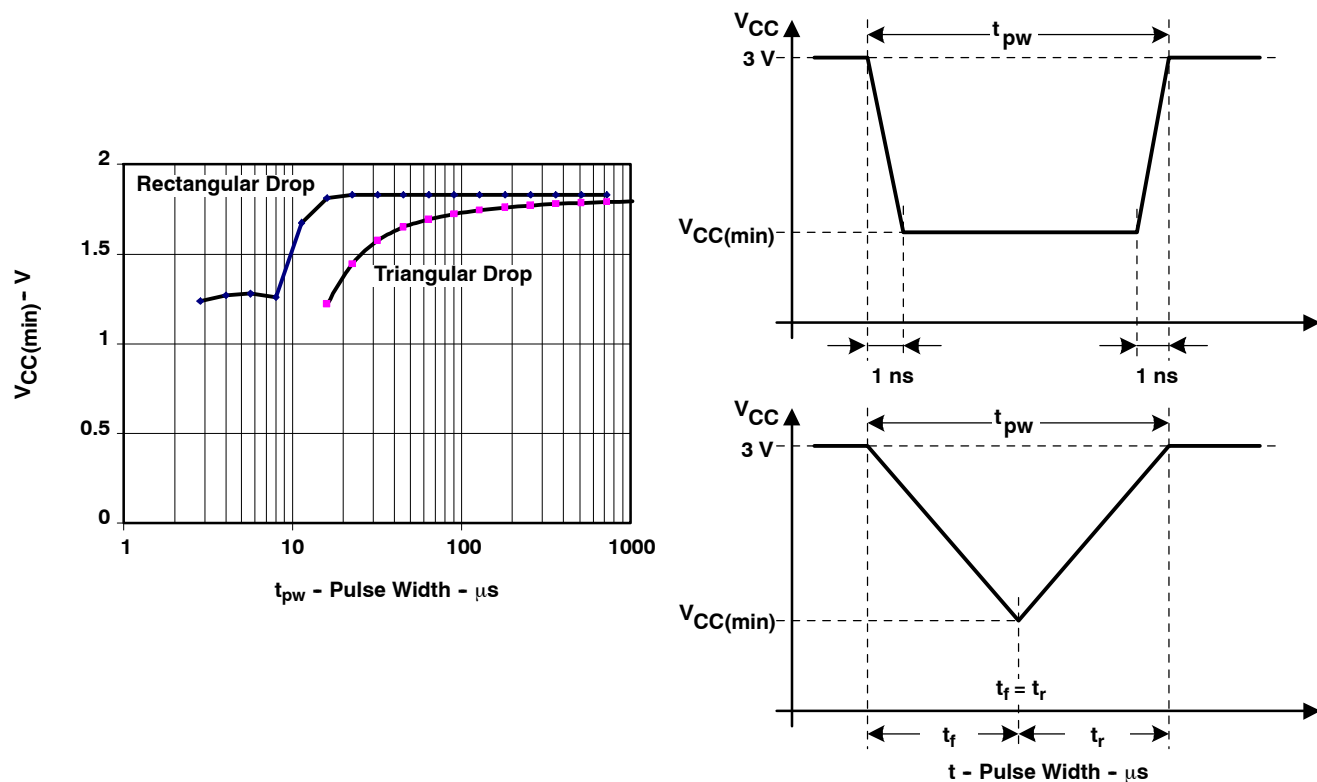


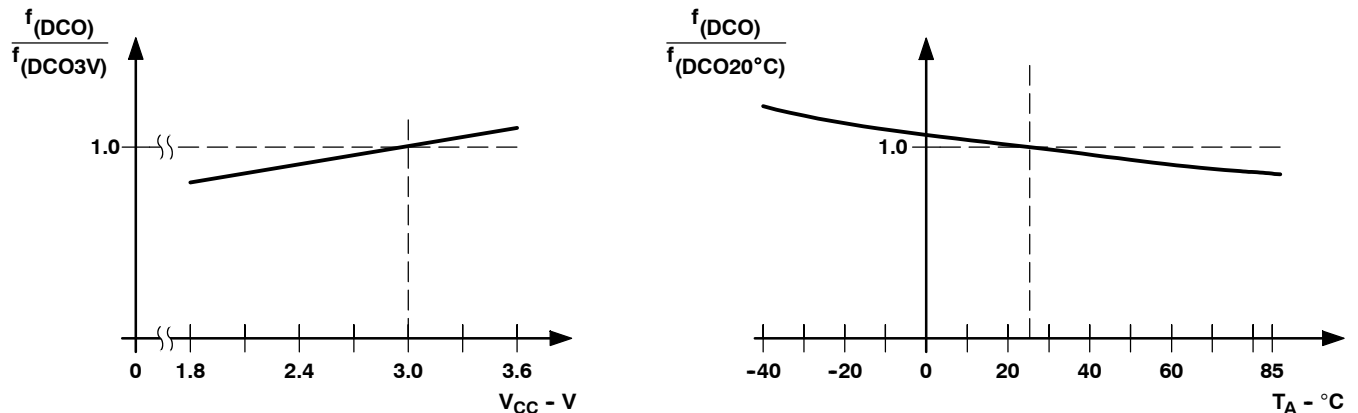
Figure 11.  $V_{CC(min)}$ : Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal ( $VLD = 1$ )

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**DCO**

| PARAMETER             | TEST CONDITIONS                                                                                                                                                 | V <sub>CC</sub> | MIN  | TYP  | MAX  | UNIT |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|------|------|------|
| f <sub>(DCOCLK)</sub> | N <sub>(DCO)</sub> = 01E0h, FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, D = 2, DCOPLUS = 0                                       | 2.2 V/3 V       | 1    |      |      | MHz  |
| f <sub>(DCO2)</sub>   | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, DCOPLUS = 1                                                                          | 2.2 V           | 0.3  | 0.65 | 1.25 | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 0.3  | 0.7  | 1.3  |      |
| f <sub>(DCO27)</sub>  | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, DCOPLUS = 1 (see Note 1)                                                             | 2.2 V           | 2.5  | 5.6  | 10.5 | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 2.7  | 6.1  | 11.3 |      |
| f <sub>(DCO2)</sub>   | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = 0, FN <sub>2</sub> = 1, DCOPLUS = 1                                                                       | 2.2 V           | 0.7  | 1.3  | 2.3  | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 0.8  | 1.5  | 2.5  |      |
| f <sub>(DCO27)</sub>  | FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = 0, FN <sub>2</sub> = 1, DCOPLUS = 1 (see Note 1)                                                          | 2.2 V           | 5.7  | 10.8 | 18   | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 6.5  | 12.1 | 20   |      |
| f <sub>(DCO2)</sub>   | FN <sub>8</sub> = FN <sub>4</sub> = 0, FN <sub>3</sub> = 1, FN <sub>2</sub> = x, DCOPLUS = 1                                                                    | 2.2 V           | 1.2  | 2    | 3    | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 1.3  | 2.2  | 3.5  |      |
| f <sub>(DCO27)</sub>  | FN <sub>8</sub> = FN <sub>4</sub> = 0, FN <sub>3</sub> = 1, FN <sub>2</sub> = x, DCOPLUS = 1 (see Note 1)                                                       | 2.2 V           | 9    | 15.5 | 25   | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 10.3 | 17.9 | 28.5 |      |
| f <sub>(DCO2)</sub>   | FN <sub>8</sub> = 0, FN <sub>4</sub> = 1, FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1                                                                    | 2.2 V           | 1.8  | 2.8  | 4.2  | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 2.1  | 3.4  | 5.2  |      |
| f <sub>(DCO27)</sub>  | FN <sub>8</sub> = 0, FN <sub>4</sub> = 1, FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1 (see Note 1)                                                       | 2.2 V           | 13.5 | 21.5 | 33   | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 16   | 26.6 | 41   |      |
| f <sub>(DCO2)</sub>   | FN <sub>8</sub> = 1, FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1                                                                       | 2.2 V           | 2.8  | 4.2  | 6.2  | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 4.2  | 6.3  | 9.2  |      |
| f <sub>(DCO27)</sub>  | FN <sub>8</sub> = 1, FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = x, DCOPLUS = 1 (see Note 1)                                                          | 2.2 V           | 21   | 32   | 46   | MHz  |
|                       |                                                                                                                                                                 | 3 V             | 30   | 46   | 70   |      |
| S <sub>n</sub>        | Step size between adjacent DCO taps:<br>S <sub>n</sub> = f <sub>DCO(Tap n+1)</sub> / f <sub>DCO(Tap n)</sub> , (see Figure 13 for taps 21 to 27)                | 1 < TAP ≤ 20    | 1.06 |      | 1.11 |      |
|                       |                                                                                                                                                                 | TAP = 27        | 1.07 |      | 1.17 |      |
| D <sub>t</sub>        | Temperature drift, N <sub>(DCO)</sub> = 01E0h, FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, D = 2, DCOPLUS = 0                    | 2.2 V           | -0.2 | -0.4 | -0.6 | %/°C |
|                       |                                                                                                                                                                 | 3 V             | -0.2 | -0.4 | -0.6 |      |
| D <sub>V</sub>        | Drift with V <sub>CC</sub> variation, N <sub>(DCO)</sub> = 01E0h, FN <sub>8</sub> = FN <sub>4</sub> = FN <sub>3</sub> = FN <sub>2</sub> = 0, D = 2, DCOPLUS = 0 |                 | 0    | 5    | 15   | %/V  |

NOTES: 1. Do not exceed the maximum system frequency.



**Figure 12. DCO Frequency vs Supply Voltage V<sub>CC</sub> and vs Ambient Temperature**

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

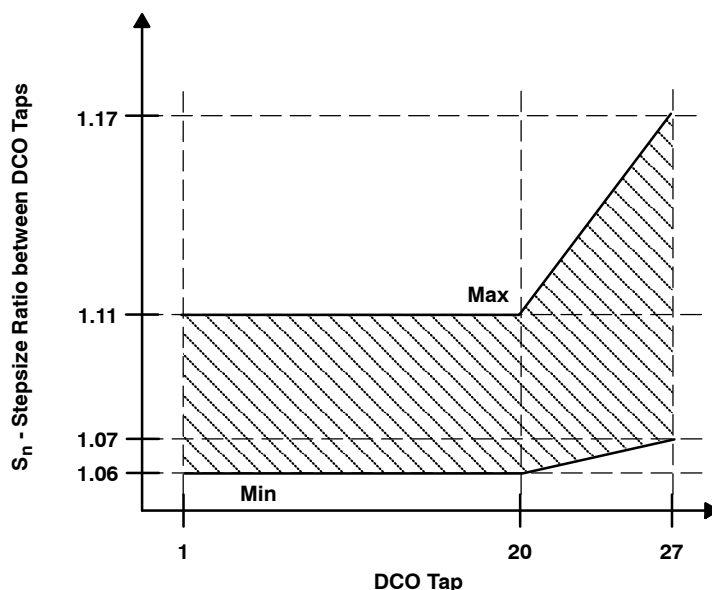


Figure 13. DCO Tap Step Size

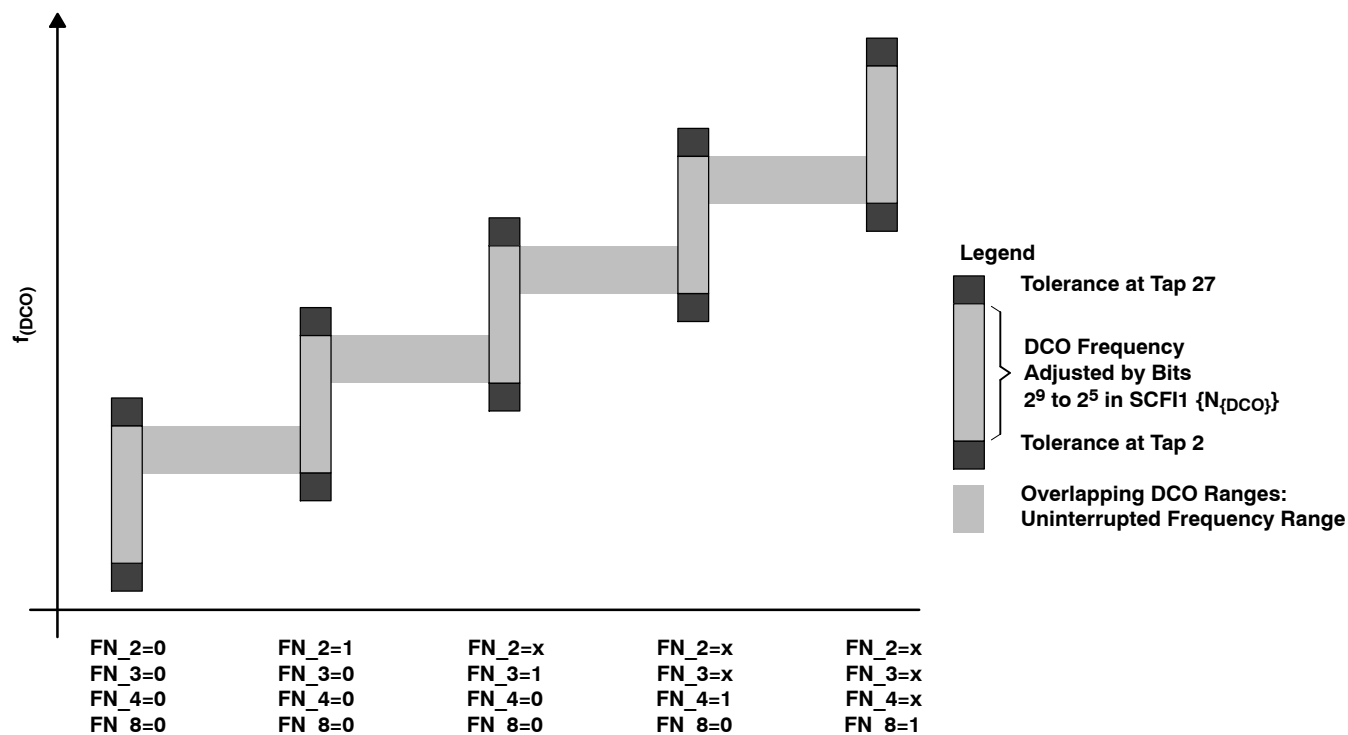


Figure 14. Five Overlapping DCO Ranges Controlled by FN\_x Bits

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

**crystal oscillator, LFXT1, low-frequency modes (see Note 4)**

| PARAMETER             |                                                             | TEST CONDITIONS                                                                     | V <sub>CC</sub> | MIN | TYP   | MAX   | UNIT |
|-----------------------|-------------------------------------------------------------|-------------------------------------------------------------------------------------|-----------------|-----|-------|-------|------|
| f <sub>LFXT1,LF</sub> | LFXT1 oscillator crystal frequency, LF mode 0, 1            | XTS = 0, LFXT1Sx = 0 or 1                                                           | 1.8 V to 3.6 V  |     | 32768 |       | Hz   |
| OA <sub>LF</sub>      | Oscillation allowance for LF crystals                       | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 kHz, C <sub>L,eff</sub> = 6 pF  |                 |     | 500   |       | kΩ   |
|                       |                                                             | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 kHz, C <sub>L,eff</sub> = 12 pF |                 |     | 200   |       |      |
| C <sub>L,eff</sub>    | Integrated effective load capacitance, LF mode (see Note 1) | XTS = 0, XCAPx = 0                                                                  |                 |     | 1     |       | pF   |
|                       |                                                             | XTS = 0, XCAPx = 1                                                                  |                 |     | 5.5   |       |      |
|                       |                                                             | XTS = 0, XCAPx = 2                                                                  |                 |     | 8.5   |       |      |
|                       |                                                             | XTS = 0, XCAPx = 3                                                                  |                 |     | 11    |       |      |
| Duty cycle            | LF mode                                                     | XTS = 0, Measured at P1.6/ACLK, f <sub>LFXT1,LF</sub> = 32768Hz                     | 2.2 V/3 V       | 30  | 50    | 70    | %    |
| f <sub>Fault,LF</sub> | Oscillator fault frequency, LF mode (see Note 3)            | XTS = 0, XCAPx = 0, LFXT1Sx = 3 (see Note 2)                                        | 2.2 V/3 V       | 10  |       | 10000 | Hz   |

- NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

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## MIXED SIGNAL MICROCONTROLLER

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**electrical characteristics over recommended operating free-air temperature (unless otherwise noted)**

### crystal oscillator, LFXT1, high frequency modes

| PARAMETER                                                                      | TEST CONDITIONS       | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT |
|--------------------------------------------------------------------------------|-----------------------|-----------------|------|-----|-----|------|
| f <sub>LFXT1</sub> LFXT1 oscillator crystal frequency                          | Ceramic resonator     | 1.8 V to 3.6 V  | 0.45 |     | 6   | MHz  |
|                                                                                | Crystal resonator     | 1.8 V to 3.6 V  | 1    |     | 6   |      |
| C <sub>L,eff</sub> Integrated effective load capacitance, HF mode (see Note 1) | See Note 2            |                 |      | 1   |     | pF   |
| Duty cycle                                                                     | Measured at P1.6/ACLK | 2.2 V/3 V       | 40   | 50  | 60  | %    |

- NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
 Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

### internal very low power, low-frequency oscillator (VLO)

| PARAMETER                                                              | TEST CONDITIONS                | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------|--------------------------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub> VLO frequency                                         | T <sub>A</sub> = -40°C to 85°C | 2.2 V/3 V       | 4   | 12  | 20  | kHz  |
| df <sub>VLO</sub> /dT VLO frequency temperature drift                  | See Note                       | 2.2 V/3 V       |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> VLO frequency supply voltage drift | See Note 2                     | 1.8 V to 3.6 V  |     | 4   |     | %/V  |

- NOTES: 1. Calculated using the box method:  
 I Version: (MAX(-40°C to 85°C) - MIN(-40°C to 85°C))/MIN(-40°C to 85°C)/(85°C - (-40°C))
2. Calculated using the box method: (MAX(1.8 V to 3.6 V) - MIN(1.8 V to 3.6 V))/MIN(1.8 V to 3.6 V)/(3.6 V - 1.8 V)

### RAM

| PARAMETER        | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|-----------------|-----|-----|------|
| VRAMh See Note 1 | CPU halted      | 1.6 |     | V    |

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.



**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**LCD\_A**

| PARAMETER            |                                     | TEST CONDITIONS                                                                                                                                                                 | V <sub>CC</sub> | MIN | TYP             | MAX  | UNIT |
|----------------------|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----------------|------|------|
| V <sub>CC(LCD)</sub> | Supply voltage range                | Charge pump enabled<br>(LCDCPEN = 1, VLCDx > 0000)                                                                                                                              |                 | 2.2 |                 | 3.6  | V    |
| C <sub>LCD</sub>     | Capacitor on LCDCAP (see Note 1)    | Charge pump enabled<br>(LCDCPEN = 1, VLCDx > 0000)                                                                                                                              |                 | 4.7 |                 |      | μF   |
| I <sub>CC(LCD)</sub> | Average supply current (see Note 2) | V <sub>LCD(typ)</sub> = 3V, LCDCPEN = 1,<br>VLCDx = 1000, all segments on<br>f <sub>LCD</sub> = f <sub>ACLK</sub> /32<br>no LCD connected (see Note 3)<br>T <sub>A</sub> = 25°C | 2.2 V           |     | 3.8             |      | μA   |
| f <sub>LCD</sub>     | LCD frequency                       |                                                                                                                                                                                 |                 |     |                 | 1.1  | kHz  |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0000                                                                                                                                                                    |                 |     | V <sub>CC</sub> |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0001                                                                                                                                                                    |                 |     | 2.60            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0010                                                                                                                                                                    |                 |     | 2.66            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0011                                                                                                                                                                    |                 |     | 2.72            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0100                                                                                                                                                                    |                 |     | 2.78            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0101                                                                                                                                                                    |                 |     | 2.84            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0110                                                                                                                                                                    |                 |     | 2.90            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 0111                                                                                                                                                                    |                 |     | 2.96            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1000                                                                                                                                                                    |                 |     | 3.02            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1001                                                                                                                                                                    |                 |     | 3.08            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1010                                                                                                                                                                    |                 |     | 3.14            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1011                                                                                                                                                                    |                 |     | 3.20            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1100                                                                                                                                                                    |                 |     | 3.26            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1101                                                                                                                                                                    |                 |     | 3.32            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1110                                                                                                                                                                    |                 |     | 3.38            |      | V    |
| V <sub>LCD</sub>     | LCD voltage                         | VLCDx = 1111                                                                                                                                                                    |                 |     | 3.44            | 3.60 | V    |
| R <sub>LCD</sub>     | LCD driver output impedance         | V <sub>LCD</sub> = 3 V, LCDCPEN = 1,<br>VLCDx = 1000, I <sub>LOAD</sub> = ±10 μA                                                                                                | 2.2 V           |     |                 | 10   | kΩ   |

- NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.  
2. Refer to the supply current specifications I<sub>(LPM3)</sub> for additional current specifications with the LCD\_A module active.  
3. Connecting an actual display will increase the current consumption depending on the size of the LCD.

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**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

### Comparator\_A+ (see Note 1)

| PARAMETER                                      |                                                             | TEST CONDITIONS                                                                                | V <sub>CC</sub> | MIN  | TYP                | MAX  | UNIT |
|------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------------------------------------------|-----------------|------|--------------------|------|------|
| I <sub>(CC)</sub>                              |                                                             | CAON = 1, CARSEL = 0, CAREF = 0                                                                | 2.2 V           | 25   |                    | 40   | μA   |
|                                                |                                                             |                                                                                                | 3 V             | 45   |                    | 60   |      |
| I <sub>(Refladder/RefDiode)</sub>              |                                                             | CAON = 1, CARSEL = 0, CAREF = 1/2/3,<br>No load at P1.6/CA0 and P1.7/CA1                       | 2.2 V           | 30   |                    | 50   | μA   |
|                                                |                                                             |                                                                                                | 3 V             | 45   |                    | 80   |      |
| V <sub>(Ref025)</sub>                          | $\frac{\text{Voltage @ } 0.25 V_{CC} \text{ node}}{V_{CC}}$ | PCA0 = 1, CARSEL = 1, CAREF = 1,<br>No load at P1.6/CA0 and P1.7/CA1                           | 2.2 V / 3 V     | 0.23 | 0.24               | 0.25 |      |
| V <sub>(Ref050)</sub>                          | $\frac{\text{Voltage @ } 0.5 V_{CC} \text{ node}}{V_{CC}}$  | PCA0 = 1, CARSEL = 1, CAREF = 2,<br>No load at P1.6/CA0 and P1.7/CA1                           | 2.2V / 3 V      | 0.47 | 0.48               | 0.5  |      |
| V <sub>(RefVT)</sub>                           | See Figure 15 and<br>Figure 16                              | PCA0 = 1, CARSEL = 1, CAREF = 3,<br>No load at P1.6/CA0 and P1.7/CA1,<br>T <sub>A</sub> = 85°C | 2.2 V           | 390  | 480                | 540  | mV   |
|                                                |                                                             |                                                                                                | 3 V             | 400  | 490                | 550  |      |
| V <sub>IC</sub>                                | Common-mode input<br>voltage range                          | CAON = 1                                                                                       | 2.2 V / 3 V     | 0    | V <sub>CC</sub> -1 |      | V    |
| V <sub>p</sub> -V <sub>S</sub>                 | Offset voltage                                              | See Note 2                                                                                     | 2.2 V / 3 V     | -30  | 30                 |      | mV   |
| V <sub>hys</sub>                               | Input hysteresis                                            | CAON = 1                                                                                       | 2.2 V / 3 V     | 0    | 0.7                | 1.4  | mV   |
| t <sub>(response LH and HL)</sub> (see Note 3) |                                                             | T <sub>A</sub> = 25°C,<br>Overdrive 10 mV, without filter: CAF = 0                             | 2.2 V           | 80   | 165                | 300  | ns   |
|                                                |                                                             |                                                                                                | 3 V             | 70   | 120                | 240  |      |
|                                                |                                                             | T <sub>A</sub> = 25°C<br>Overdrive 10 mV, with filter: CAF = 1                                 | 2.2 V           | 1.4  | 1.9                | 2.8  | μs   |
|                                                |                                                             |                                                                                                | 3 V             | 0.9  | 1.5                | 2.2  |      |

- NOTES: 1. The leakage current for the Comparator\_A terminals is identical to I<sub>lkg(Px.x)</sub> specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator\_A inputs on successive measurements. The two successive measurements are then summed together.
3. The response time is measured at P1.6/CA0 with an input voltage step and the Comparator\_A already enabled (CAON=1). If CAON is set at the same time, a settling time of up to 300ns is added to the response time.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics

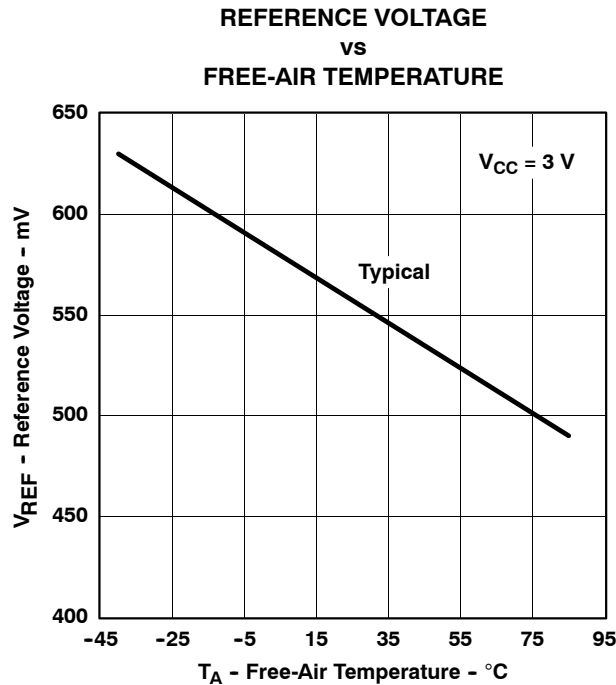


Figure 15. V<sub>(RefVT)</sub> vs Temperature

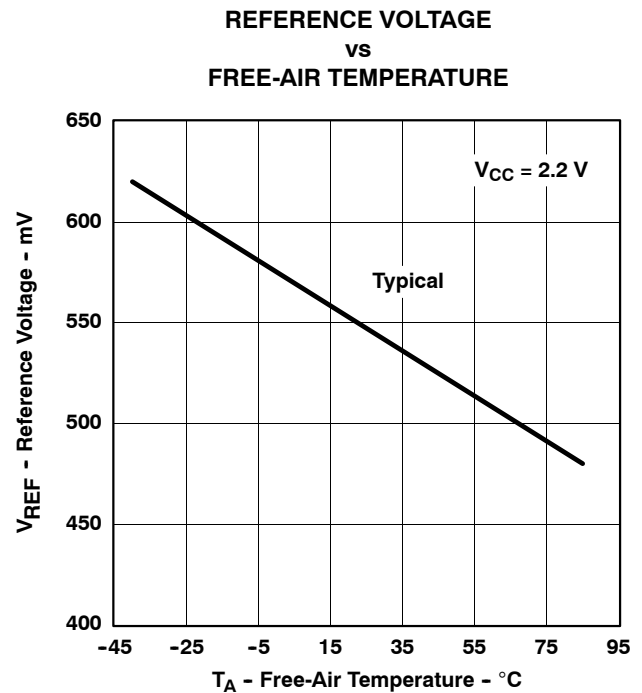


Figure 16. V<sub>(RefVT)</sub> vs Temperature

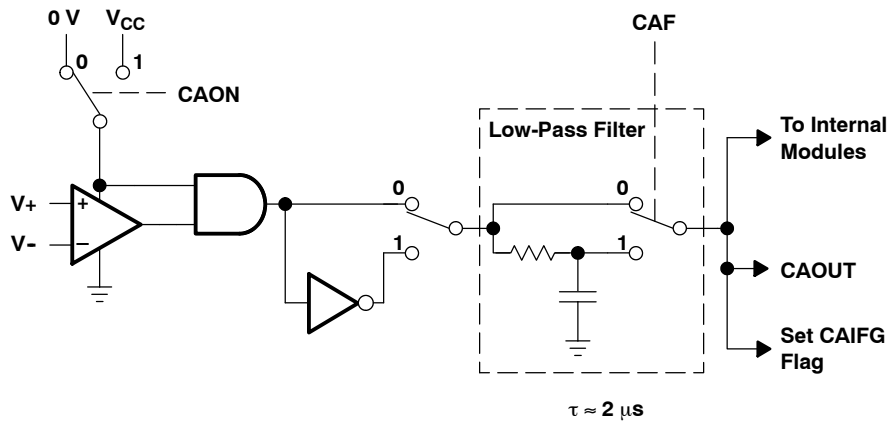


Figure 17. Block Diagram of Comparator\_A Module

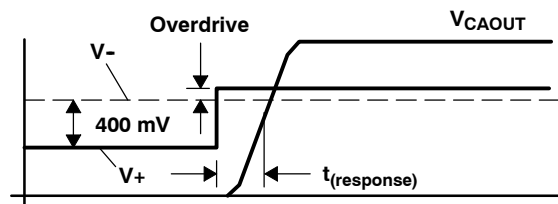


Figure 18. Overdrive Definition

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## MIXED SIGNAL MICROCONTROLLER

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**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

### 10-bit ADC, power supply and input range conditions (see Note )

| PARAMETER                                                                          | TEST CONDITIONS                                                                                            | V <sub>CC</sub> | MIN | TYP  | MAX             | UNIT |
|------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----------------|-----|------|-----------------|------|
| V <sub>CC</sub> Analog supply voltage range                                        | V <sub>SS</sub> = 0 V                                                                                      |                 | 2.2 |      | 3.6             | V    |
| V <sub>AX</sub> Analog input voltage range (see Note 2)                            | All Ax terminals,<br>Analog inputs selected in ADC10AE register                                            |                 | 0   |      | V <sub>CC</sub> | V    |
| I <sub>ADC10</sub> ADC10 supply current (see Note 3)                               | f <sub>ADC10CLK</sub> = 5 MHz,<br>ADC10ON = 1, REFON = 0<br>ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0     | 2.2 V           |     | 0.52 | 1.05            | mA   |
|                                                                                    |                                                                                                            | 3 V             |     | 0.6  | 1.2             |      |
| I <sub>REF+</sub> Reference supply current, reference buffer disabled (see Note 4) | f <sub>ADC10CLK</sub> = 5 MHz,<br>ADC10ON = 0, REF2_5V = 0,<br>REFON = 1, REFOUT = 0                       | 2.2 V/3 V       |     | 0.25 | 0.4             | mA   |
|                                                                                    | f <sub>ADC10CLK</sub> = 5 MHz,<br>ADC10ON = 0, REF2_5V = 1,<br>REFON = 1, REFOUT = 0                       | 3 V             |     |      |                 | mA   |
| I <sub>REFB,0</sub> Reference buffer supply current with ADC10SR = 0 (see Note 4)  | f <sub>ADC10CLK</sub> = 5 MHz,<br>ADC10ON = 0,<br>REFON = 1, REF2_5V = 0,<br>REFOUT = 1,<br>ADC10SR = 0    | 2.2 V/3 V       |     | 1.1  | 1.4             | mA   |
|                                                                                    |                                                                                                            | 2.2 V/3 V       |     |      | 1.8             | mA   |
| I <sub>REFB,1</sub> Reference buffer supply current with ADC10SR = 1 (see Note 4)  | f <sub>ADC10CLK</sub> = 5 MHz,<br>ADC10ON = 0,<br>REFON = 1,<br>REF2_5V = 0,<br>REFOUT = 1,<br>ADC10SR = 1 | 2.2 V/3 V       |     | 0.5  | 0.7             | mA   |
|                                                                                    |                                                                                                            | 2.2 V/3 V       |     |      | 0.8             | mA   |
| C <sub>I</sub> Input capacitance                                                   | Only one terminal Ax selected at a time                                                                    |                 |     |      | 27              | pF   |
| R <sub>I</sub> Input MUX ON resistance                                             | 0V ≤ V <sub>AX</sub> ≤ V <sub>CC</sub>                                                                     | 2.2 V/3 V       |     |      | 2000            | Ω    |

- NOTES: 1. The leakage current is defined in the leakage current table with Px.x/Ax parameter.  
2. The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results.  
3. The internal reference supply current is not included in current consumption parameter I<sub>ADC10</sub>.  
4. The internal reference current is supplied via terminal V<sub>CC</sub>. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**10-bit ADC, built-in voltage reference**

| PARAMETER                                       |                                                          | TEST CONDITIONS                                                                                                         |             | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT   |
|-------------------------------------------------|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-------------|-----------------|------|-----|------|--------|
| V <sub>CC,REF+</sub>                            | Positive built-in reference analog supply voltage range  | I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 0                                                                                  |             |                 | 2.2  |     |      | V      |
|                                                 |                                                          | I <sub>VREF+</sub> ≤ 0.5 mA, REF2_5V = 1                                                                                |             |                 | 2.8  |     |      |        |
|                                                 |                                                          | I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 1                                                                                  |             |                 | 2.9  |     |      |        |
| V <sub>REF+</sub>                               | Positive built-in reference voltage                      | I <sub>VREF+</sub> ≤ I <sub>VREF+,max</sub> , REF2_5V = 0                                                               |             | 2.2 V/<br>3 V   | 1.41 | 1.5 | 1.59 | V      |
|                                                 |                                                          | I <sub>VREF+</sub> ≤ I <sub>VREF+,max</sub> , REF2_5V = 1                                                               |             | 3 V             | 2.35 | 2.5 | 2.65 | V      |
| I <sub>LD,VREF+</sub>                           | Maximum V <sub>REF+</sub> load current                   |                                                                                                                         |             | 2.2 V           |      |     | ±0.5 | mA     |
|                                                 |                                                          |                                                                                                                         |             | 3 V             |      |     | ±1   |        |
| V <sub>REF+</sub> load regulation               |                                                          | I <sub>VREF+</sub> = 500 µA ± 100 µA,<br>Analog input voltage V <sub>AX</sub> ≈ 0.75 V,<br>REF2_5V = 0                  |             | 2.2 V/<br>3 V   |      |     | ±2   | LSB    |
|                                                 |                                                          | I <sub>VREF+</sub> = 500 µA ± 100 µA,<br>Analog input voltage V <sub>AX</sub> ≈ 1.25 V,<br>REF2_5V = 1                  |             | 3 V             |      |     | ±2   | LSB    |
| V <sub>REF+</sub> load regulation response time |                                                          | I <sub>VREF+</sub> = 100 µA → 900 µA,<br>V <sub>AX</sub> ≈ 0.5 × V <sub>REF+</sub> , Error of conversion result ≤ 1 LSB | ADC10SR = 0 | 3 V             |      |     | 400  | ns     |
|                                                 |                                                          |                                                                                                                         | ADC10SR = 1 | 3V              |      |     | 2000 |        |
| C <sub>VREF+</sub>                              | Max. capacitance at pin V <sub>REF+</sub> (see Note 1)   | I <sub>VREF+</sub> ≤ ±1 mA,<br>REFON = 1, REFOUT = 1                                                                    |             | 2.2 V/<br>3 V   |      |     | 100  | pF     |
| TC <sub>REF+</sub>                              | Temperature coefficient                                  | I <sub>VREF+</sub> = const. with 0 mA ≤ I <sub>VREF+</sub> ≤ 1 mA (see Note 3)                                          |             | 2.2 V/<br>3 V   |      |     | ±100 | ppm/°C |
| t <sub>REFON</sub>                              | Settling time of internal reference voltage (see Note 2) | I <sub>VREF+</sub> = 0.5 mA, REF2_5V = 0,<br>REFON = 0 → 1                                                              |             | 3.6 V           |      |     | 30   | µs     |
| t <sub>REFBURST</sub>                           | Settling time of reference buffer (see Note 2)           | I <sub>VREF+</sub> = 0.5 mA,<br>REF2_5V = 0,<br>REFON = 1,<br>REFBURST = 1                                              | ADC10SR = 0 | 2.2 V           |      |     | 1    | µs     |
|                                                 |                                                          |                                                                                                                         | ADC10SR = 1 | 2.2 V           |      |     | 2.5  |        |
|                                                 |                                                          | I <sub>VREF+</sub> = 0.5 mA,<br>REF2_5V = 1,<br>REFON = 1,<br>REFBURST = 1                                              | ADC10SR = 0 | 3 V             |      |     | 2    |        |
|                                                 |                                                          |                                                                                                                         | ADC10SR = 1 | 3 V             |      |     | 4.5  |        |

NOTES: 1. The capacitance applied to the internal buffer operational amplifier, if switched to terminal P6.4/UCB0CLK/UCAOSTE/A4/CA6/V<sub>ref+</sub>/V<sub>ref+</sub> (REFOUT = 1), must be limited; the reference buffer may become unstable, otherwise.

2. The condition is that the error in a conversion started after t<sub>REFON</sub> or t<sub>RefBuf</sub> is less than ±0.5 LSB.

3. Calculated using the box method: ((MAX(V<sub>REF</sub>(T)) - MIN(V<sub>REF</sub>(T))) / MIN(V<sub>REF</sub>(T))) / (T<sub>MAX</sub> - T<sub>MIN</sub>)

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

### 10-bit ADC, external reference (see Note 1)

| PARAMETER                                                                                                                              | TEST CONDITIONS                                                                                           | V <sub>CC</sub> | MIN | TYP | MAX             | UNIT |
|----------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-----------------|------|
| V <sub>eREF+</sub> Positive external reference input voltage range (see Note 2)                                                        | V <sub>eREF+</sub> > V <sub>eREF-</sub> ,<br>SREF1 = 1, SREF0 = 0                                         |                 | 1.4 |     | V <sub>CC</sub> | V    |
|                                                                                                                                        | V <sub>eREF-</sub> ≤ V <sub>eREF+</sub> ≤ (V <sub>CC</sub> - 0.15 V)<br>SREF1 = 1, SREF0 = 1 (see Note 3) |                 | 1.4 |     | 3.0             |      |
| V <sub>eREF-</sub> Negative external reference input voltage range (see Note 4)                                                        | V <sub>eREF+</sub> > V <sub>eREF-</sub>                                                                   |                 | 0   |     | 1.2             | V    |
| ΔV <sub>eREF</sub> Differential external reference input voltage range<br>ΔV <sub>eREF</sub> = V <sub>eREF+</sub> - V <sub>eREF-</sub> | V <sub>eREF+</sub> > V <sub>eREF-</sub> (see Note 5)                                                      |                 | 1.4 |     | V <sub>CC</sub> | V    |
| I <sub>VeREF+</sub> Static input current into V <sub>eREF+</sub>                                                                       | 0V ≤ V <sub>eREF+</sub> ≤ V <sub>CC</sub> ,<br>SREF1 = 1, SREF0 = 0                                       | 2.2 V/3 V       |     |     | ±1              | μA   |
|                                                                                                                                        | 0V ≤ V <sub>eREF+</sub> ≤ (V <sub>CC</sub> - 0.15 V) ≤ 3 V,<br>SREF1 = 1, SREF0 = 1 (see Note 3)          | 2.2 V/3 V       |     |     | 0               |      |
| I <sub>VeREF-</sub> Static input current into V <sub>eREF-</sub>                                                                       | 0V ≤ V <sub>eREF-</sub> ≤ V <sub>CC</sub>                                                                 | 2.2 V/3 V       |     |     | ±1              | μA   |

- NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C<sub>I</sub>, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I<sub>REFB</sub>. The current consumption can be limited to the sample and conversion period with REBURST = 1.
4. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
5. The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**10-bit ADC, timing parameters**

| PARAMETER             |                                     | TEST CONDITIONS                                                                            | V <sub>CC</sub> | MIN  | TYP                                         | MAX  | UNIT |
|-----------------------|-------------------------------------|--------------------------------------------------------------------------------------------|-----------------|------|---------------------------------------------|------|------|
| f <sub>ADC10CLK</sub> | ADC10 input clock frequency         | For specified performance of ADC10 linearity parameters                                    |                 |      |                                             |      |      |
|                       |                                     | ADC10SR = 0                                                                                | 2.2 V/3 V       | 0.45 |                                             | 6.3  | MHz  |
|                       |                                     | ADC10SR = 1                                                                                | 2.2 V/3 V       | 0.45 |                                             | 1.5  |      |
| f <sub>ADC10OSC</sub> | ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0<br>f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub>             | 2.2 V/3 V       | 3.7  |                                             | 6.3  | MHz  |
| t <sub>CONVERT</sub>  | Conversion time                     | ADC10 built-in oscillator, ADC10SSELx = 0<br>f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub> | 2.2 V/3 V       | 2.06 |                                             | 3.51 | μs   |
|                       |                                     | f <sub>ADC10CLK</sub> from ACLK, MCLK or SMCLK: ADC10SSELx ≠ 0                             |                 |      | 13x<br>ADC10DIVx<br>1/f <sub>ADC10CLK</sub> |      | μs   |
| t <sub>ADC10ON</sub>  | Turn on settling time of the ADC    | See Note 1                                                                                 |                 |      |                                             | 100  | ns   |

NOTE 1: The condition is that the error in a conversion started after t<sub>ADC10ON</sub> is less than ±0.5 LSB. The reference and input signals are already settled.

**10-bit ADC, linearity parameters**

| PARAMETER      |                              | TEST CONDITIONS                                                                   | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|----------------|------------------------------|-----------------------------------------------------------------------------------|-----------------|-----|------|-----|------|
| E <sub>I</sub> | Integral linearity error     |                                                                                   | 2.2 V/3 V       |     |      | ±1  | LSB  |
| E <sub>D</sub> | Differential linearity error |                                                                                   | 2.2 V/3 V       |     |      | ±1  | LSB  |
| E <sub>O</sub> | Offset error                 | Source impedance R <sub>S</sub> < 100 Ω                                           | 2.2 V/3 V       |     |      | ±1  | LSB  |
| E <sub>G</sub> | Gain error                   | SREFx = 010, Unbuffered external reference, V <sub>eREF+</sub> = 1.5 V            | 2.2 V           |     | ±1.1 | ±2  | LSB  |
|                |                              | SREFx = 010, Unbuffered external reference, V <sub>eREF+</sub> = 2.5 V            | 3 V             |     | ±1.1 | ±2  | LSB  |
|                |                              | SREFx = 011, Buffered external reference (see Note 2), V <sub>eREF+</sub> = 1.5 V | 2.2 V           |     | ±1.1 | ±4  | LSB  |
|                |                              | SREFx = 011, Buffered external reference (see Note 2), V <sub>eREF+</sub> = 2.5 V | 3 V             |     | ±1.1 | ±3  | LSB  |
| E <sub>T</sub> | Total unadjusted error       | SREFx = 010, Unbuffered external reference, V <sub>eREF+</sub> = 1.5 V            | 2.2 V           |     | ±2   | ±5  | LSB  |
|                |                              | SREFx = 010, Unbuffered external reference, V <sub>eREF+</sub> = 2.5 V            | 3 V             |     | ±2   | ±5  | LSB  |
|                |                              | SREFx = 011, Buffered external reference (see Note 2), V <sub>eREF+</sub> = 1.5 V | 2.2 V           |     | ±2   | ±7  | LSB  |
|                |                              | SREFx = 011, Buffered external reference (see Note 2), V <sub>eREF+</sub> = 2.5 V | 3 V             |     | ±2   | ±6  | LSB  |

NOTE 1: The reference buffer's offset adds to the gain and total unadjusted error.

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

### 10-bit ADC, temperature sensor and built-in $V_{MID}$

| PARAMETER                                                                        | TEST CONDITIONS                                                    | $V_{CC}$  | MIN  | TYP  | MAX  | UNIT          |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------|-----------|------|------|------|---------------|
| $I_{SENSOR}$ Temperature sensor supply current (see Note )                       | REFON = 0, INCHx = 0Ah, ADC10ON = 1, $T_A = 25^\circ C$            | 2.2 V     |      | 40   | 120  | $\mu A$       |
|                                                                                  |                                                                    | 3 V       |      | 60   | 160  |               |
| $TC_{SENSOR}$                                                                    | ADC10ON = 1, INCHx = 0Ah (see Note 2)                              | 2.2 V/3 V |      | 3.55 |      | $mV/^\circ C$ |
| $V_{Offset, Sensor}$ Sensor offset voltage                                       | ADC10ON = 1, INCHx = 0Ah (see Note 2)                              |           | -100 |      | 100  | mV            |
| $V_{Sensor}$ Sensor output voltage (see Note 3)                                  | Temperature sensor voltage at $T_A = 85^\circ C$                   | 2.2 V/3 V | 1195 | 1295 | 1395 | mV            |
|                                                                                  | Temperature sensor voltage at $T_A = 25^\circ C$                   | 2.2 V/3 V | 985  | 1085 | 1185 |               |
|                                                                                  | Temperature sensor voltage at $T_A = 0^\circ C$                    | 2.2 V/3 V | 895  | 995  | 1095 |               |
| $t_{Sensor(sample)}$ Sample time required if channel 10 is selected (see Note 4) | ADC10ON = 1, INCHx = 0Ah, Error of conversion result $\leq 1$ LSB  | 2.2 V/3 V | 30   |      |      | $\mu s$       |
| $I_{VMID}$ Current into divider at channel 11 (see Note 5)                       | ADC10ON = 1, INCHx = 0Bh                                           | 2.2 V     |      |      | NA   | $\mu A$       |
|                                                                                  |                                                                    | 3 V       |      |      | NA   |               |
| $V_{MID}$ $V_{CC}$ divider at channel 11                                         | ADC10ON = 1, INCHx = 0Bh, $V_{MID}$ is $\approx 0.5 \times V_{CC}$ | 2.2 V     | 1.06 | 1.1  | 1.14 | V             |
|                                                                                  |                                                                    | 3 V       | 1.46 | 1.5  | 1.54 |               |
| $t_{VMID(sample)}$ Sample time required if channel 11 is selected (see Note 6)   | ADC10ON = 1, INCHx = 0Bh, Error of conversion result $\leq 1$ LSB  | 2.2 V     | 1400 |      |      | ns            |
|                                                                                  |                                                                    | 3 V       | 1220 |      |      |               |

- NOTES: 1. The sensor current  $I_{SENSOR}$  is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1,  $I_{SENSOR}$  is included in  $I_{REF+}$ . When REFON = 0,  $I_{SENSOR}$  applies during conversion of the temperature sensor input (INCH = 0Ah).
2. The following formula can be used to calculate the temperature sensor output voltage:  
 $V_{Sensor, typ} = TC_{Sensor} (273 + T [^\circ C]) + V_{Offset, sensor} [mV]$  or  
 $V_{Sensor, typ} = TC_{Sensor} T [^\circ C] + V_{Sensor}(T_A = 0^\circ C) [mV]$
3. Results based on characterization and/or production test, not  $TC_{Sensor}$  or  $V_{Offset, sensor}$ .
4. The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor-on time  $t_{SENSOR(on)}$ .
5. No additional current is needed. The  $V_{MID}$  is used during sampling.
6. The on-time  $t_{VMID(on)}$  is included in the sampling time  $t_{VMID(sample)}$ ; no additional on time is needed.

### Timer0\_A3, Timer1\_A5

| PARAMETER                             | TEST CONDITIONS                                                                  | $V_{CC}$  | MIN | MAX | UNIT |
|---------------------------------------|----------------------------------------------------------------------------------|-----------|-----|-----|------|
| $f_{TA}$ Timer_A clock frequency      | Internal: SMCLK, ACLK,<br>External: TACLK, INCLK,<br>Duty cycle = 50% $\pm 10\%$ | 2.2 V     |     | 8   | MHz  |
|                                       |                                                                                  | 3 V       |     | 10  |      |
| $t_{TA, cap}$ Timer_A, capture timing | TA0, TA1, TA2                                                                    | 2.2 V/3 V | 20  |     | ns   |



**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**USCI (UART mode)**

| PARAMETER                                                                                      | TEST CONDITIONS                                                   | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                                                   | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% |                 |     | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>max,BITCLK</sub> Maximum BITCLK clock frequency (equals baudrate in MBaud) (see Note 1) |                                                                   | 2.2V /3 V       | 2   |                     |     | MHz  |
| t <sub>r</sub> UART receive deglitch time (see Note 2)                                         |                                                                   | 2.2 V           | 50  | 150                 |     | ns   |
|                                                                                                |                                                                   | 3 V             | 50  | 100                 |     |      |

NOTES: 1. The DCO wake-up time must be considered in LPM3/4 for baudrates above 1 MHz.  
2. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

**USCI (SPI master mode) (see Figure 19 and Figure 20)**

| PARAMETER                                         | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN                 | MAX | UNIT |
|---------------------------------------------------|----------------------------------------------------|-----------------|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency      | SMCLK, ACLK<br>Duty cycle = 50% ± 10%              |                 | f <sub>SYSTEM</sub> |     | MHz  |
| t <sub>SU,MI</sub> SOMI input data setup time     |                                                    | 2.2 V           | 110                 |     | ns   |
|                                                   |                                                    | 3 V             | 75                  |     |      |
| t <sub>HD,MI</sub> SOMI input data hold time      |                                                    | 2.2 V           | 0                   |     | ns   |
|                                                   |                                                    | 3 V             | 0                   |     |      |
| t <sub>VALID,MO</sub> SIMO output data valid time | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF | 2.2 V           |                     | 30  | ns   |
|                                                   |                                                    | 3 V             |                     | 20  |      |

NOTE:  $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$ .

For the slave's parameters t<sub>SU,SI</sub>(Slave) and t<sub>VALID,SO</sub>(Slave) refer to the SPI parameters of the attached slave.

**USCI (SPI slave mode) (see Figure 21 and Figure 22)**

| PARAMETER                                                                | TEST CONDITIONS                                    | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------------------------------------------------------------|----------------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>STE,LEAD</sub> STE lead time<br>STE low to clock                  |                                                    | 2.2 V/3 V       | 50  |     |     | ns   |
| t <sub>STE,LAG</sub> STE lag time<br>Last clock to STE high              |                                                    | 2.2 V/3 V       | 10  |     |     | ns   |
| t <sub>STE,ACC</sub> STE access time<br>STE low to SOMI data out         |                                                    | 2.2 V/3 V       | 50  |     |     | ns   |
| t <sub>STE,DIS</sub> STE disable time<br>STE high to SOMI high impedance |                                                    | 2.2 V/3 V       | 50  |     |     | ns   |
| t <sub>SU,SI</sub> SIMO input data setup time                            |                                                    | 2.2 V           | 20  |     |     | ns   |
|                                                                          |                                                    | 3 V             | 15  |     |     |      |
| t <sub>HD,SI</sub> SIMO input data hold time                             |                                                    | 2.2 V           | 10  |     |     | ns   |
|                                                                          |                                                    | 3 V             | 10  |     |     |      |
| t <sub>VALID,SO</sub> SOMI output data valid time                        | UCLK edge to SOMI valid,<br>C <sub>L</sub> = 20 pF | 2.2 V           | 75  | 110 |     | ns   |
|                                                                          |                                                    | 3 V             | 50  | 75  |     |      |

NOTE:  $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO}(Master) + t_{SU,SI}(USCI), t_{SU,MI}(Master) + t_{VALID,SO}(USCI))$ .

For the master's parameters t<sub>SU,MI</sub>(Master) and t<sub>VALID,MO</sub>(Master) refer to the SPI parameters of the attached master.

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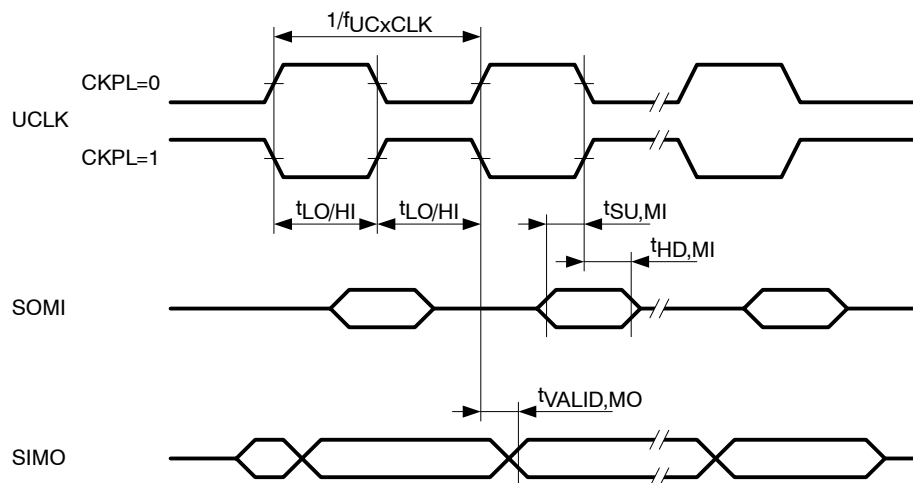


Figure 19. SPI Master Mode, CKPH = 0

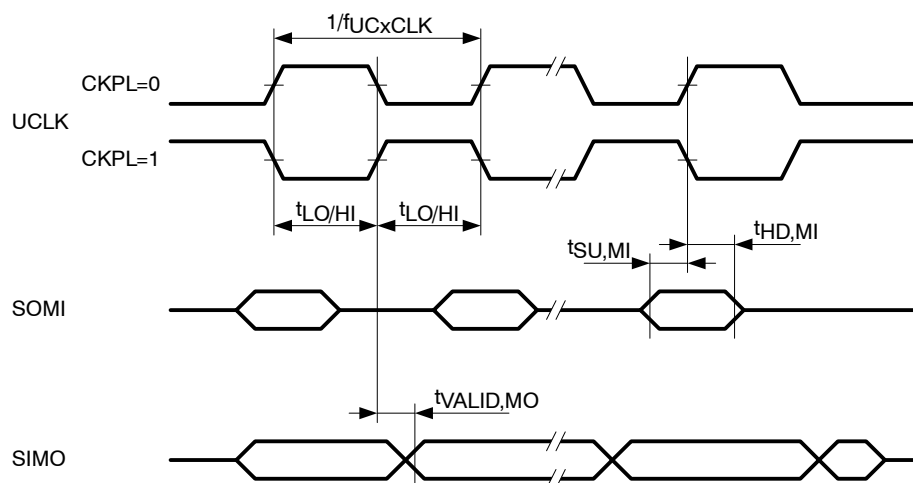
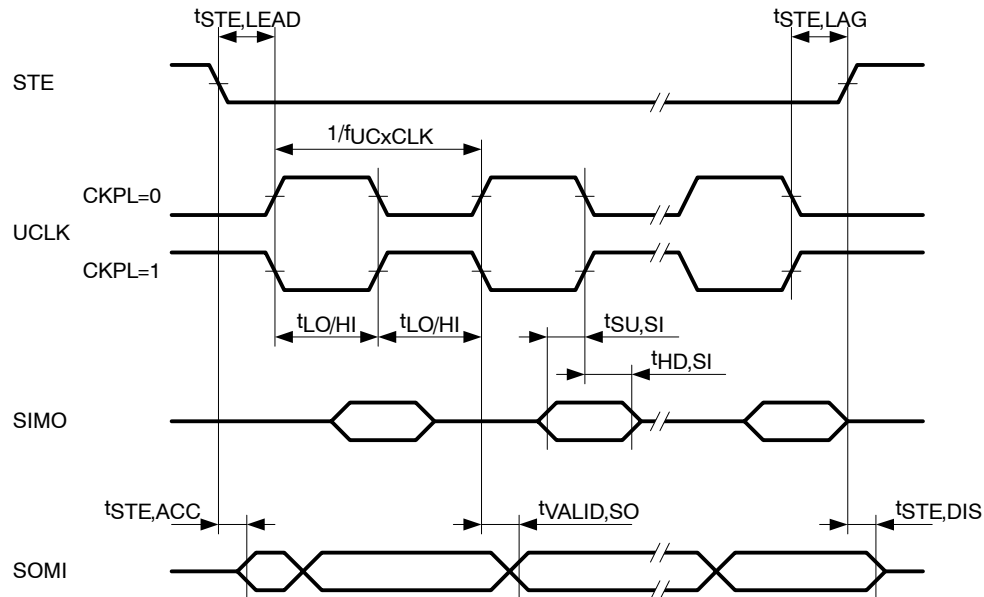
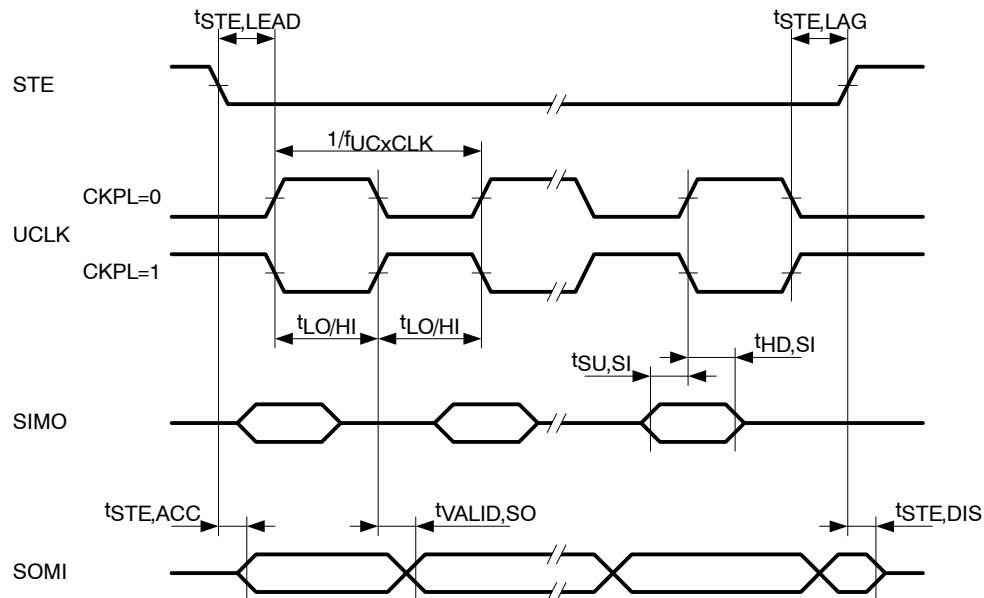


Figure 20. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)



**Figure 21. SPI Slave Mode, CKPH = 0**



**Figure 22. SPI Slave Mode, CKPH = 1**

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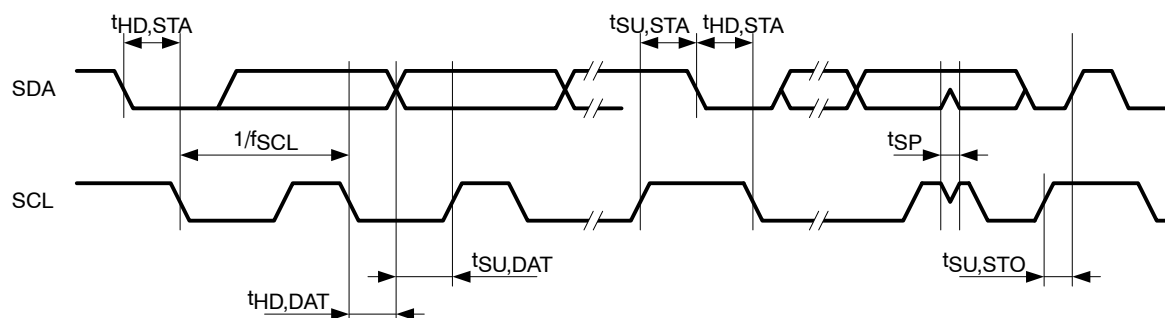
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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

### USCI (I2C mode) (see Figure 23)

| PARAMETER                                                        | TEST CONDITIONS                                                   | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|------------------------------------------------------------------|-------------------------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                     | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% |                 |     | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>SCL</sub> SCL clock frequency                             |                                                                   | 2.2 V/3 V       | 0   |                     | 400 | kHz  |
| t <sub>HD,STA</sub> Hold time (repeated) START                   | f <sub>SCL</sub> ≤ 100kHz                                         | 2.2 V/3 V       | 4.0 |                     |     | us   |
|                                                                  | f <sub>SCL</sub> > 100kHz                                         | 2.2 V/3 V       | 0.6 |                     |     | us   |
| t <sub>SU,STA</sub> Setup time for a repeated START              | f <sub>SCL</sub> ≤ 100kHz                                         | 2.2 V/3 V       | 4.7 |                     |     | us   |
|                                                                  | f <sub>SCL</sub> > 100kHz                                         | 2.2 V/3 V       | 0.6 |                     |     | us   |
| t <sub>HD,DAT</sub> Data hold time                               |                                                                   | 2.2 V/3 V       | 0   |                     |     | ns   |
| t <sub>SU,DAT</sub> Data set-up time                             |                                                                   | 2.2 V/3 V       | 250 |                     |     | ns   |
| t <sub>SU,STO</sub> Setup time for STOP                          |                                                                   | 2.2 V/3 V       | 4.0 |                     |     | us   |
| t <sub>SP</sub> Pulse width of spikes suppressed by input filter |                                                                   | 2.2 V           | 50  | 150                 | 600 | ns   |
|                                                                  |                                                                   | 3 V             | 50  | 100                 | 600 | ns   |



**Figure 23. I2C Mode Timing**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

**flash memory**

| PARAMETER                  |                                                     | TEST CONDITIONS       | V <sub>CC</sub> | MIN             | NOM             | MAX | UNIT             |
|----------------------------|-----------------------------------------------------|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V <sub>CC(PGM/ERASE)</sub> | Program and Erase supply voltage                    |                       |                 | 2.2             |                 | 3.6 | V                |
| f <sub>FTG</sub>           | Flash Timing Generator frequency                    |                       |                 | 257             |                 | 476 | kHz              |
| I <sub>PGM</sub>           | Supply current from DV <sub>CC</sub> during program |                       | 2.5V/3.6V       |                 | 3               | 5   | mA               |
| I <sub>ERASE</sub>         | Supply current from DV <sub>CC</sub> during erase   |                       | 2.5V/3.6V       |                 | 3               | 7   | mA               |
| t <sub>CPT</sub>           | Cumulative program time                             | see Note 1            | 2.5V/3.6V       |                 |                 | 10  | ms               |
| t <sub>CMErase</sub>       | Cumulative mass erase time                          | see Note 2            | 2.5V/3.6V       | 200             |                 |     | ms               |
|                            | Program/Erase endurance                             |                       |                 | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles           |
| t <sub>Retention</sub>     | Data retention duration                             | T <sub>J</sub> = 25°C |                 | 100             |                 |     | years            |
| t <sub>Word</sub>          | Word or byte program time                           | see Note 3            |                 |                 | 35              |     | t <sub>FTG</sub> |
| t <sub>Block, 0</sub>      | Block program time for 1 <sup>st</sup> byte or word |                       |                 |                 | 30              |     |                  |
| t <sub>Block, 1-63</sub>   | Block program time for each additional byte or word |                       |                 |                 | 21              |     |                  |
| t <sub>Block, End</sub>    | Block program end-sequence wait time                |                       |                 |                 | 6               |     |                  |
| t <sub>Mass Erase</sub>    | Mass erase time                                     |                       |                 |                 | 5297            |     |                  |
| t <sub>Seg Erase</sub>     | Segment erase time                                  |                       |                 |                 | 4819            |     |                  |

- NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297x1 / f<sub>FTG</sub>, max = 5297 x 1 / 476 kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles is required.)
3. These values are hardwired into the Flash Controller's state machine (t<sub>FTG</sub> = 1 / f<sub>FTG</sub>).

**JTAG and Spy-Bi-Wire interface**

| PARAMETER             |                                                                                   | TEST CONDITIONS | V <sub>CC</sub> | MIN   | TYP | MAX | UNIT |
|-----------------------|-----------------------------------------------------------------------------------|-----------------|-----------------|-------|-----|-----|------|
| f <sub>SBW</sub>      | Spy-Bi-Wire input frequency                                                       |                 | 2.2 V/3 V       | 0     |     | 8   | MHz  |
| t <sub>SBW,Low</sub>  | Spy-Bi-Wire low clock pulse length                                                |                 | 2.2 V/3 V       | 0.025 |     | 15  | us   |
| t <sub>SBW,En</sub>   | Spy-Bi-Wire enable time, TEST high to acceptance of first clock edge (see Note 1) |                 | 2.2 V/3 V       |       |     | 1   | us   |
| t <sub>SBW,Ret</sub>  | Spy-Bi-Wire return to normal operation time                                       |                 | 2.2 V/3 V       | 15    |     | 100 | us   |
| f <sub>TCK</sub>      | TCK input frequency (see Note 2)                                                  |                 | 2.2 V           | 0     |     | 5   | MHz  |
|                       |                                                                                   |                 | 3 V             | 0     |     | 10  | MHz  |
| R <sub>Internal</sub> | Internal pulldown resistance on TEST                                              |                 | 2.2 V/3 V       | 25    | 60  | 90  | kΩ   |

- NOTES: 1. Tools accessing the Spy-Bi-Wire interface need to wait for the maximum t<sub>SBW,En</sub> time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
2. f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

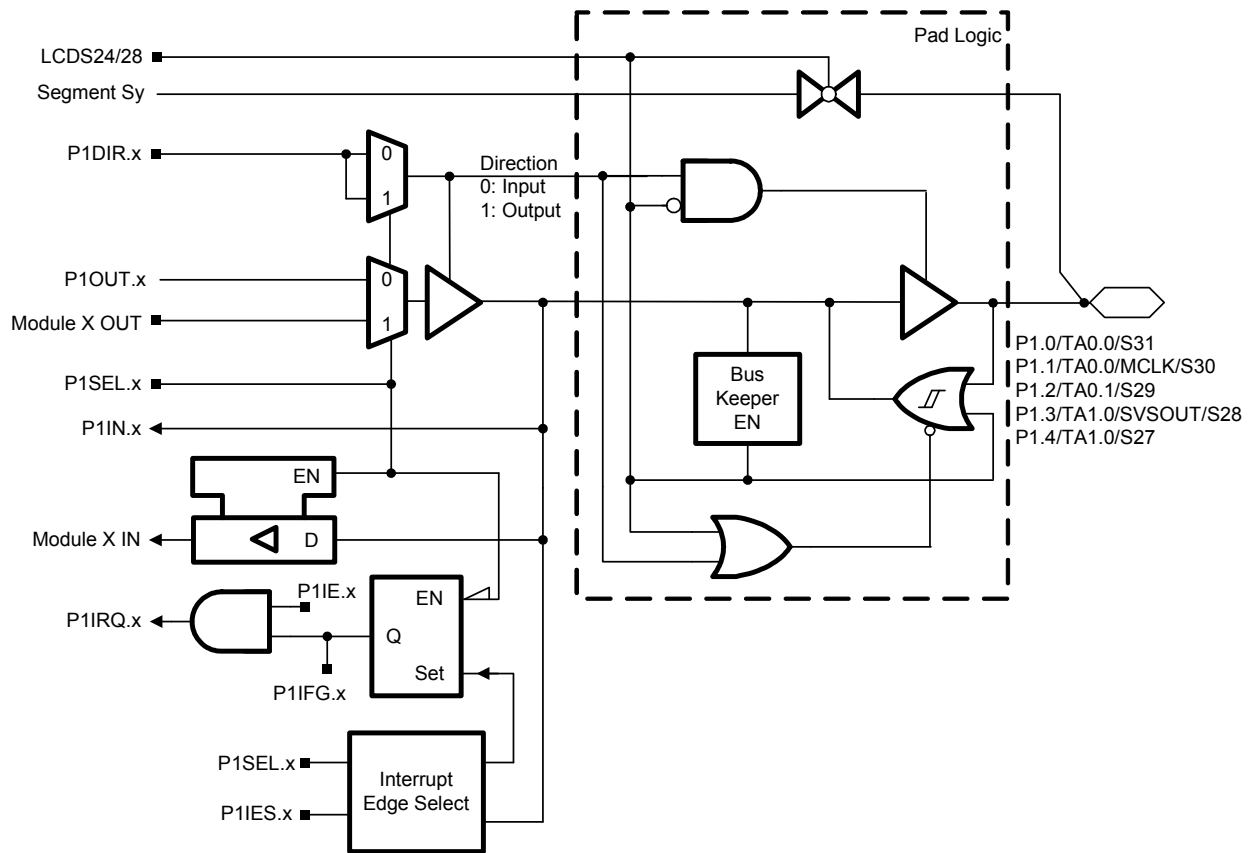
### JTAG fuse (see Note 1)

| PARAMETER           |                                               | TEST CONDITIONS       | V <sub>CC</sub> | MIN | MAX | UNIT |
|---------------------|-----------------------------------------------|-----------------------|-----------------|-----|-----|------|
| V <sub>CC(FB)</sub> | Supply voltage during fuse-blow condition     | T <sub>A</sub> = 25°C |                 | 2.5 |     | V    |
| V <sub>FB</sub>     | Voltage level on TDI/TCLK for fuse-blow       |                       |                 | 6   | 7   | V    |
| I <sub>FB</sub>     | Supply current into TDI/TCLK during fuse blow |                       |                 |     | 100 | mA   |
| t <sub>FB</sub>     | Time to blow fuse                             |                       |                 |     | 1   | ms   |

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

**APPLICATION INFORMATION**

**Port P1 pin schematic: P1.0 to P1.4, input/output with Schmitt trigger**



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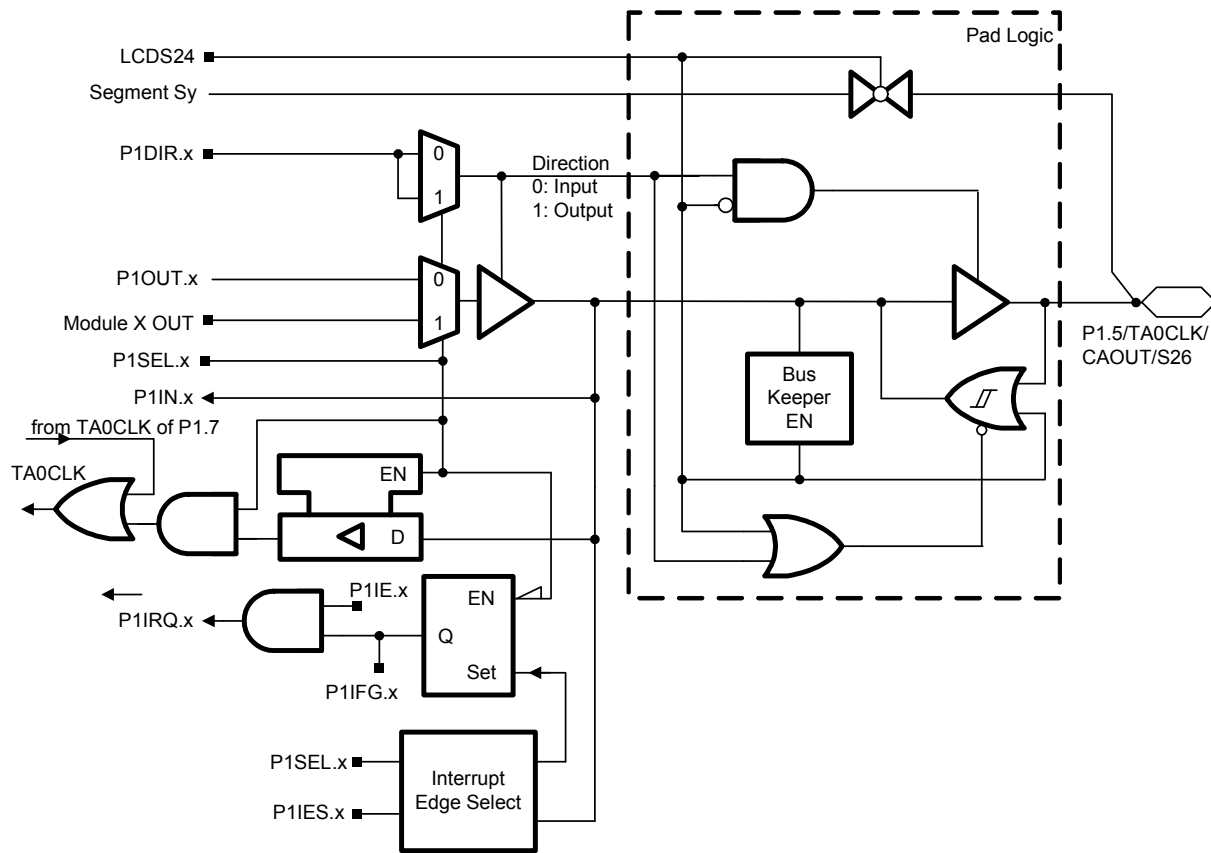
### Port P1 (P1.0 to P1.4) pin functions

| PIN NAME (P1.X)       | X | FUNCTION        | CONTROL BITS / SIGNALS |         |                  |
|-----------------------|---|-----------------|------------------------|---------|------------------|
|                       |   |                 | P1DIR.x                | P1SEL.x | LCDS24<br>LCDS28 |
| P1.0/TA0.0/S31        | 0 | P1.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer0_A3.CCI0A | 0                      | 1       | 0                |
|                       |   | Timer0_A3.TA0   | 1                      | 1       | 0                |
|                       |   | S31             | x                      | x       | 1 (LCDS28)       |
| P1.1/TA0.0/MCLK/S30   | 1 | P1.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer0_A3.CCI0B | 0                      | 1       | 0                |
|                       |   | MCLK            | 1                      | 1       | 0                |
|                       |   | S30             | x                      | x       | 1 (LCDS28)       |
| P1.2/TA0.1/S29        | 2 | P1.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer0_A3.CCI1A | 0                      | 1       | 0                |
|                       |   | Timer0_A3.TA1   | 1                      | 1       | 0                |
|                       |   | S29             | x                      | x       | 1 (LCDS28)       |
| P1.3/TA1.0/SVSOUT/S28 | 3 | P1.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer1_A5.CCI0B | 0                      | 1       | 0                |
|                       |   | SVSOUT          | 1                      | 1       | 0                |
|                       |   | S28             | x                      | x       | 1 (LCDS28)       |
| P1.4/TA1.0/S27        | 4 | P1.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer1_A5.CCI0A | 0                      | 1       | 0                |
|                       |   | Timer1_A5.TA0   | 1                      | 1       | 0                |
|                       |   | S27             | x                      | x       | 1 (LCDS24)       |

NOTES: 1. x: Don't care

## APPLICATION INFORMATION

### Port P1 pin schematic: P1.5, input/output with Schmitt trigger



### Port P1 (P1.5) pin functions

| PIN NAME (P1.X)       | X | FUNCTION        | CONTROL BITS / SIGNALS |         |                  |
|-----------------------|---|-----------------|------------------------|---------|------------------|
|                       |   |                 | P1DIR.x                | P1SEL.x | LCDS24<br>LCDS28 |
| P1.5/TA0CLK/CAOUT/S26 | 5 | P1.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer0_A3.TACLK | 0                      | 1       | 0                |
|                       |   | CAOUT           | 1                      | 1       | 0                |
|                       |   | S26             | x                      | x       | 1 (LCDS24)       |

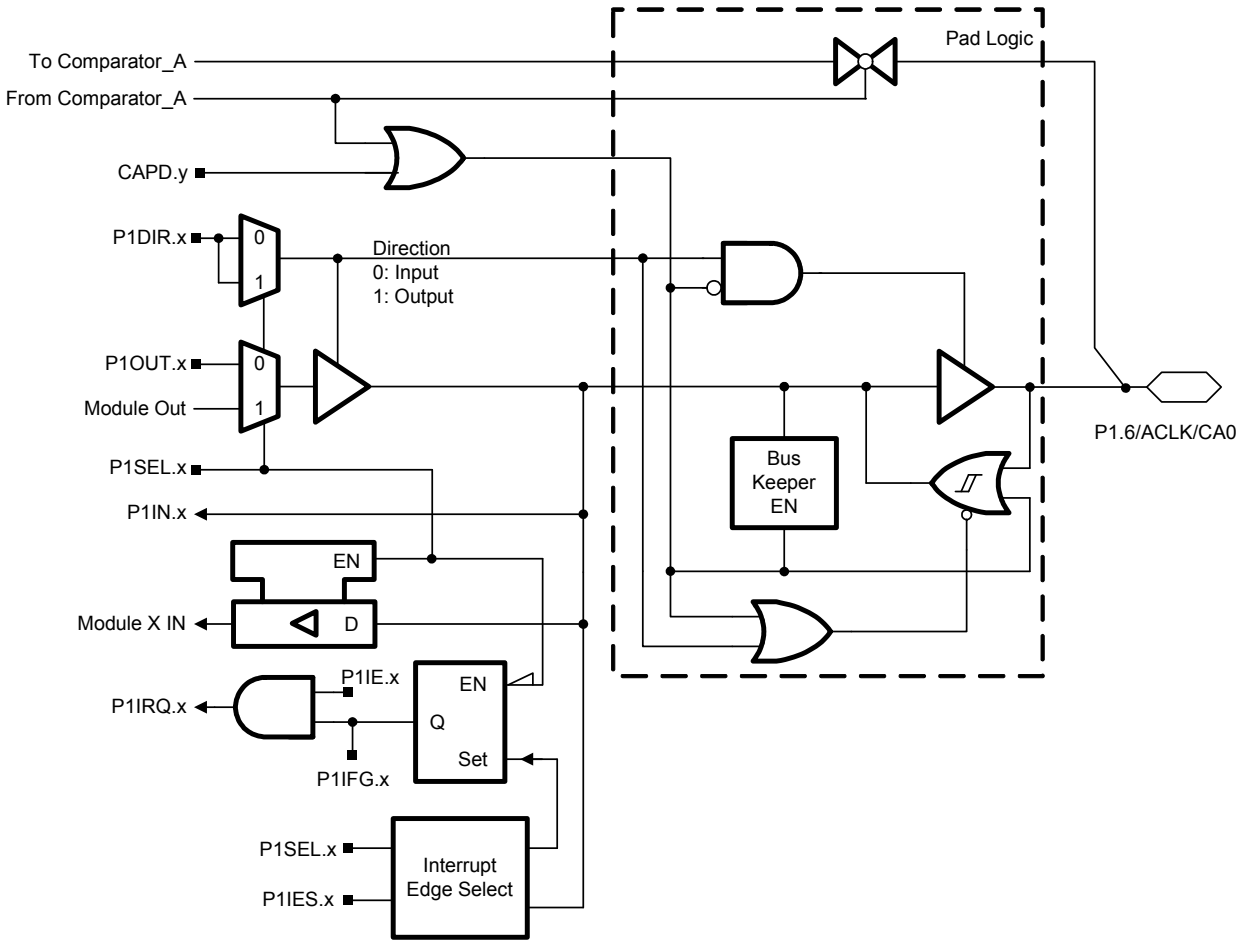
NOTES: 1. x: Don't care  
2. The input TA0CLK of P1.5 and P1.7 are logically ORed. Therefore only one of them should be enabled at a time to feed in TA0CLK.

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APPLICATION INFORMATION

Port P1 pin schematic: P1.6, input/output with Schmitt trigger



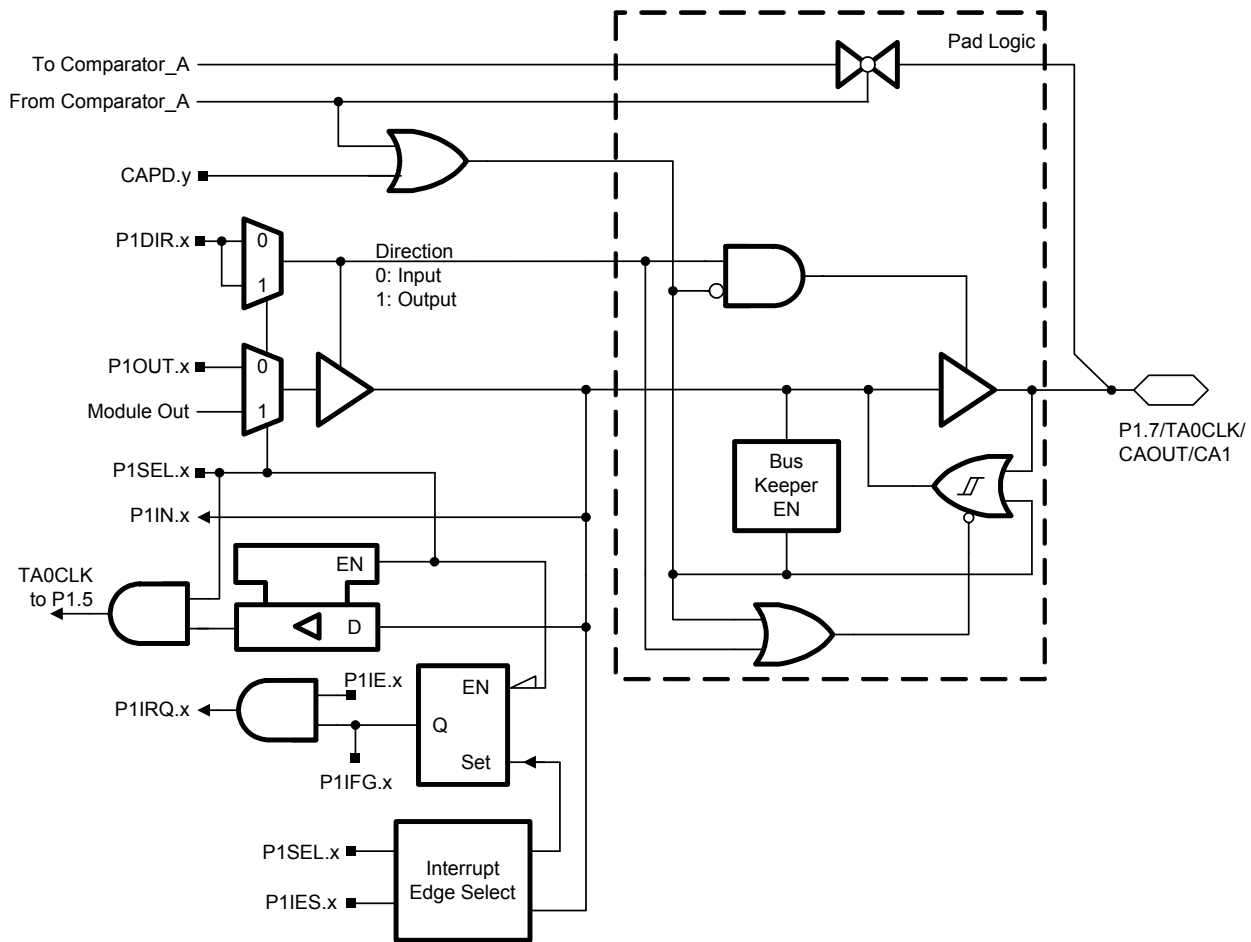
Port P1 (P1.6) pin functions

| PIN NAME (P1.X) | X | FUNCTION   | CONTROL BITS / SIGNALS |            |         |
|-----------------|---|------------|------------------------|------------|---------|
|                 |   |            | CAPD                   | P1DIR.x    | P1SEL.x |
| P1.6/ACLK/CA0   | 6 | P1.x (I/O) | 0                      | I: 0, O: 1 | 0       |
|                 |   | ACLK       | 0                      | 1          | 1       |
|                 |   | CA0        | 1 (CAPD.0)             | x          | x       |

NOTES: 1. x: Don't care

## APPLICATION INFORMATION

### Port P1 pin schematic: P1.7, input/output with Schmitt trigger



### Port P1 (P1.7) pin functions

| PIN NAME (P1.X)       | X | FUNCTION        | CONTROL BITS / SIGNALS |            |         |
|-----------------------|---|-----------------|------------------------|------------|---------|
|                       |   |                 | CAPD                   | P1DIR.x    | P1SEL.x |
| P1.7/TA0CLK/CAOUT/CA1 | 7 | P1.x (I/O)      | 0                      | I: 0, O: 1 | 0       |
|                       |   | Timer0_A3.TACLK | 0                      | 0          | 1       |
|                       |   | CAOUT           | 0                      | 1          | 1       |
|                       |   | CA1             | 1 (CAPD.1)             | x          | x       |

NOTES: 1. x: Don't care  
2. The input TA0CLK of P1.5 and P1.7 are combined by a logical OR. Therefore, only one of them should be enabled at a time to feed in TA0CLK.

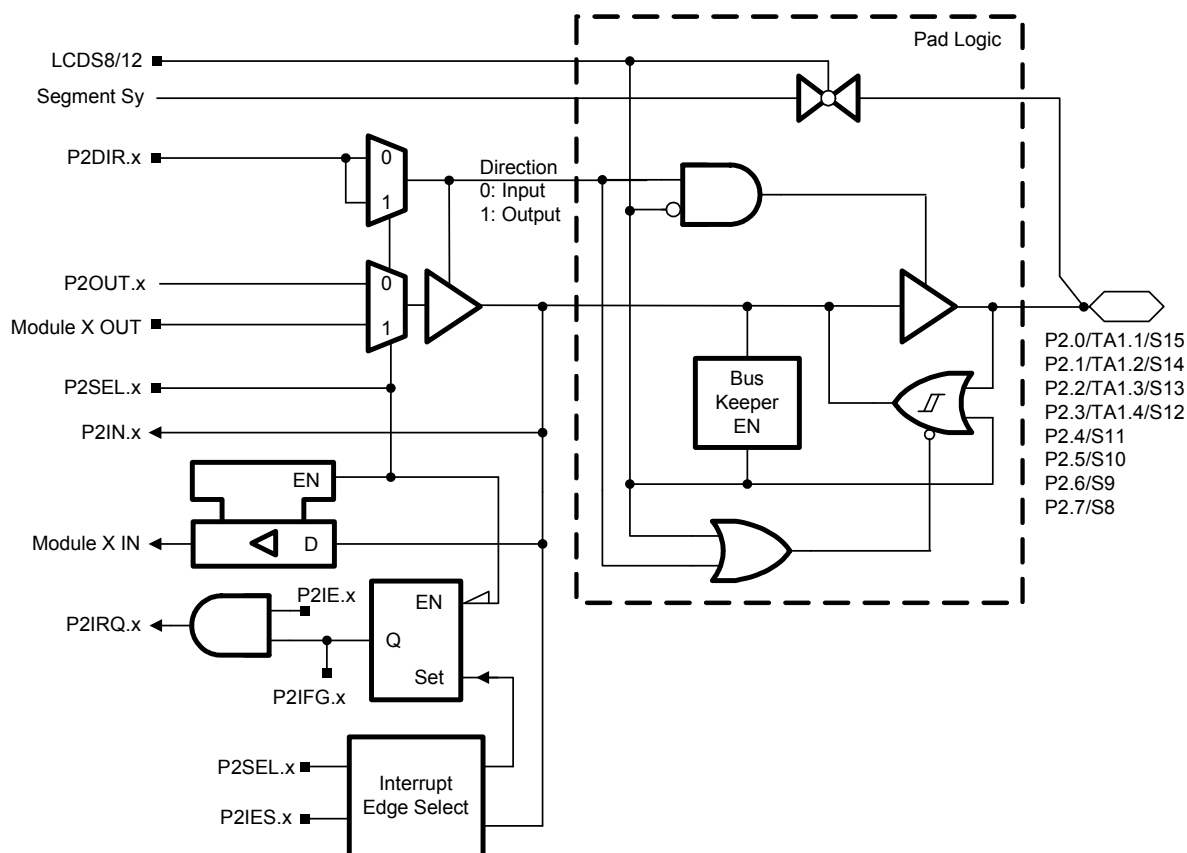
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## MIXED SIGNAL MICROCONTROLLER

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### APPLICATION INFORMATION

#### Port P2 pin schematic: P2.0 to P2.7 input/output with Schmitt trigger



**Port P2 (P2.0 to P2.7) pin functions**

| PIN NAME (P2.X) | X | FUNCTION      | CONTROL BITS / SIGNALS |         |                 |
|-----------------|---|---------------|------------------------|---------|-----------------|
|                 |   |               | P2DIR.x                | P2SEL.x | LCDS8<br>LCDS12 |
| P2.0/TA1.1/S15  | 0 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | Timer1_A5.TA1 | 1                      | 1       | 0               |
|                 |   | S15           | x                      | x       | 1 (LCDS12)      |
| P2.1/TA1.2/S14  | 1 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | Timer1_A5.TA2 | 1                      | 1       | 0               |
|                 |   | S14           | x                      | x       | 1 (LCDS12)      |
| P2.2/TA1.3/S13  | 2 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | Timer1_A5.TA3 | 1                      | 1       | 0               |
|                 |   | S13           | x                      | x       | 1 (LCDS12)      |
| P2.3/TA1.4/S12  | 3 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | Timer1_A5.TA4 | 1                      | 1       | 0               |
|                 |   | S12           | x                      | x       | 1 (LCDS12)      |
| P2.4/S11        | 4 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | S11           | x                      | x       | 1 (LCDS8)       |
| P2.5/S10        | 5 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | S10           | x                      | x       | 1 (LCDS8)       |
| P2.6/S9         | 6 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | S9            | x                      | x       | 1 (LCDS8)       |
| P2.7/S8         | 7 | P2.x (I/O)    | I: 0, O: 1             | 0       | 0               |
|                 |   | S8            | x                      | x       | 1 (LCDS8)       |

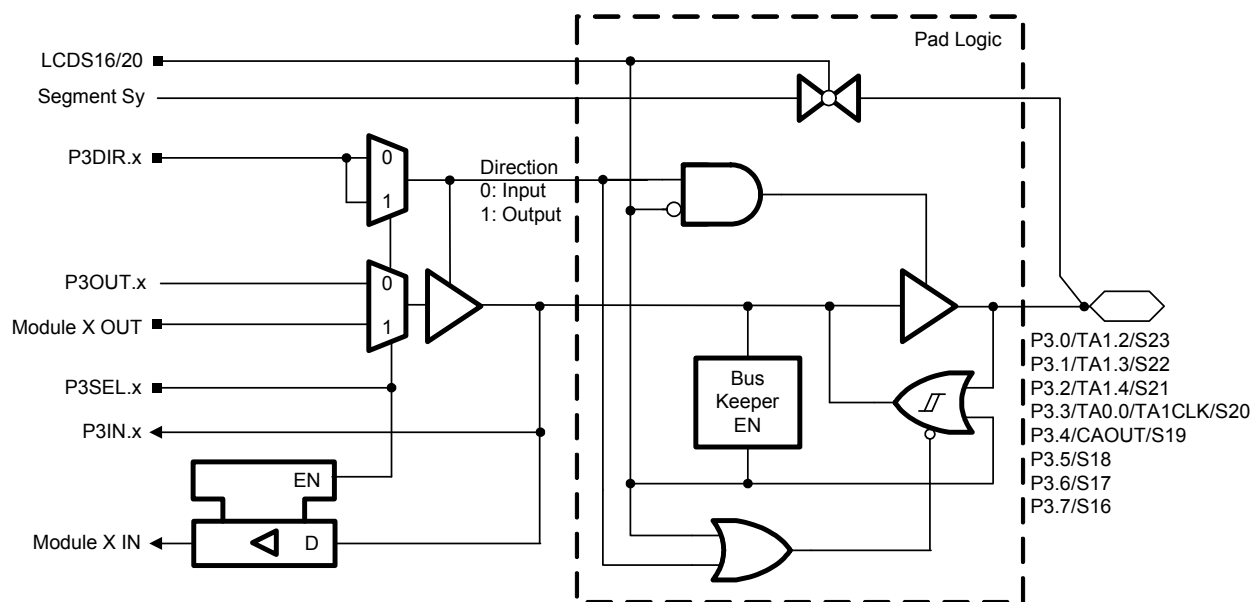
NOTES: 1. x: Don't care

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## APPLICATION INFORMATION

### Port P3 pin schematic: P3.0 to P3.7 input/output with Schmitt trigger



**Port P3 (P3.0 to P3.7) pin functions**

| PIN NAME (P3.X)       | X | FUNCTION        | CONTROL BITS / SIGNALS |         |                  |
|-----------------------|---|-----------------|------------------------|---------|------------------|
|                       |   |                 | P3DIR.x                | P3SEL.x | LCDS16<br>LCDS20 |
| P3.0/TA1.2/S23        | 0 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer1_A5.CCI2A | 0                      | 1       | 0                |
|                       |   | Timer1_A5.TA2   | 1                      | 1       | 0                |
|                       |   | S23             | x                      | x       | 1 (LCDS20)       |
| P3.1/TA1.3/S22        | 1 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer1_A5.CCI3A | 0                      | 1       | 0                |
|                       |   | Timer1_A5.TA3   | 1                      | 1       | 0                |
|                       |   | S22             | x                      | x       | 1 (LCDS20)       |
| P3.2/TA1.4/S21        | 2 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer1_A5.CCI4A | 0                      | 1       | 0                |
|                       |   | Timer1_A5.TA4   | 1                      | 1       | 0                |
|                       |   | S21             | x                      | x       | 1 (LCDS20)       |
| P3.3/TA0.0/TA1CLK/S20 | 3 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | Timer1_A5.TACLK | 0                      | 1       | 0                |
|                       |   | Timer0_A3.TA0   | 1                      | 1       | 0                |
|                       |   | S20             | x                      | x       | 1 (LCDS20)       |
| P3.4/CAOUT/S19        | 4 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | CAOUT           | 1                      | 1       | 0                |
|                       |   | S19             | x                      | x       | 1 (LCDS16)       |
| P3.5/S18              | 5 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | S18             | x                      | x       | 1 (LCDS16)       |
| P3.6/S17              | 6 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | S17             | x                      | x       | 1 (LCDS16)       |
| P3.7/S16              | 7 | P3.x (I/O)      | I: 0, O: 1             | 0       | 0                |
|                       |   | S16             | x                      | x       | 1 (LCDS16)       |

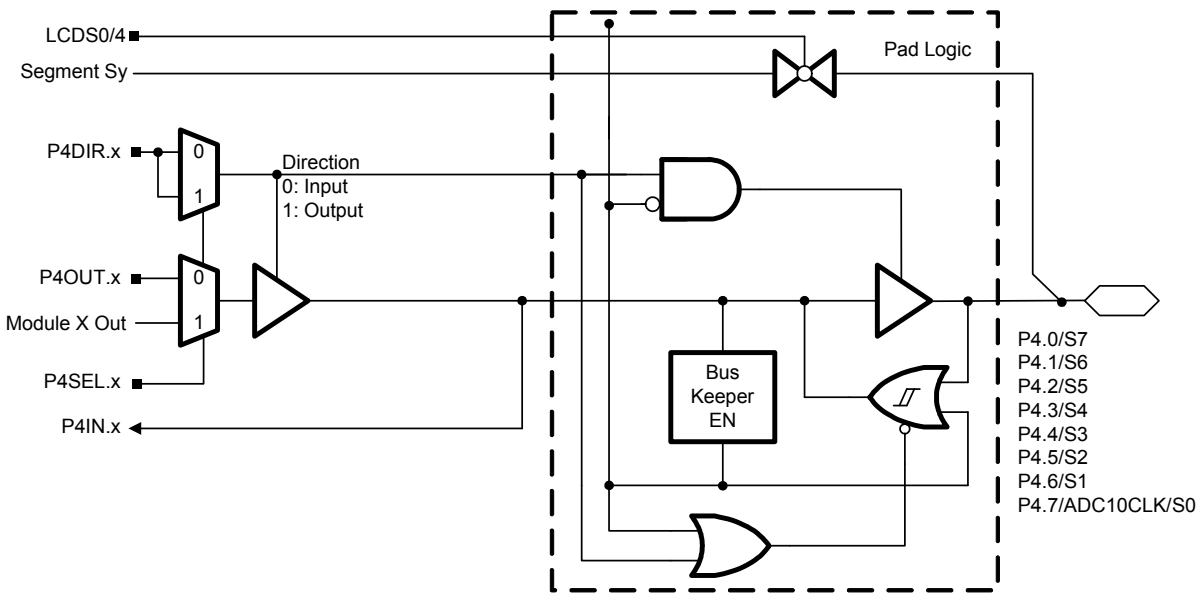
NOTES: 1. x: Don't care

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APPLICATION INFORMATION

Port P4 pin schematic: P4.0 to P4.7 input/output with Schmitt trigger



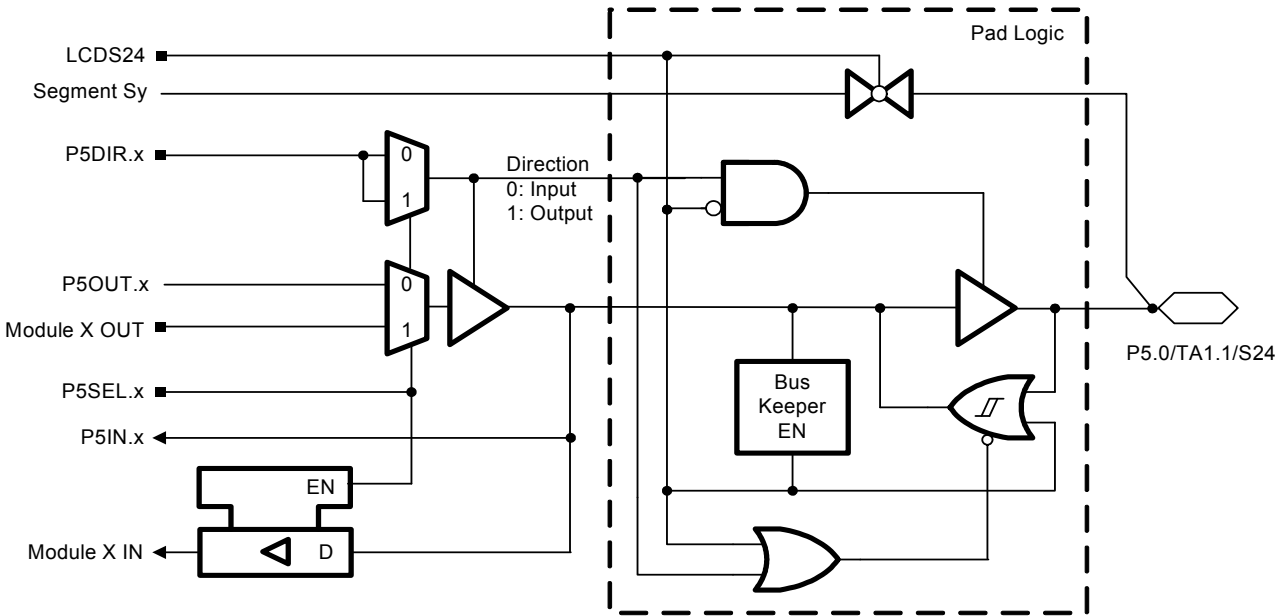
Port P4 (P4.0 to P4.7) pin functions

| PIN NAME (P4.X)  | X | FUNCTION   | CONTROL BITS / SIGNALS |         |                |
|------------------|---|------------|------------------------|---------|----------------|
|                  |   |            | P4DIR.x                | P4SEL.x | LCDS4<br>LCDS0 |
| P4.0/S7          | 0 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | S7         | x                      | x       | 1 (LCDS4)      |
| P4.1/S6          | 1 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | S6         | x                      | x       | 1 (LCDS4)      |
| P4.2/S5          | 2 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | S5         | x                      | x       | 1 (LCDS4)      |
| P4.3/S4          | 3 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | S4         | x                      | x       | 1 (LCDS4)      |
| P4.4/S3          | 4 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | S3         | x                      | x       | 1 (LCDS0)      |
| P4.5/S2          | 5 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | S2         | x                      | x       | 1 (LCDS0)      |
| P4.6/S1          | 6 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | S1         | x                      | x       | 1 (LCDS0)      |
| P4.7/ADC10CLK/S0 | 7 | P4.x (I/O) | I: 0, O: 1             | 0       | 0              |
|                  |   | ADC10CLK   | 1                      | 1       | 0              |
|                  |   | S0         | x                      | x       | 1 (LCDS0)      |

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P5 pin schematic: P5.0, input/output with Schmitt trigger



Port P5 (P5.0) pin functions

| PIN NAME (P5.X) | X | FUNCTION        | CONTROL BITS / SIGNALS |         |         |
|-----------------|---|-----------------|------------------------|---------|---------|
|                 |   |                 | P5DIR.x                | P5SEL.x | LCD S24 |
| P5.0/TA1.1/S24  | 0 | P5.x (I/O)      | I: 0, O: 1             | 0       | 0       |
|                 |   | Timer1_A5.CCI1A | 0                      | 1       | 0       |
|                 |   | Timer1_A5.TA1   | 1                      | 1       | 0       |
|                 |   | S24             | x                      | x       | 1       |

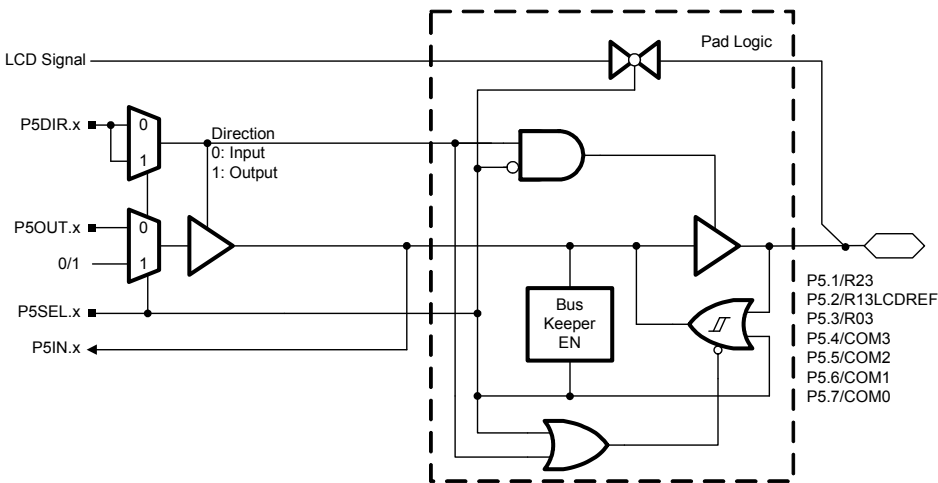
NOTES: 1. x: Don't care

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APPLICATION INFORMATION

Port P5 pin schematic: P5.1 to P5.7, input/output with Schmitt trigger



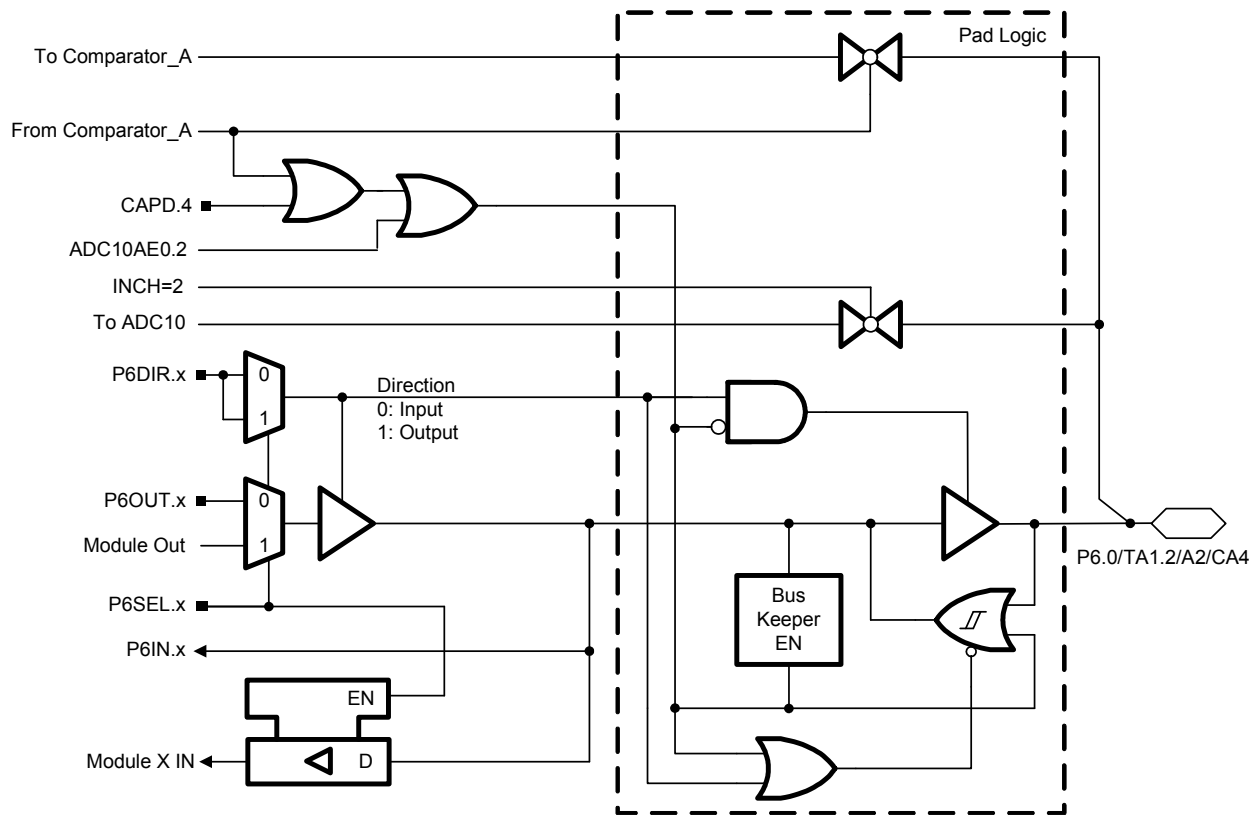
Port P5 (P5.1 to P5.7) pin functions

| PIN NAME (P5.X) | X | FUNCTION      | CONTROL BITS / SIGNALS |         |
|-----------------|---|---------------|------------------------|---------|
|                 |   |               | P5DIR.x                | P5SEL.x |
| P5.1/R23        | 1 | P5.x (I/O)    | I: 0, O: 1             | 0       |
|                 |   | R23           | x                      | 1       |
| P5.2/LCDREF/R13 | 2 | P5.x (I/O)    | I: 0, O: 1             | 0       |
|                 |   | R13 or LCDREF | x                      | 1       |
| P5.3/R03        | 3 | P5.x (I/O)    | I: 0, O: 1             | 0       |
|                 |   | R03           | x                      | 1       |
| P5.4/COM3       | 4 | P5.x (I/O)    | I: 0, O: 1             | 0       |
|                 |   | COM3          | x                      | 1       |
| P5.5/COM2       | 5 | P5.x (I/O)    | I: 0, O: 1             | 0       |
|                 |   | COM2          | x                      | 1       |
| P5.6/COM1       | 6 | P5.x (I/O)    | I: 0, O: 1             | 0       |
|                 |   | COM1          | x                      | 1       |
| P5.7/COM0       | 7 | P5.x (I/O)    | I: 0, O: 1             | 0       |
|                 |   | COM0          | x                      | 1       |

NOTES: 1. x: Don't care

## APPLICATION INFORMATION

### Port P6 pin schematic: P6.0, input/output with Schmitt trigger



### Port P6 (P6.0) pin functions

| PIN NAME (P6.X)   | X | FUNCTION      | CONTROL BITS / SIGNALS |            |            |         |
|-------------------|---|---------------|------------------------|------------|------------|---------|
|                   |   |               | CAPD                   | ADC10AE0.y | P6DIR.x    | P6SEL.x |
| P6.0/TA1.2/A2/CA4 | 0 | P6.x (I/O)    | 0                      | 0          | I: 0, O: 1 | 0       |
|                   |   | Timer1_A5.TA2 | 0                      | 0          | 1          | 1       |
|                   |   | A2            | x                      | 1 (y=2)    | x          | x       |
|                   |   | CA4           | 1 (CAPD.4)             | x          | x          | x       |

NOTES: 1. x: Don't care

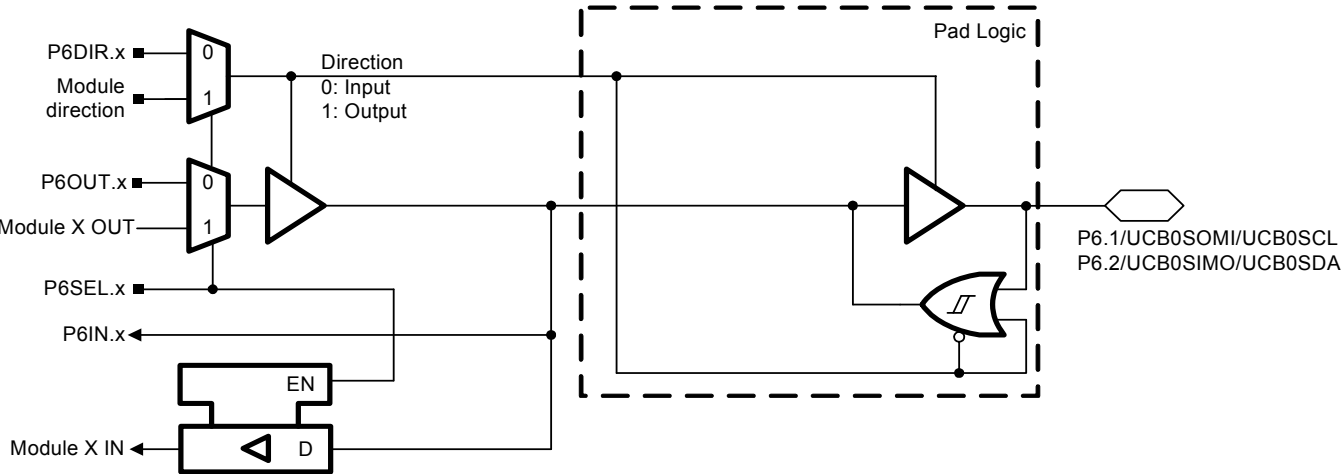
MSP430F41x2

MIXED SIGNAL MICROCONTROLLER

SLAS648E – APRIL 2009 – REVISED MARCH 2011

APPLICATION INFORMATION

Port P6 pin schematic: P6.1 and P6.2, input/output with Schmitt trigger



Port P6 (P6.1 and P6.2) pin functions

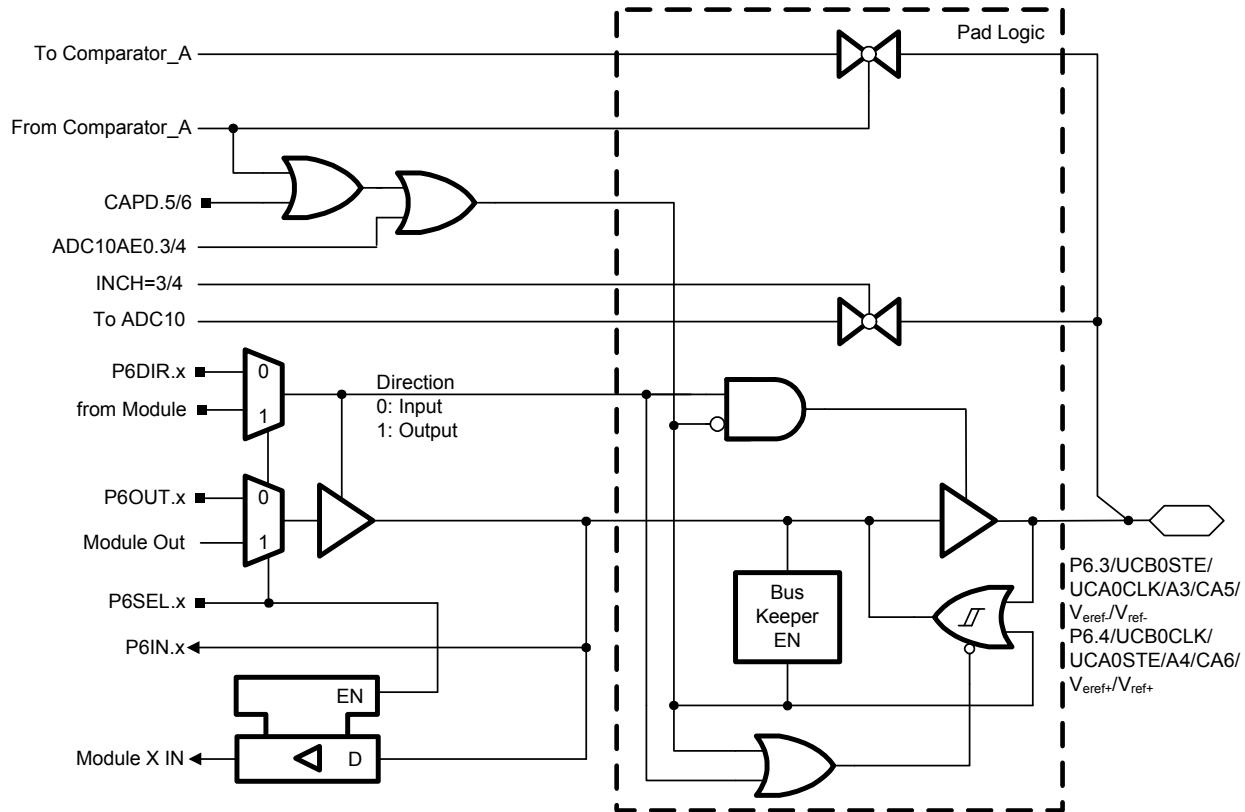
| PIN NAME (P6.X)       | X | FUNCTION                      | CONTROL BITS / SIGNALS |         |
|-----------------------|---|-------------------------------|------------------------|---------|
|                       |   |                               | P6DIR.x                | P6SEL.x |
| P6.1/UCB0SOMI/UCB0SCL | 1 | P6.x (I/O)                    | I: 0, O: 1             | 0       |
|                       |   | UCB0SOMI/UCB0SCL (see Note 2) | x                      | 1       |
| P6.2/UCB0SIMO/UCB0SDA | 2 | P6.x (I/O)                    | I: 0, O: 1             | 0       |
|                       |   | UCB0SIMO/UCB0SDA (see Note 2) | x                      | 1       |

NOTES: 1. x: Don't care

2. The pin direction is controlled by the USC1 module.

## APPLICATION INFORMATION

### Port P6 pin schematic: P6.3 and P6.4, input/output with Schmitt trigger



### Port P6 (P6.3 and P6.4) pin functions

| PIN NAME (P6.X)                                                          | X | FUNCTION                                | CONTROL BITS / SIGNALS |            |            |         |
|--------------------------------------------------------------------------|---|-----------------------------------------|------------------------|------------|------------|---------|
|                                                                          |   |                                         | CAPD                   | ADC10AE0.y | P6DIR.x    | P6SEL.x |
| P6.3/UCB0STE/<br>UCA0CLK/A3/CA5/<br>V <sub>ref-</sub> /V <sub>ref-</sub> | 3 | P6.x (I/O)                              | 0                      | 0          | I: 0, O: 1 | 0       |
|                                                                          |   | UCB0STE/UCA0CLK (see Note 2)            | 0                      | 0          | x          | 1       |
|                                                                          |   | A3/V <sub>ref-</sub> /V <sub>ref-</sub> | x                      | 1 (y=3)    | x          | x       |
|                                                                          |   | CA5                                     | 1 (CAPD.5)             | x          | x          | x       |
| P6.4/UCB0CLK/<br>UCA0STE/A4/CA6/<br>V <sub>ref+</sub> /V <sub>ref+</sub> | 4 | P6.x (I/O)                              | 0                      | 0          | I: 0, O: 1 | 0       |
|                                                                          |   | UCB0CLK/UCA0STE (see Note 2)            | 0                      | 0          | x          | 1       |
|                                                                          |   | A4/V <sub>ref+</sub> /V <sub>ref+</sub> | x                      | 1 (y=4)    | x          | x       |
|                                                                          |   | CA6                                     | 1 (CAPD.6)             | x          | x          | x       |

NOTES: 1. x: Don't care  
2. The pin direction is controlled by the USCI module.

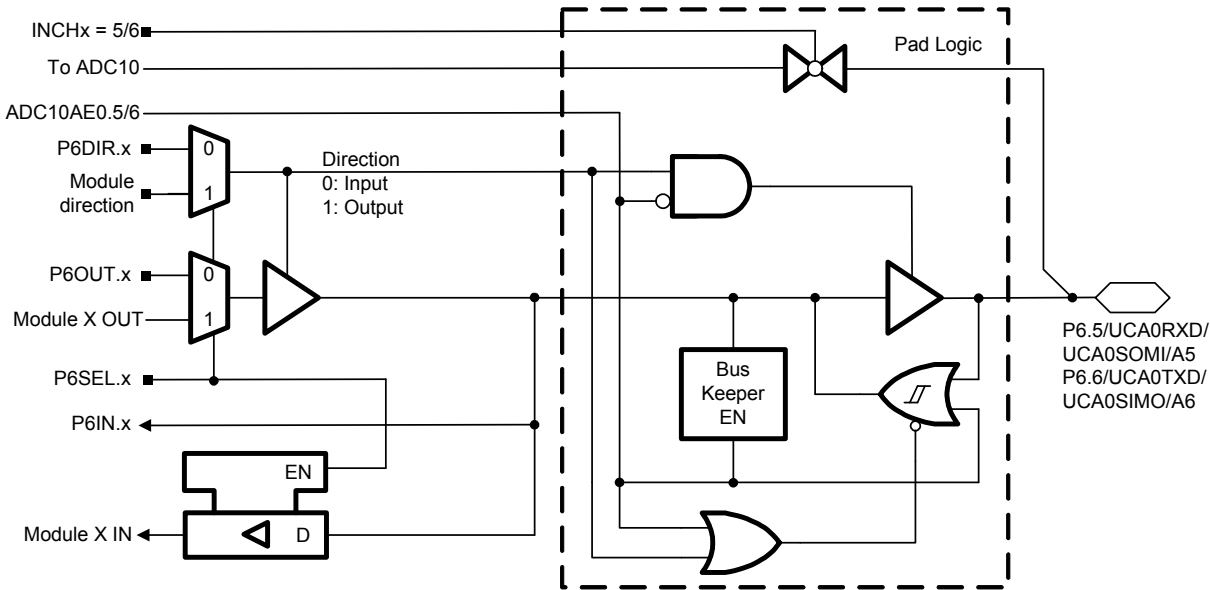
MSP430F41x2

MIXED SIGNAL MICROCONTROLLER

SLAS648E – APRIL 2009 – REVISED MARCH 2011

APPLICATION INFORMATION

Port P6 pin schematic: P6.5 and P6.6, input/output with Schmitt trigger



Port P6 (P6.5 and P6.6) pin functions

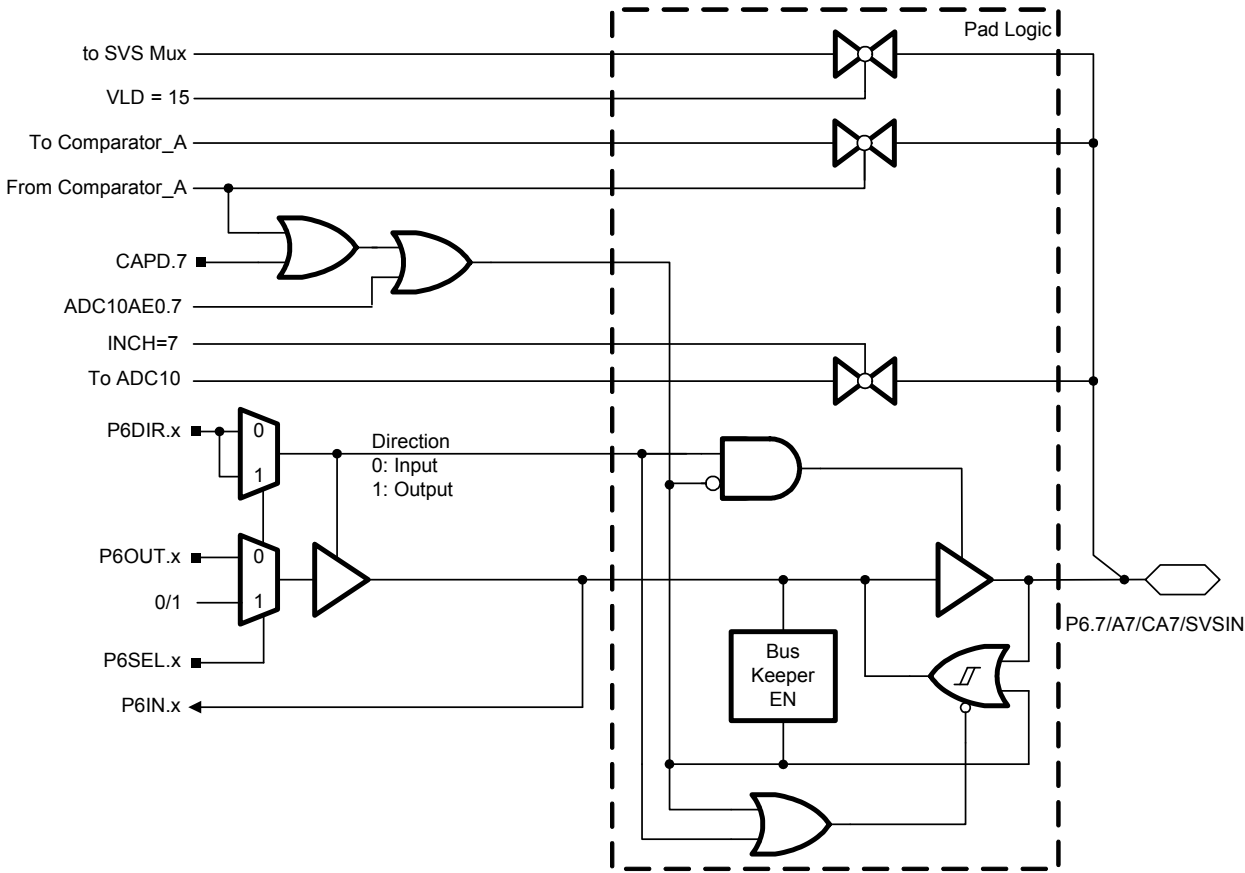
| PIN NAME (P6.X)              | X | FUNCTION                      | CONTROL BITS / SIGNALS |            |         |
|------------------------------|---|-------------------------------|------------------------|------------|---------|
|                              |   |                               | ADC10AE0.y             | P6DIR.x    | P6SEL.x |
| P6.5/UCA0RXD/<br>UCA0SOMI/A5 | 5 | P6.x (I/O)                    | 0                      | I: 0, O: 1 | 0       |
|                              |   | UCA0RXD/UCA0SOMI (see Note 2) | 0                      | x          | 1       |
|                              |   | A5                            | 1 (y=5)                | x          | x       |
| P6.6/UCA0TXD/<br>UCA0SIMO/A6 | 6 | P6.x (I/O)                    | 0                      | I: 0, O: 1 | 0       |
|                              |   | UCA0TXD/UCA0SIMO (see Note 2) | 0                      | x          | 1       |
|                              |   | A6                            | 1 (y=6)                | x          | x       |

NOTES: 1. x: Don't care

2. The pin direction is controlled by the USCI module.

APPLICATION INFORMATION

Port P6 pin schematic: P6.7, input/output with Schmitt trigger



Port P6 (P6.7) pin functions

| PIN NAME (P6.X)   | X | FUNCTION   | CONTROL BITS / SIGNALS |            |           |            |         |
|-------------------|---|------------|------------------------|------------|-----------|------------|---------|
|                   |   |            | VLDx = 15              | CAPD       | ADC10AE0  | P6DIR.x    | P6SEL.x |
| P6.7/A7/CA7/SVSIN | 7 | P7.x (I/O) | 0                      | 0          | 0         | I: 0, O: 1 | 0       |
|                   |   | A7         | 0                      | x          | 1 (y = 7) | x          | x       |
|                   |   | CA7        | 0                      | 1 (CAPD.7) | x         | x          | x       |
|                   |   | SVSIN      | 1                      | 0          | 0         | x          | x       |

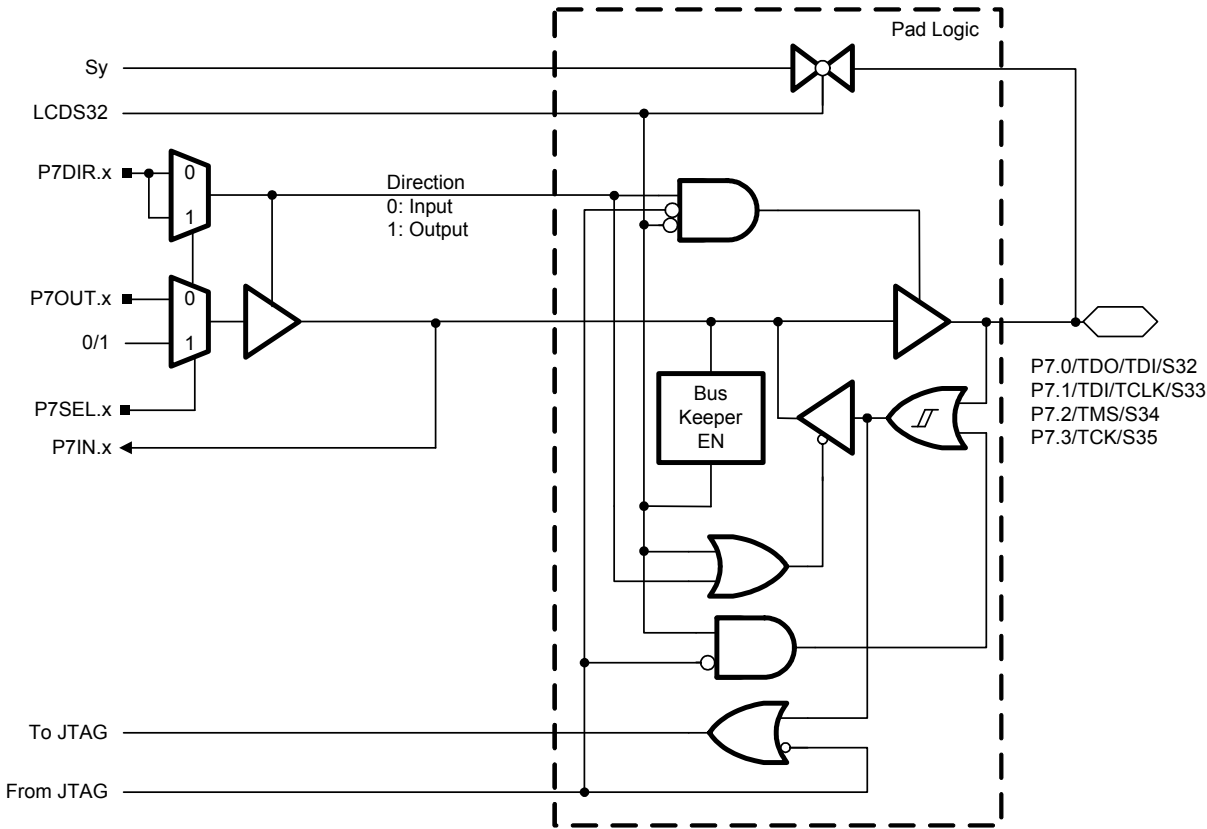
NOTES: 1. x: Don't care

MSP430F41x2  
MIXED SIGNAL MICROCONTROLLER

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/APPLICATION INFORMATION

Port P7 pin schematic: P7.0 to P7.3, input/output with Schmitt trigger



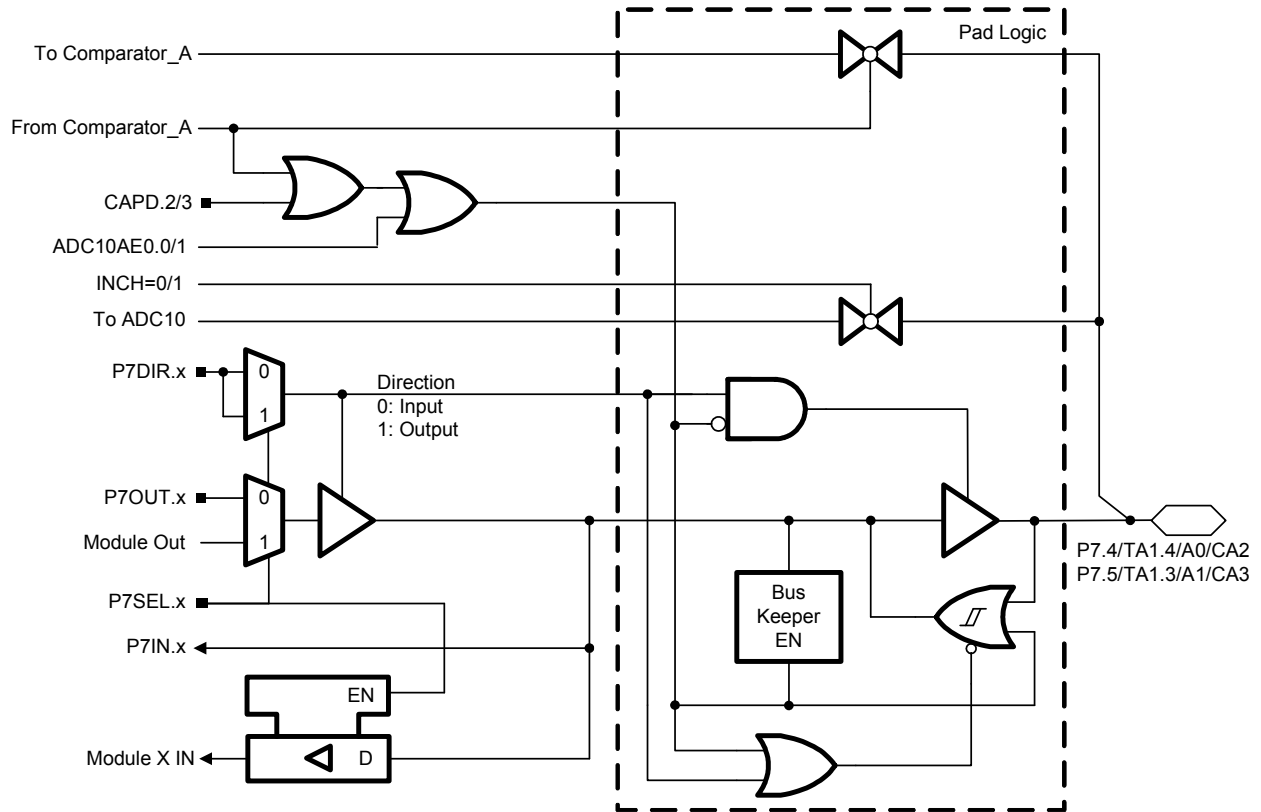
Port P7 (P7.0 to P7.3) pin functions

| PIN NAME (P7.X)   | X | FUNCTION              | CONTROL BITS / SIGNALS |            |         |        |
|-------------------|---|-----------------------|------------------------|------------|---------|--------|
|                   |   |                       | JTAG Mode              | P7DIR.x    | P7SEL.x | LCDS32 |
| P7.0/TDO/TDI/S32  | 0 | P7.x (I/O)            | 0                      | I: 0, O: 1 | 0       | 0      |
|                   |   | TDO/TDI (see Note 1)  | 1                      | x          | x       | x      |
|                   |   | S32                   | 0                      | x          | x       | 1      |
| P7.1/TDI/TCLK/S33 | 1 | P7.x (I/O)            | 0                      | I: 0, O: 1 | 0       | 0      |
|                   |   | TDI/TCLK (see Note 1) | 1                      | x          | x       | x      |
|                   |   | S33                   | 0                      | x          | x       | 1      |
| P7.2/TMS/S34      | 2 | P7.x (I/O)            | 0                      | I: 0, O: 1 | 0       | 0      |
|                   |   | TMS (see Note 1)      | 1                      | x          | x       | x      |
|                   |   | S34                   | 0                      | x          | x       | 1      |
| P7.3/TCK/S35      | 3 | P7.3 (I/O)            | 0                      | I: 0, O: 1 | 0       | 0      |
|                   |   | TCK (see Note 1)      | 1                      | x          | x       | x      |
|                   |   | S35                   | 0                      | x          | x       | 1      |

NOTES: 1. In JTAG Mode the internal pullup/pulldown resistors are disabled.  
2. X: Don't care.

## APPLICATION INFORMATION

### Port P7 pin schematic: P7.4 and P7.5, input/output with Schmitt trigger



### Port P7 (P7.4 and P7.5) pin functions

| PIN NAME (P7.X)   | X | FUNCTION        | CONTROL BITS / SIGNALS |            |            |         |
|-------------------|---|-----------------|------------------------|------------|------------|---------|
|                   |   |                 | CAPD                   | ADC10AE0.y | P7DIR.x    | P7SEL.x |
| P7.4/TA1.4/A0/CA2 | 4 | P7.x (I/O)      | 0                      | 0          | I: 0, O: 1 | 0       |
|                   |   | Timer1_A5.TA4   | 0                      | 0          | 1          | 1       |
|                   |   | Timer1_A5.CCI4B | 0                      | 0          | 0          | 1       |
|                   |   | A0              | x                      | 1 (y=0)    | x          | x       |
|                   |   | CA2             | 1 (CAPD.2)             | x          | x          | x       |
| P7.5/TA1.3/A1/CA3 | 5 | P7.x (I/O)      | 0                      | 0          | I: 0, O: 1 | 0       |
|                   |   | Timer1_A5.TA3   | 0                      | 0          | 1          | 1       |
|                   |   | Timer1_A5.CCI3B | 0                      | 0          | 0          | 1       |
|                   |   | A1              | x                      | 1 (y=1)    | x          | x       |
|                   |   | CA3             | 1 (CAPD.3)             | x          | x          | x       |

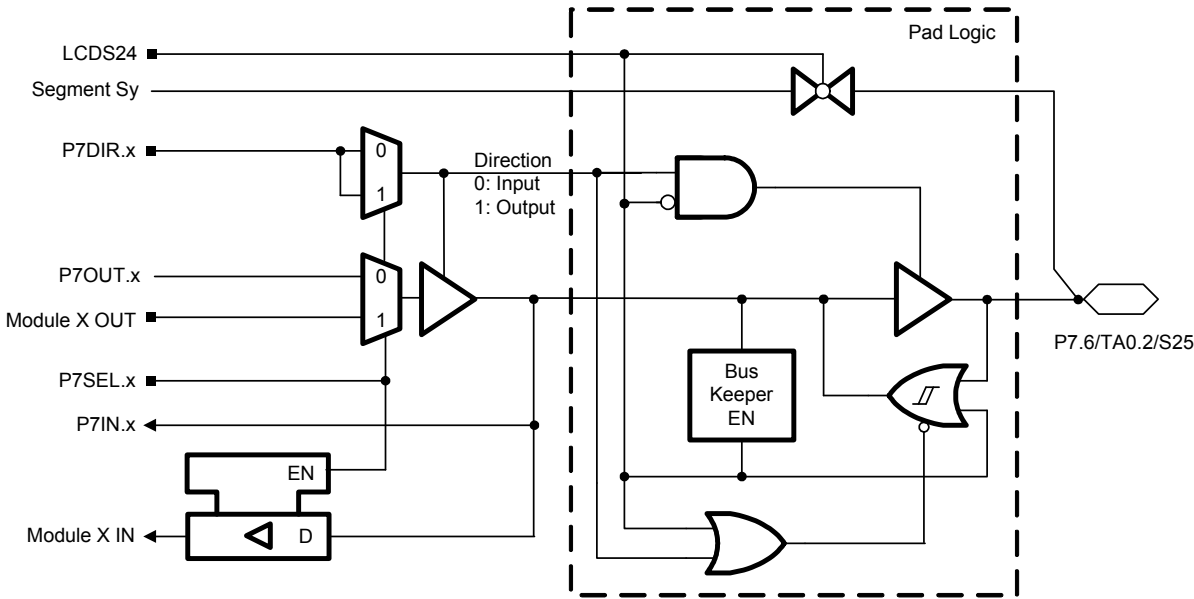
NOTES: 1. x: Don't care

MSP430F41x2  
MIXED SIGNAL MICROCONTROLLER

SLAS648E – APRIL 2009 – REVISED MARCH 2011

APPLICATION INFORMATION

Port P7 pin schematic: P7.6, input/output with Schmitt trigger



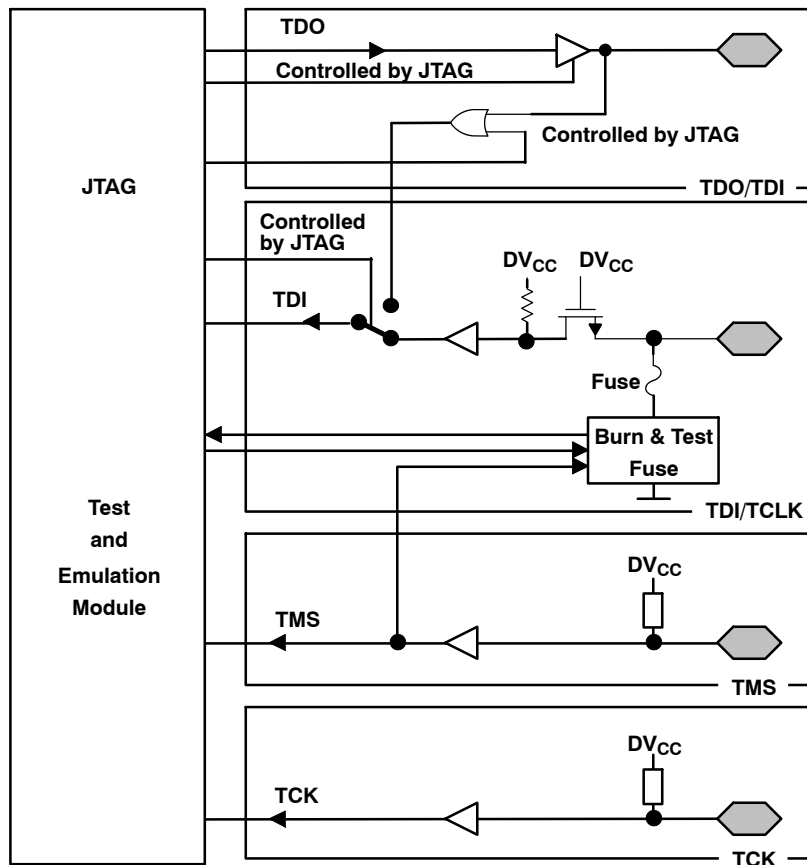
Port P7 (P7.6) pin functions

| PIN NAME (P7.X) | X | FUNCTION        | CONTROL BITS / SIGNALS |         |        |
|-----------------|---|-----------------|------------------------|---------|--------|
|                 |   |                 | P7DIR.x                | P7SEL.x | LCDS24 |
| P7.6/TA0.2/S25  | 6 | P7.x (I/O)      | I: 0, O: 1             | 0       | 0      |
|                 |   | Timer0_A3.CCI2A | 0                      | 1       | 0      |
|                 |   | Timer0_A3.TA2   | 1                      | 1       | 0      |
|                 |   | S25             | x                      | x       | 1      |

NOTES: 1. x: Don't care

## APPLICATION INFORMATION

**JTAG pins: TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger**



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

### JTAG fuse check mode

For details on the JTAG fuse check mode, see the *MSP430 Memory Programming User's Guide* (SLAU265) chapter "Fuse Check and Reset of the JTAG State Machine (TAP Controller)".

# MSP430F41x2

## MIXED SIGNAL MICROCONTROLLER

SLAS648E – APRIL 2009 – REVISED MARCH 2011

### Data Sheet Revision History

| LITERATURE NUMBER | SUMMARY                                                                                                                                                                                                                                                                                                                                                      |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SLAS648           | Production Data release                                                                                                                                                                                                                                                                                                                                      |
| SLAS648A          | Changed TDI/TCLK to TEST in Note 1 of “absolute maximum ratings” table (page 23)<br>Changed lower limit of Storage temperature, Programmed device from -40°C to -55°C in “absolute maximum ratings” table (page 23)                                                                                                                                          |
| SLAS648B          | Corrected Timer_A3 Signal Connections and Timer_A5 Signal Connections tables (pages 17, 18)<br>Removed bullet indicating that Segment A contains calibration data (page 15)                                                                                                                                                                                  |
| SLAS648C          | Added note to functional block diagram (page 5)                                                                                                                                                                                                                                                                                                              |
| SLAS648D          | In “absolute maximum ratings” table, changed LFXT1 crystal frequency, $f_{(LFXT1)}$ MIN from 450 to 0.45 MHz (with ceramic resonator) and from 1000 to 1 MHz (with crystal) (page 23)<br>In “crystal oscillator, LFXT1, high frequency modes” table, changed $f_{LFXT1}$ MAX from 8 to 6 MHz for both ceramic and crystal resonator (page 36) $t_{d(SVSON)}$ |
| SLAS648E          | Changed limits on $t_{d(SVSON)}$ parameter (page 31)                                                                                                                                                                                                                                                                                                         |



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| MSP430F4132IPM   | ACTIVE        | LQFP         | PM                 | 64   | 160         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | -40 to 85    | M430F4132                | <a href="#">Samples</a> |
| MSP430F4132IPMR  | ACTIVE        | LQFP         | PM                 | 64   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | -40 to 85    | M430F4132                | <a href="#">Samples</a> |
| MSP430F4132IRGZR | ACTIVE        | VQFN         | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | -40 to 85    | M430<br>F4132            | <a href="#">Samples</a> |
| MSP430F4132IRGZT | ACTIVE        | VQFN         | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | -40 to 85    | M430<br>F4132            | <a href="#">Samples</a> |
| MSP430F4152IPM   | ACTIVE        | LQFP         | PM                 | 64   | 160         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | -40 to 85    | M430F4152                | <a href="#">Samples</a> |
| MSP430F4152IPMR  | ACTIVE        | LQFP         | PM                 | 64   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | -40 to 85    | M430F4152                | <a href="#">Samples</a> |
| MSP430F4152IRGZ  | OBSOLETE      | VQFN         | RGZ                | 48   |             | TBD                        | Call TI          | Call TI              | -40 to 85    |                          |                         |
| MSP430F4152IRGZR | ACTIVE        | VQFN         | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  | -40 to 85    | M430<br>F4152            | <a href="#">Samples</a> |
| MSP430F4152IRGZT | ACTIVE        | VQFN         | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | M430<br>F4152            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

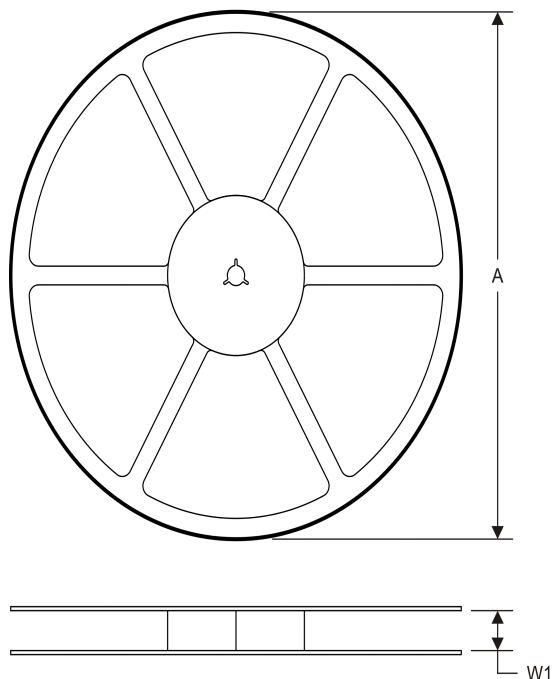
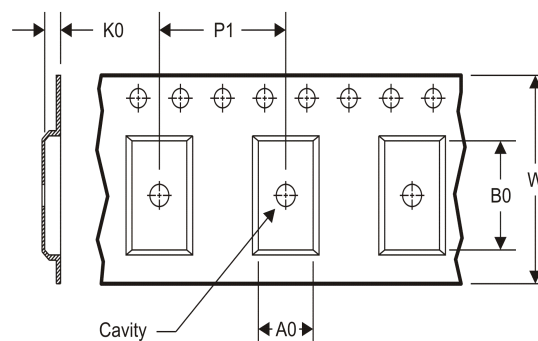
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


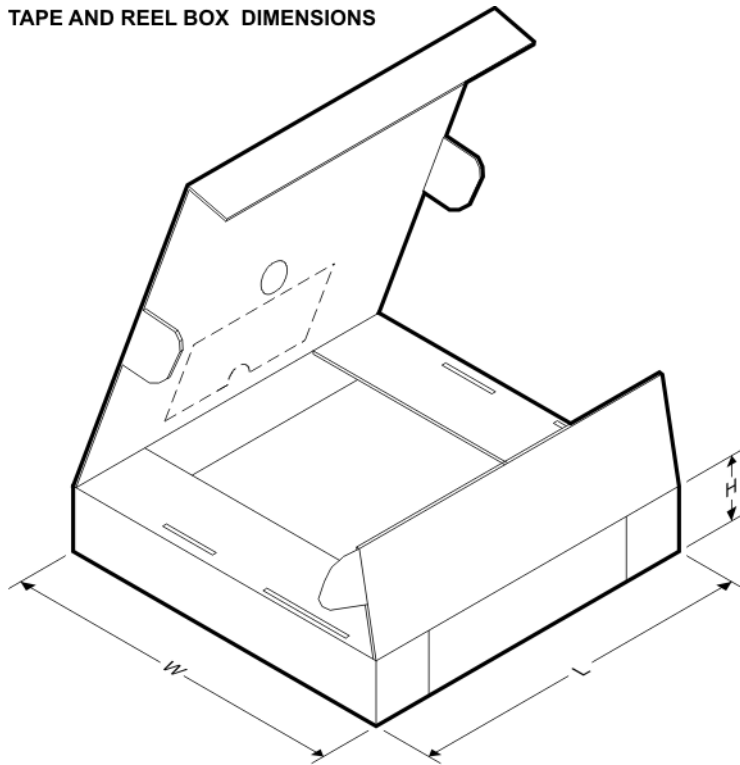
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F4132IPMR | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |
| MSP430F4152IPMR | LQFP         | PM              | 64   | 1000 | 330.0              | 24.4               | 13.0    | 13.0    | 2.1     | 16.0    | 24.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

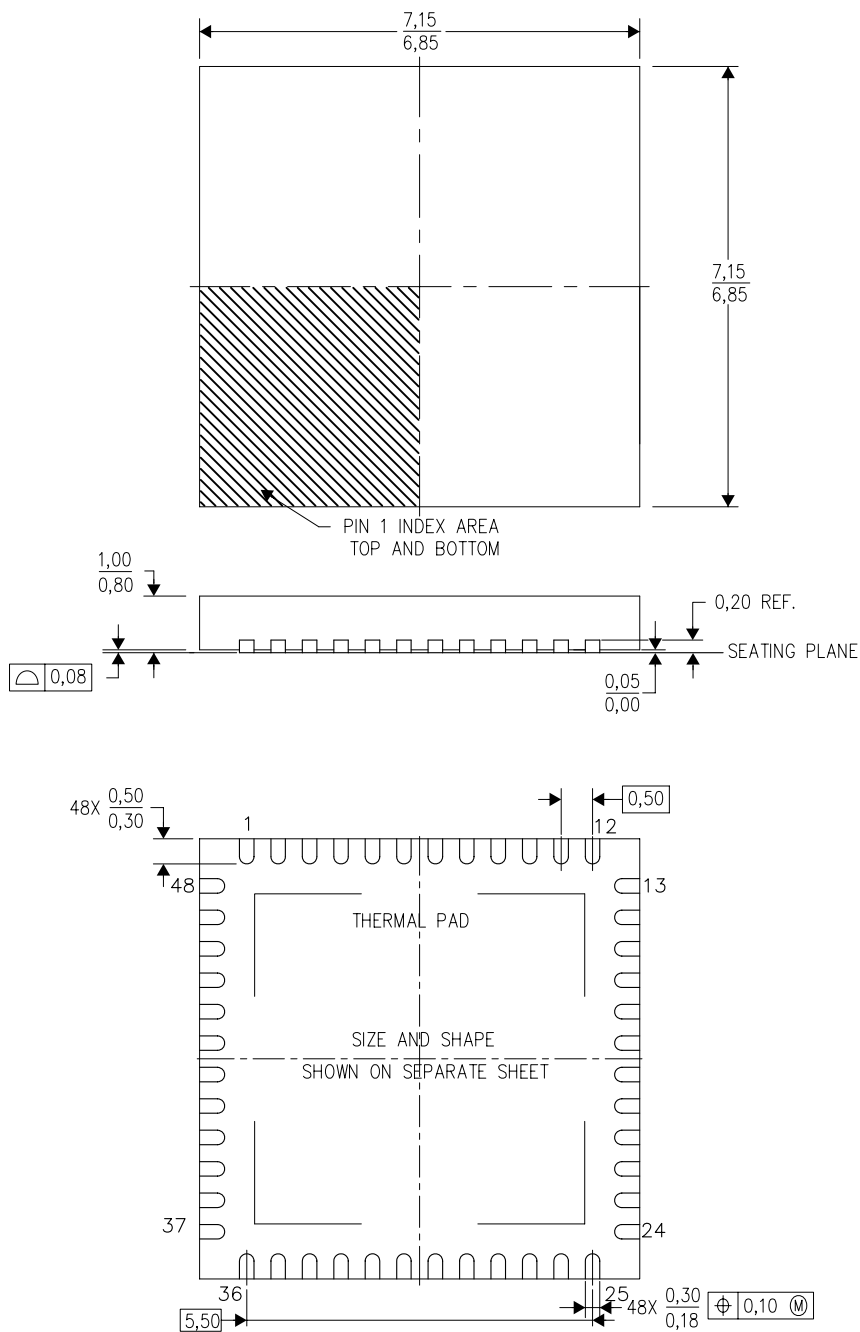


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F4132IPMR | LQFP         | PM              | 64   | 1000 | 367.0       | 367.0      | 45.0        |
| MSP430F4152IPMR | LQFP         | PM              | 64   | 1000 | 367.0       | 367.0      | 45.0        |

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

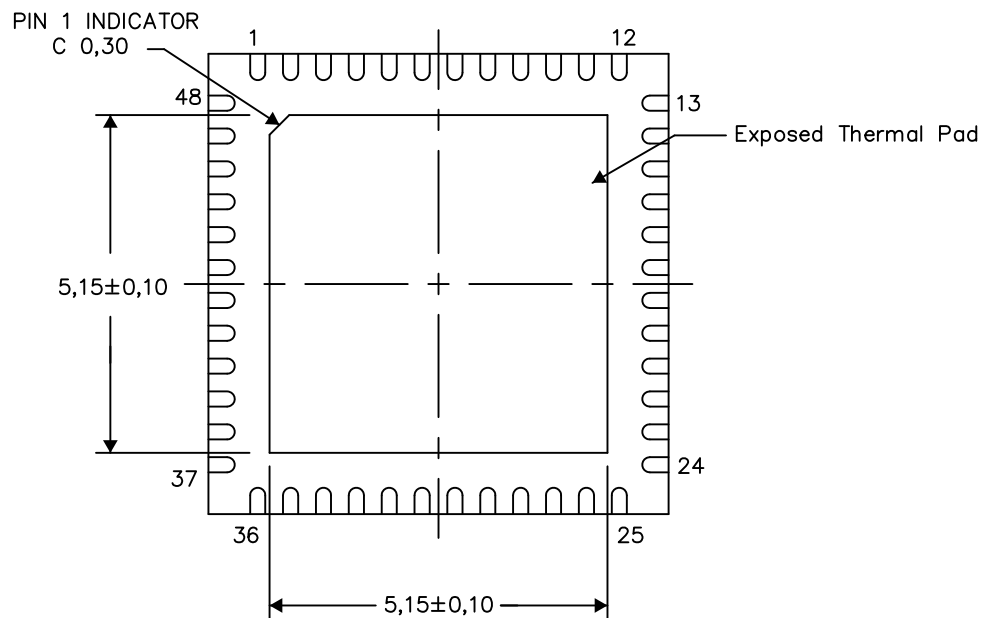
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

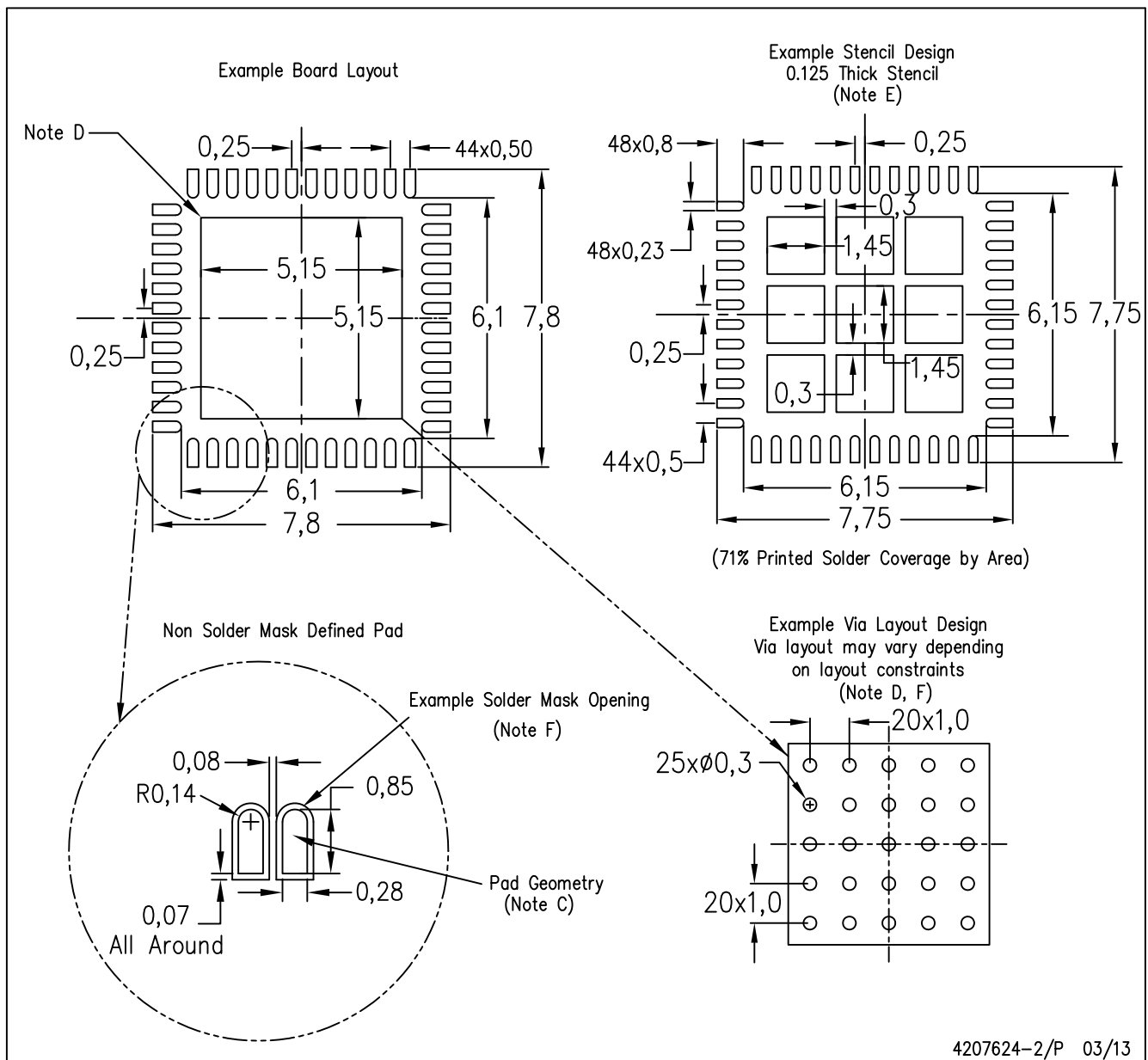
Exposed Thermal Pad Dimensions

4206354-2/T 03/13

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

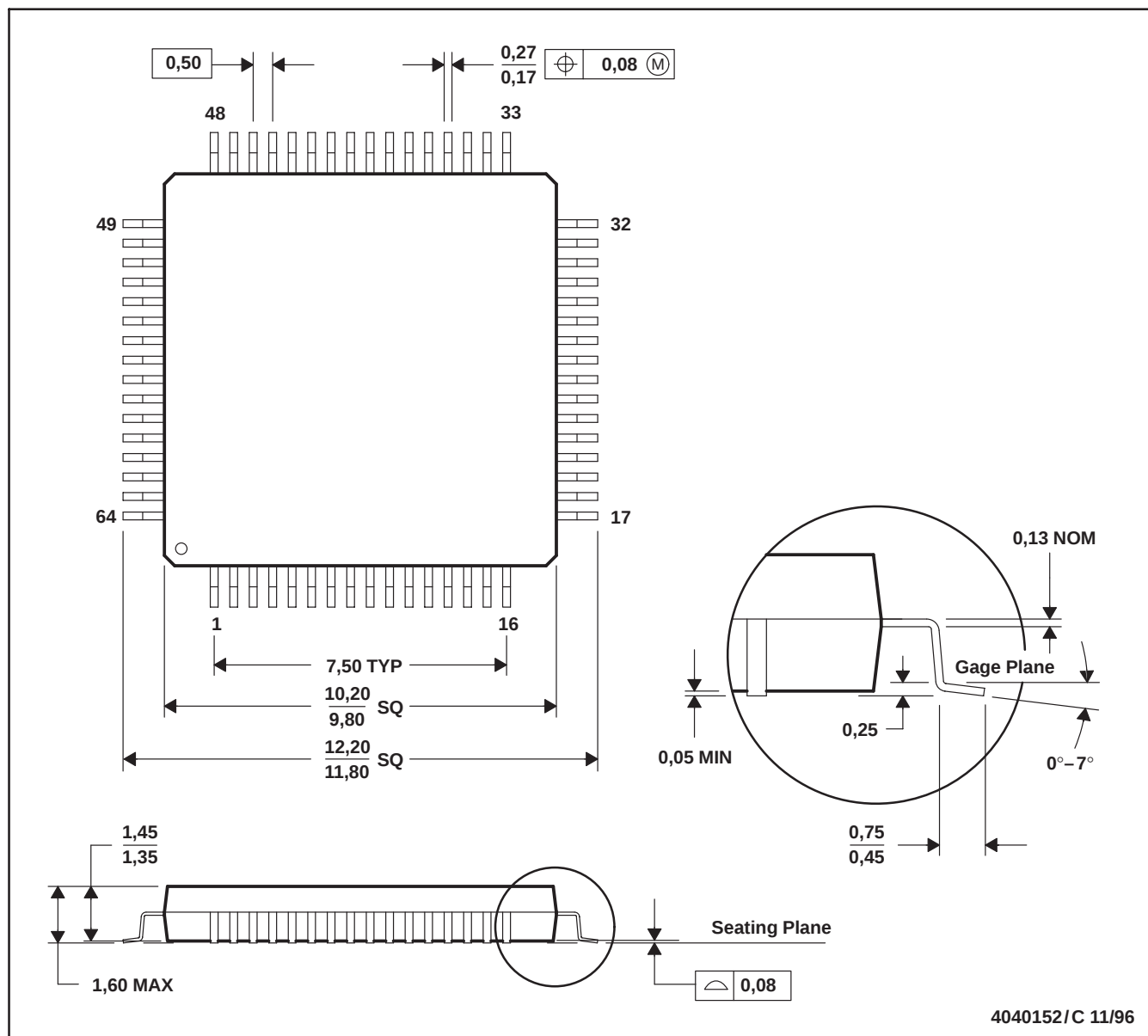
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## PM (S-PQFP-G64)

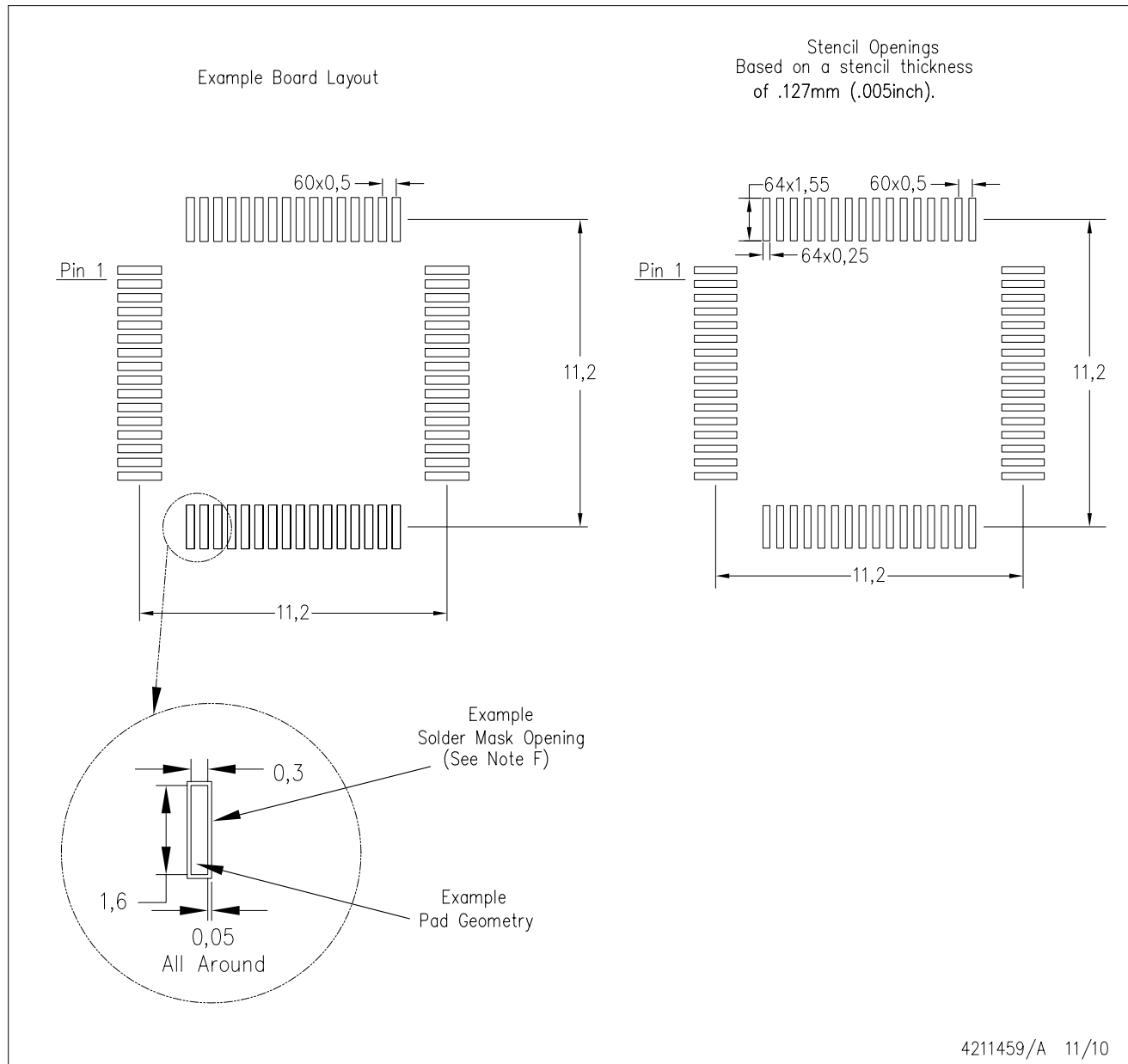
## PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-026
  - D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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