



74LVC595A

8-bit serial-in/serial-out or parallel-out shift register; 3-state

Rev. 6 — 9 May 2025

Product data sheet

1. General description

The 74LVC595A is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset MR input. A LOW on MR will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power dissipation
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

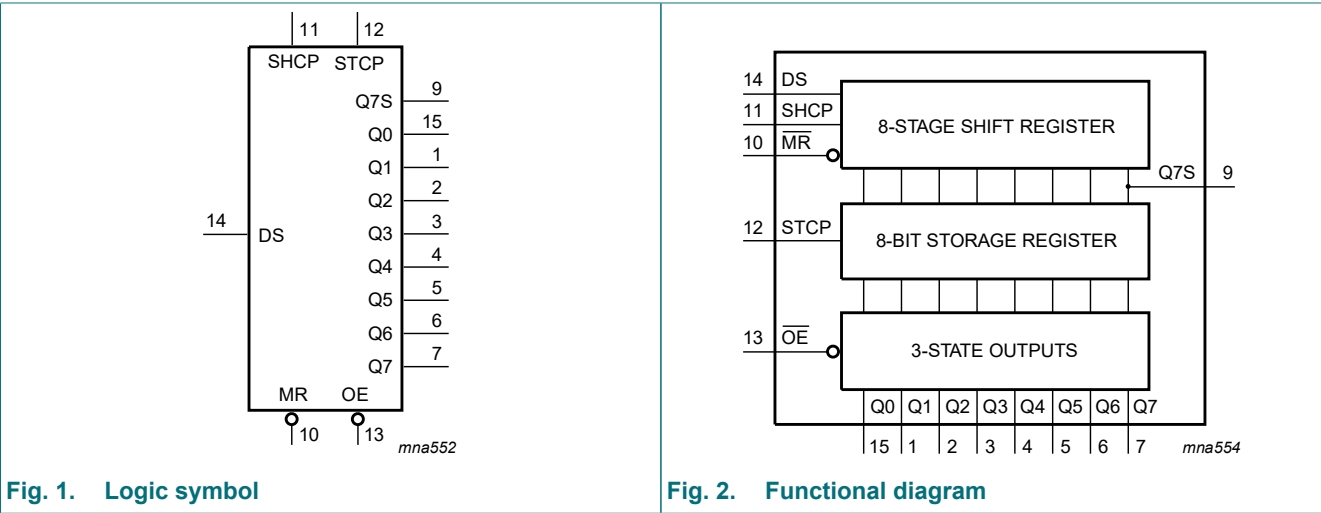
- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC595AD	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC595APW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC595ABQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74LVC595ABZ	-40 °C to +125 °C	DHXQFN16	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 16 terminals; 0.4 mm pitch; body 2 mm × 2.4 mm × 0.48 mm	SOT8016-1

5. Functional diagram



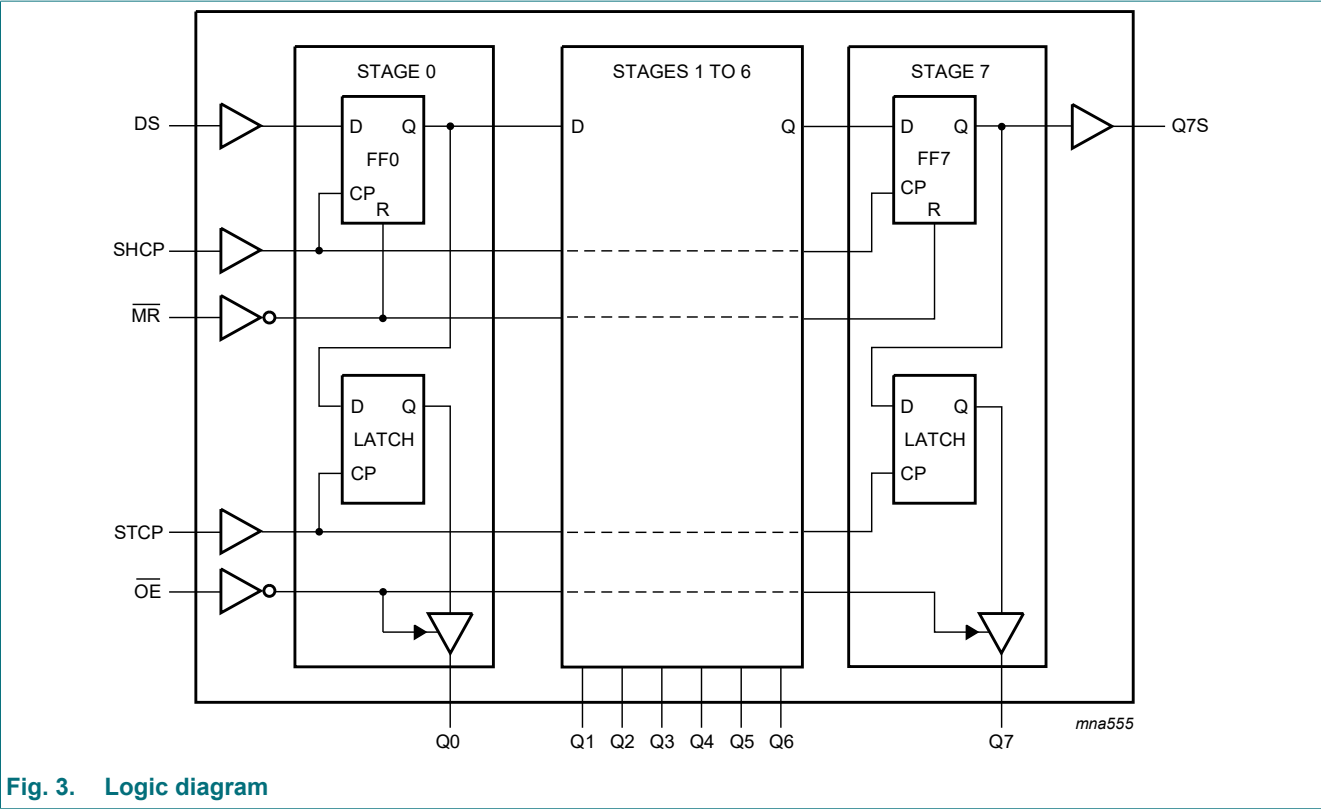


Fig. 3. Logic diagram

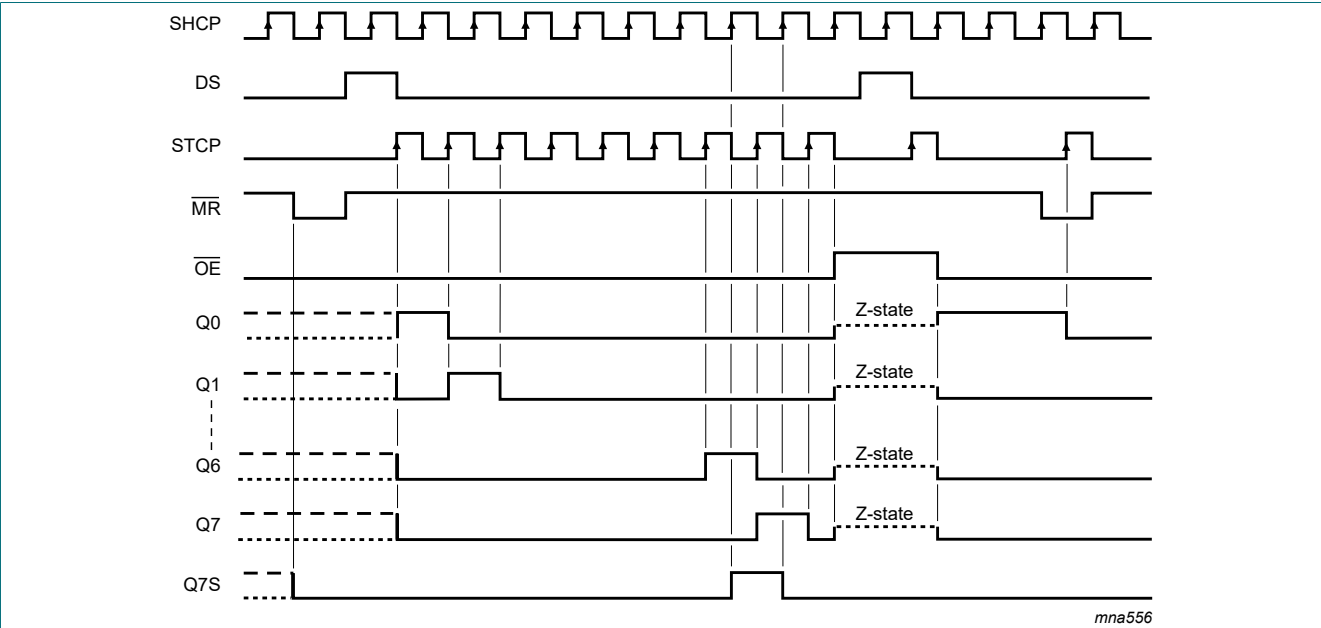
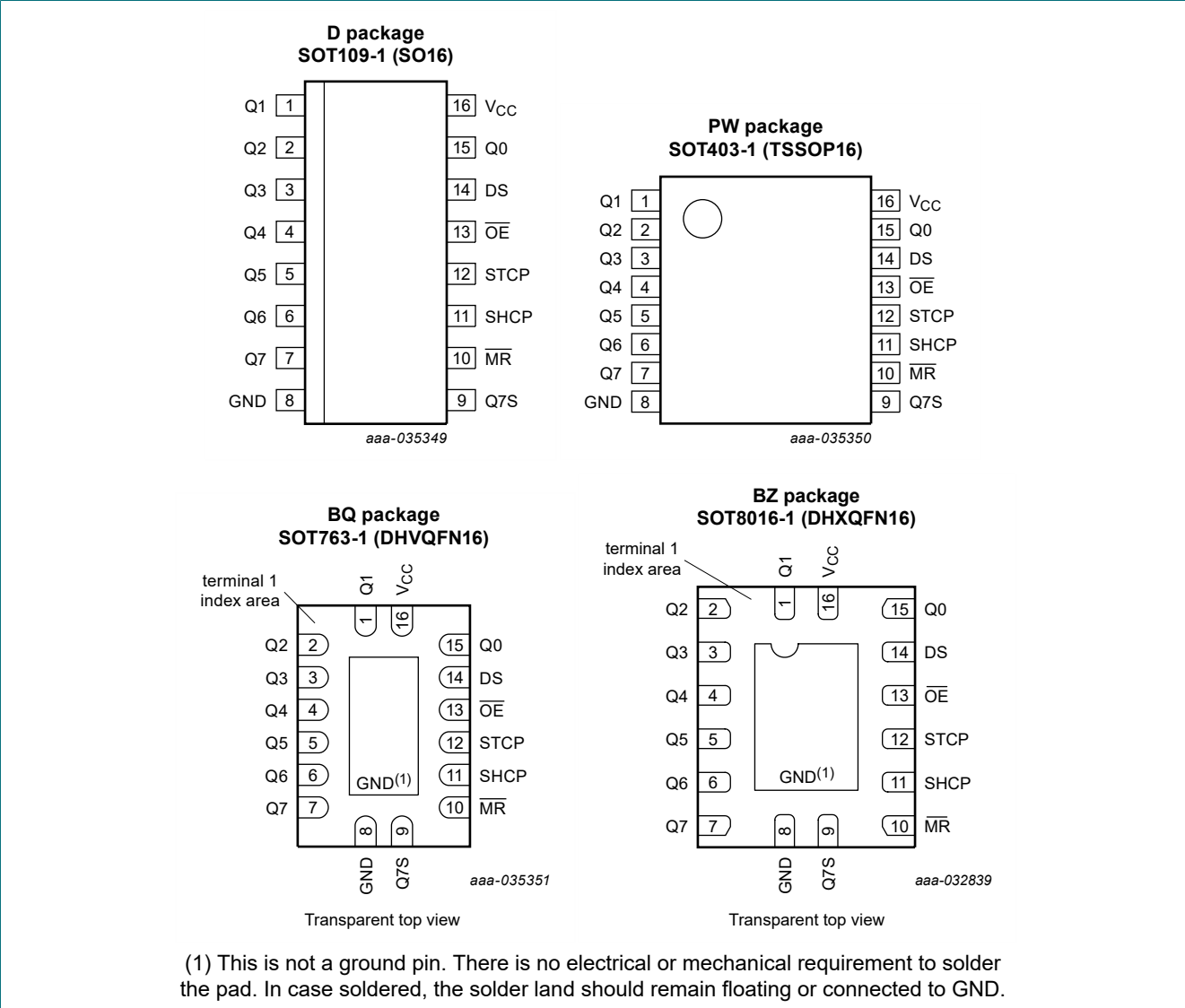


Fig. 4. Timing diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
OE	13	output enable input (active LOW)
DS	14	serial data input
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition; X = don't care; NC = no change; Z = high-impedance OFF-state.

Input					Output		Function
SHCP	STCP	OE	MR	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-state on MR only affects the shift register
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-state shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	3-state [1]	-0.5	6.5	V
		output HIGH or LOW state [1]	-0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA

8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SOT109-1 (SO16) [2] SOT403-1 (TSSOP16) [3] SOT763-1 (DHVQFN16) [4]	-	500	mW
		SOT8016-1 (DHXQFN16)	-	250	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
[3] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
[4] For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	3-state	0	-	5.5	V
		output HIGH or LOW state	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V

8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V [2]	-	0.1	±10	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	0.1	10	-	20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 1.65 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.
[2] For transceivers, the parameter I_{OZ} includes the input leaking current.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	SHCP to Q7S; see Fig. 5 [2]						
		V _{CC} = 1.2 V	-	17.5	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	6.6	15.8	2.0	18.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	4.2	8.1	1.5	9.3	ns
		V _{CC} = 2.7 V	1.5	4.7	7.6	1.5	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	4.0	6.7	1.5	7.7	ns
		STCP to Qn; see Fig. 6 [2]						
		V _{CC} = 1.2 V	-	16.8	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	5.8	15.8	2.0	18.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.7	8.1	1.5	9.3	ns
		V _{CC} = 2.7 V	1.5	4.0	7.6	1.5	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	3.3	6.7	1.2	7.7	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Q7S; see Fig. 9						
		V _{CC} = 1.2 V	-	17.3	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	6.9	15.8	2.0	18.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	4.3	8.1	1.5	9.3	ns
		V _{CC} = 2.7 V	1.5	4.5	7.6	1.5	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	3.8	6.7	1.2	7.7	ns
t _{en}	enable time	OE to Qn; see Fig. 10 [3]						
		V _{CC} = 1.2 V	-	17.9	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	6.4	14.1	2.0	16.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	4.2	8.0	1.5	9.2	ns
		V _{CC} = 2.7 V	1.5	4.5	7.6	1.5	8.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	3.8	6.7	1.2	7.7	ns
t _{dis}	disable time	OE to Qn; see Fig. 10 [4]						
		V _{CC} = 1.2 V	-	9.6	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	4.9	9.8	2.0	11.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.2	2.8	5.8	1.2	6.6	ns
		V _{CC} = 2.7 V	1.5	3.7	6.2	1.5	7.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	3.5	5.7	1.2	6.5	ns

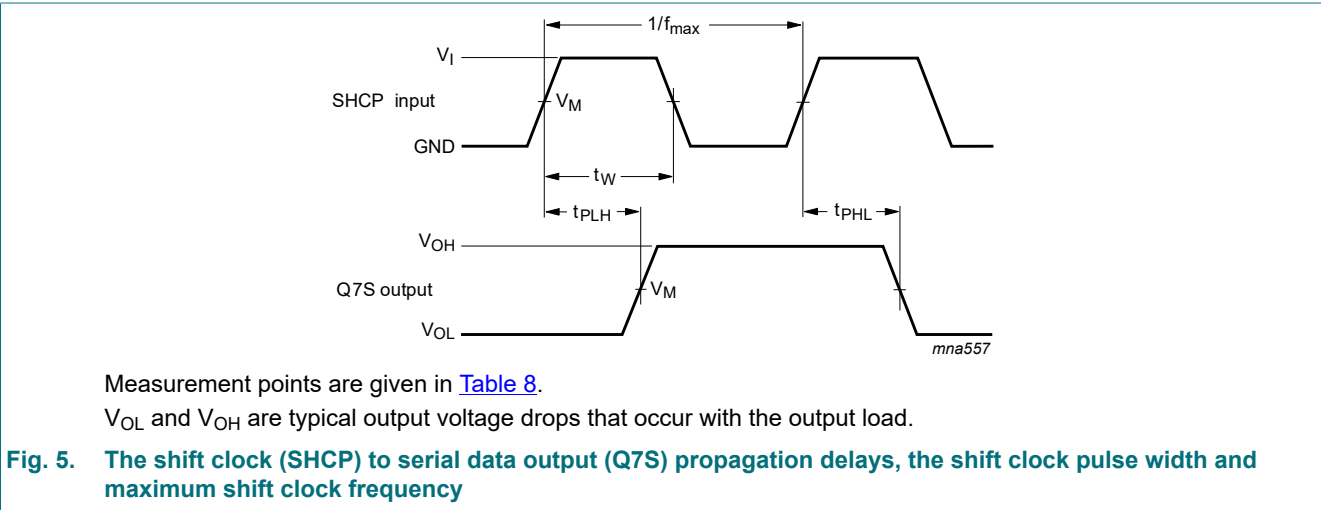
8-bit serial-in/serial-out or parallel-out shift register; 3-state

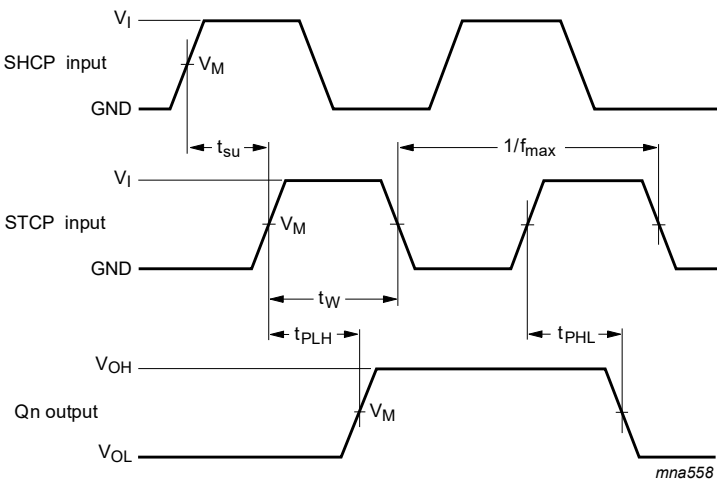
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_W	pulse width	SHCP, STCP HIGH or LOW; see Fig. 5 and Fig. 6						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	6.0	2.5	-	7.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	5.0	2.0	-	5.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	4.5	1.5	-	5.0	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	4.0	1.5	-	4.5	-	ns
		$\overline{\text{MR}}$ LOW; see Fig. 9						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	5.0	2.0	-	5.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	4.0	1.5	-	4.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	2.5	1.0	-	3.0	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.5	1.0	-	3.0	-	ns
t_{su}	set-up time	DS to SHCP; see Fig. 7						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	5.0	0.4	-	5.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	4.0	0.1	-	4.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	2.0	0	-	2.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-0.1	-	2.5	-	ns
		$\overline{\text{MR}}$ to STCP; see Fig. 8						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	8.0	3.5	-	8.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	5.0	2.1	-	5.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	4.0	1.8	-	4.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	4.0	1.7	-	4.5	-	ns
		SHCP to STCP; see Fig. 6						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	8.0	3.5	-	8.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	5.0	2.1	-	5.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	4.0	1.8	-	4.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	4.0	1.7	-	4.5	-	ns
t_h	hold time	DS to SHCP; see Fig. 7						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.5	0.2	-	2.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	0.1	-	2.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-0.1	-	2.0	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	-0.2	-	1.5	-	ns
t_{rec}	recovery time	$\overline{\text{MR}}$ to SHCP; see Fig. 9						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	5.0	-2.7	-	5.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	4.0	-1.5	-	4.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	2.0	-1.0	-	2.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-1.0	-	2.5	-	ns
f_{max}	maximum frequency	SHCP or STCP; see Fig. 5 and Fig. 6						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	80	130	-	70	-	MHz
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	100	140	-	90	-	MHz
		$V_{CC} = 2.7 \text{ V}$	110	150	-	100	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	130	180	-	115	-	MHz
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ [5]	-	-	1.0	-	1.5	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} [6]						
		V _{CC} = 1.65 V to 1.95 V	-	50	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	45	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	44	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] t_{en} is the same as t_{PZH} and t_{PZL}.
- [4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
- [5] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

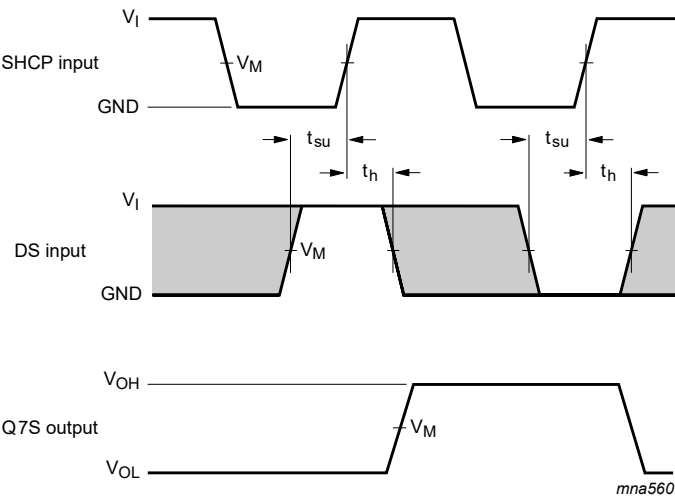
11.1. Waveforms and test circuit





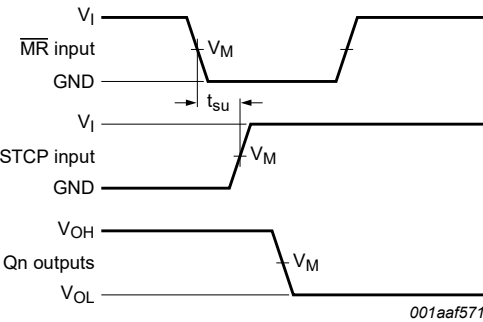
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig. 6. The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time



Measurement points are given in [Table 8](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig. 7. The data set-up and hold times for the serial data input (DS)



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig. 8. The master reset ($\overline{MR}$) to storage clock (STCP) set-up times

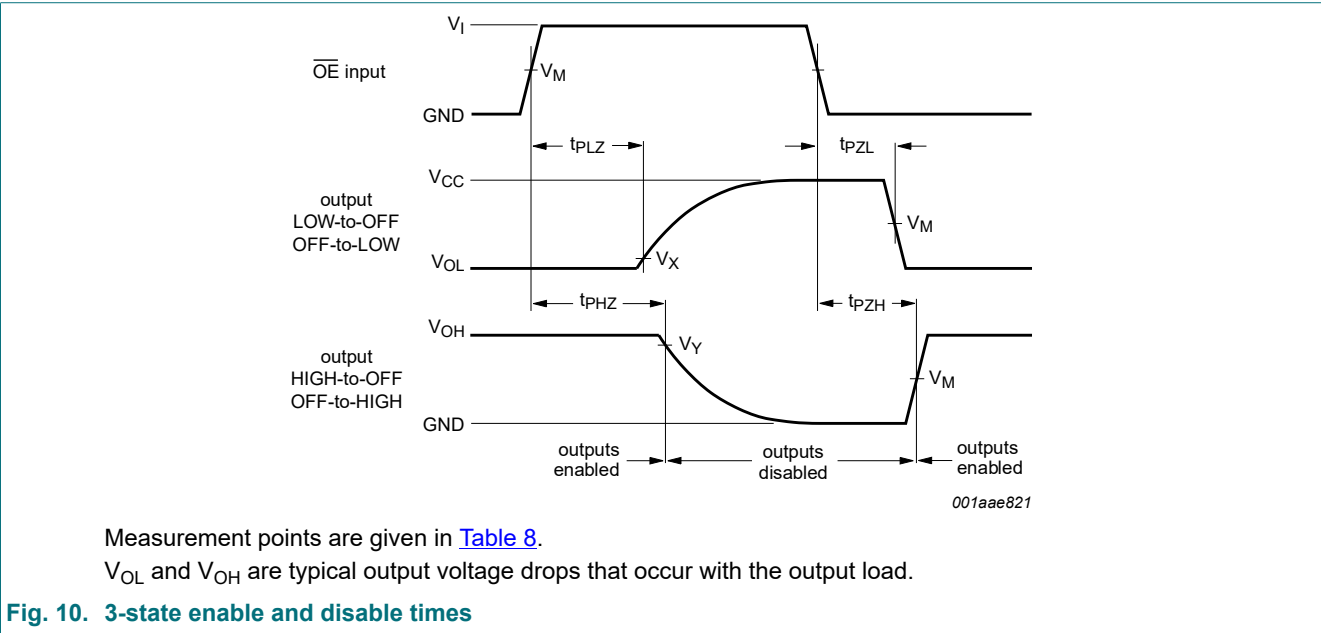
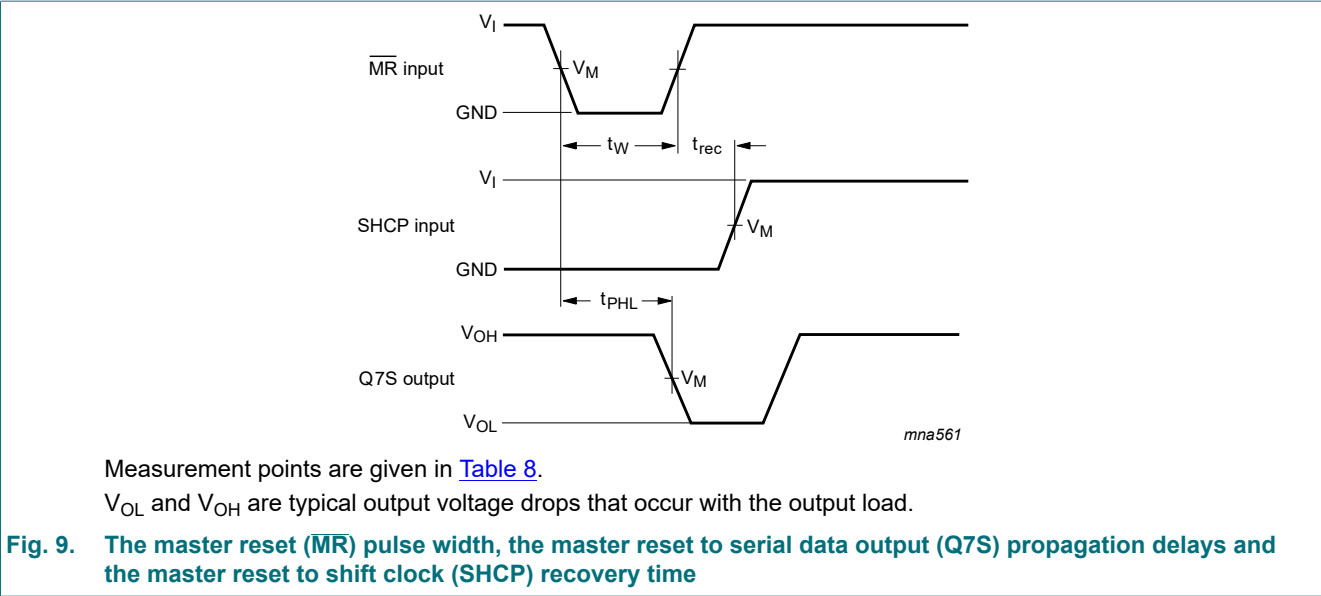


Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
$V_{CC} < 2.7 \text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
$V_{CC} \geq 2.7 \text{ V}$	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

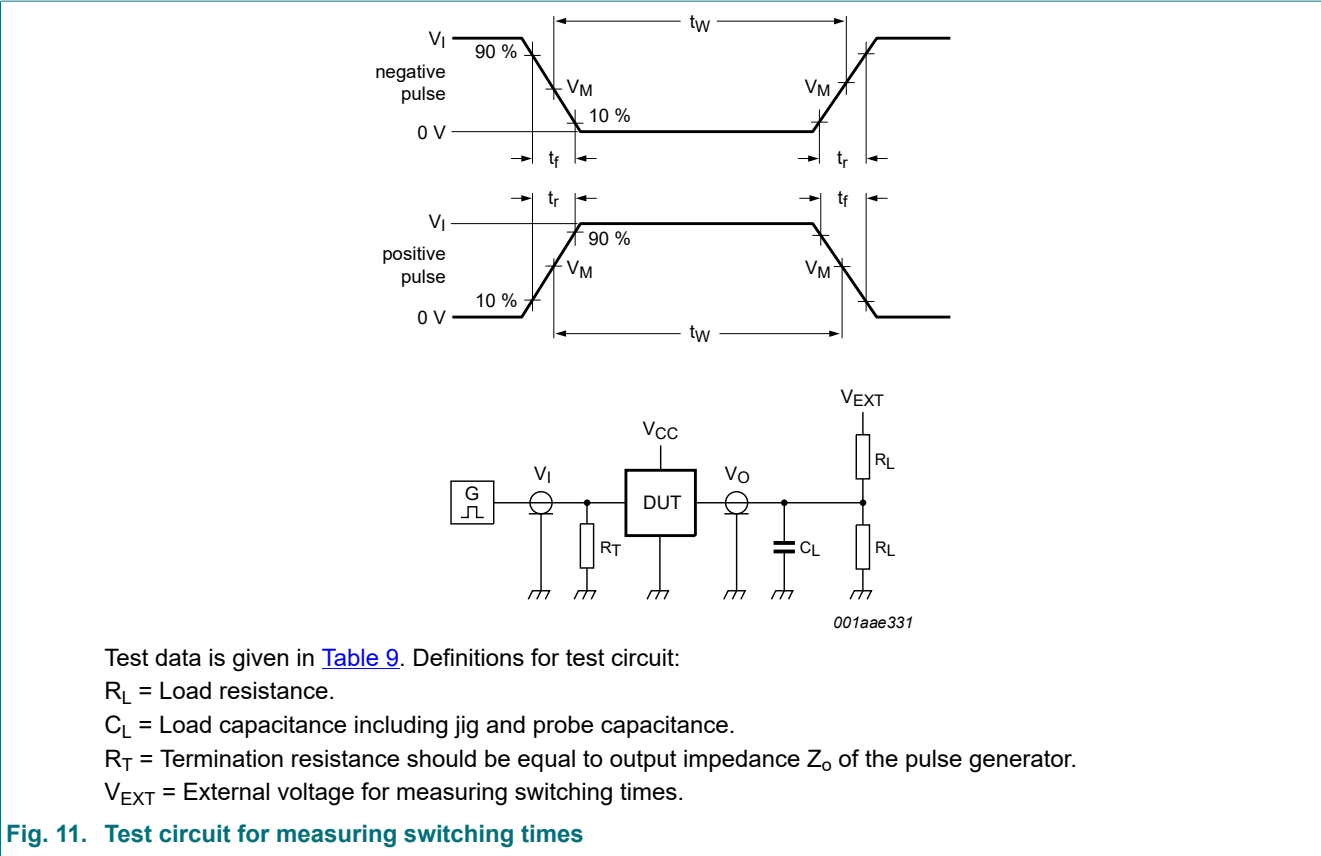


Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

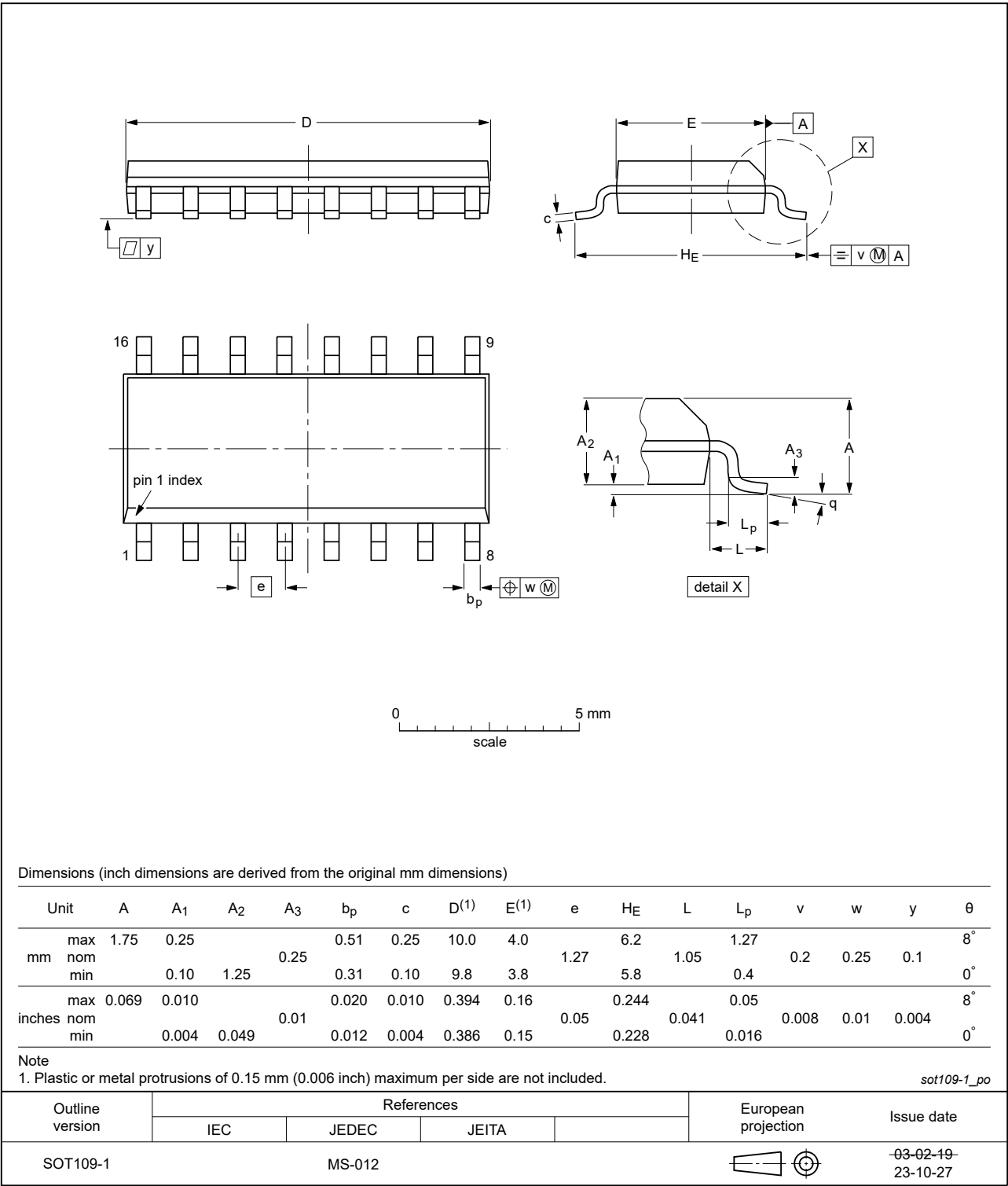


Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

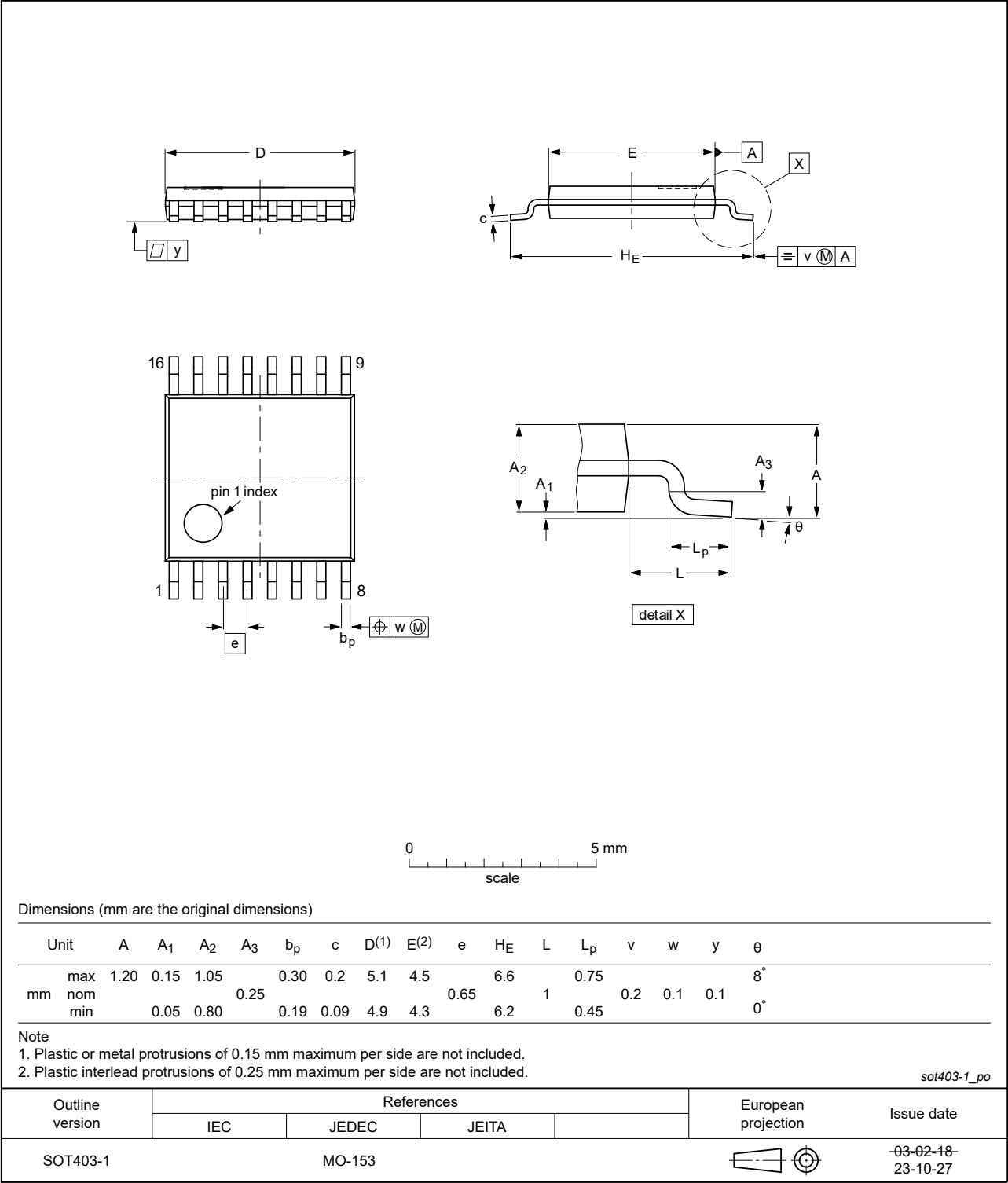


Fig. 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

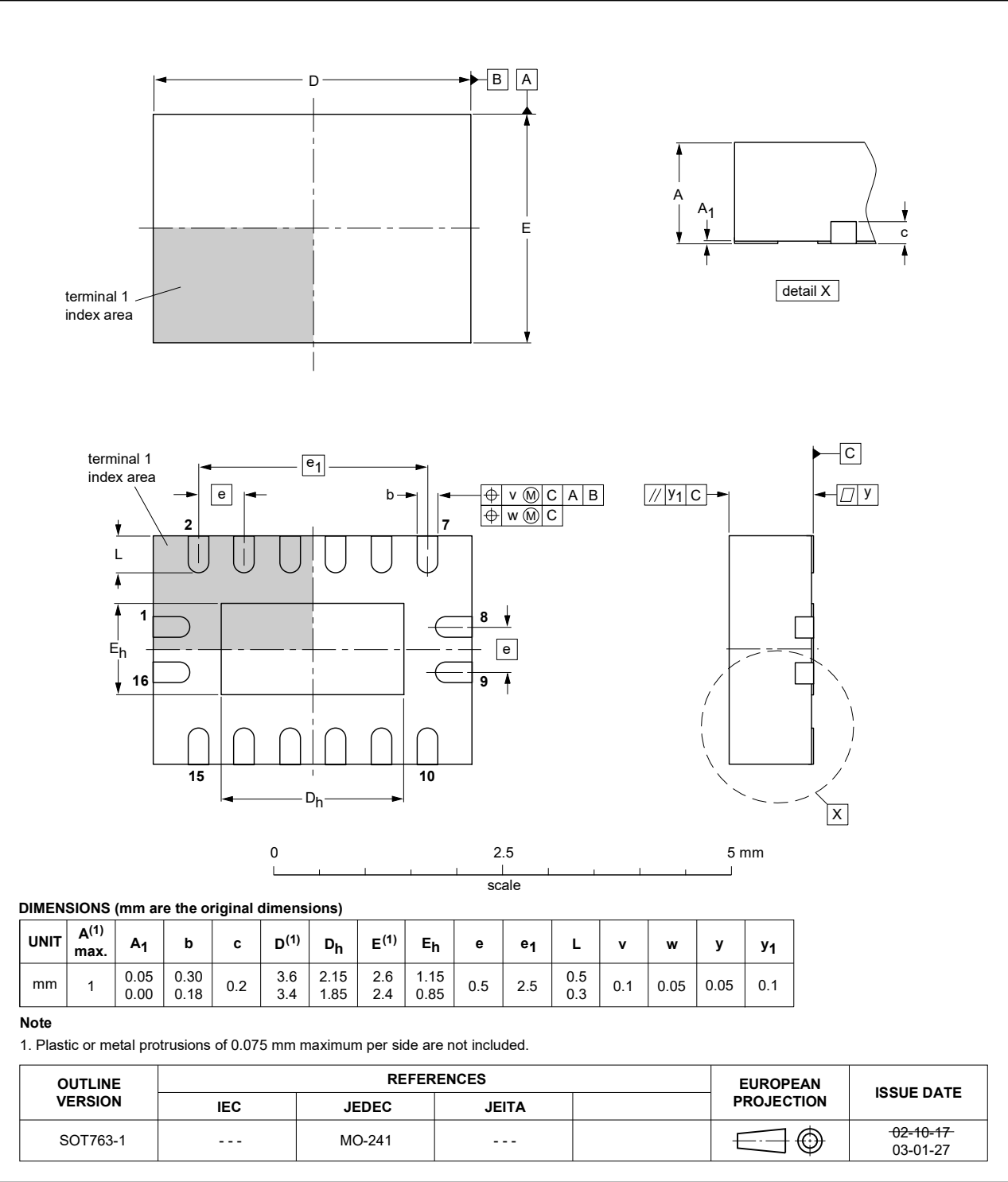


Fig. 14. Package outline SOT763-1 (DHVQFN16)

DHXQFN16: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package;
no leads; 16 terminals; 0.4 mm pitch; body 2 mm x 2.4 mm x 0.48 mm

SOT8016-1

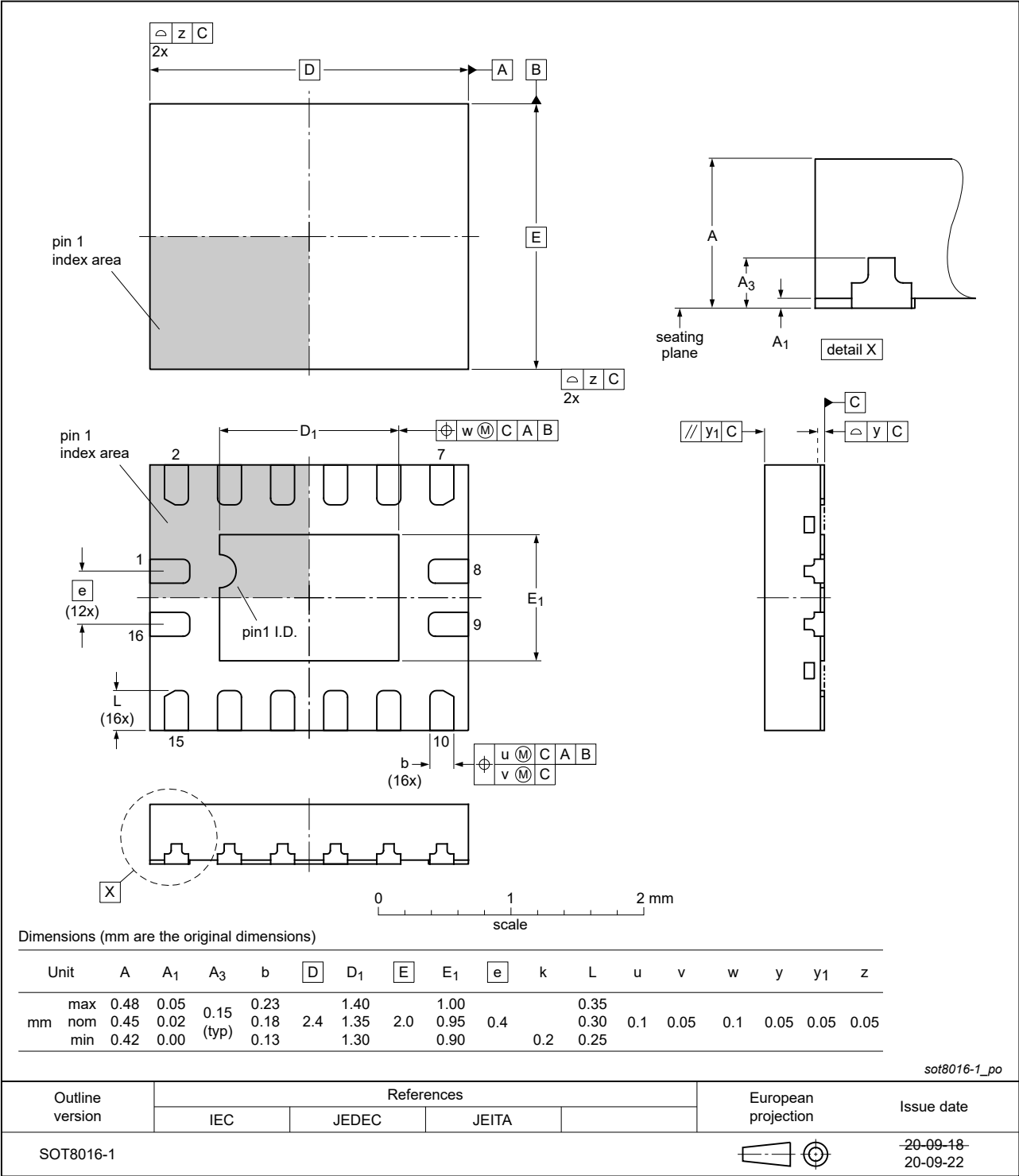


Fig. 15. Package outline SOT8016-1 (DHXQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC595A v.6	20250509	Product data sheet	-	74LVC595A v.5
Modifications:	• Type number 74LVC595ABZ (SOT8016-1/DHXQFN16) added.			
74LVC595A v.5	20240222	Product data sheet	-	74LVC595A v.4
Modifications:	• Fig. 12 , Fig. 13 : Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LVC595A v.4	20230829	Product data sheet	-	74LVC595A v.3
Modifications:	• Section 2 : ESD specification updated according to the latest JEDEC standard.			
74LVC595A v.3	20211119	Product data sheet	-	74LVC595A v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 8 : Derating values for P _{tot} total power dissipation have been updated.			
74LVC595A v.2	20140620	Product data sheet	-	74LVC595A v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Figure note for Section 6.1 added.			
74LVC595A v.1	20070529	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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