

POWER MANAGEMENT

Features

- Input Voltage Range — 2.9 to 5.5V
- Output Voltage Range — 0.8V to 3.3V
- Output Current — up to 4A for each channel
- Ultra-Small Footprint — <1mm Height Solution
- Switching Frequency — 1.6MHz
- Automatic Power Save Mode
- Efficiency Up to 95%
- Low Output Noise Across Load Range
- Excellent Transient Response
- Start Up into Pre-Bias Output
- Duty-Cycle Low Dropout Operation — 100%
- Shutdown Current — <1 μ A
- Externally Programmable Soft Start Time
- Power Good indicator
- Input Under-Voltage Lockout
- Output Over-Voltage, Current Limit Protection
- Over-Temperature Protection
- Thermally Enhanced 4 x 4 x 0.6 (mm) MLPQ-UT28 package
- Lead-free, Halogen free, and RoHS/WEEE compliant

Applications

- Routers and Network Cards
- LCD TV
- Office Automation
- Printers

Description

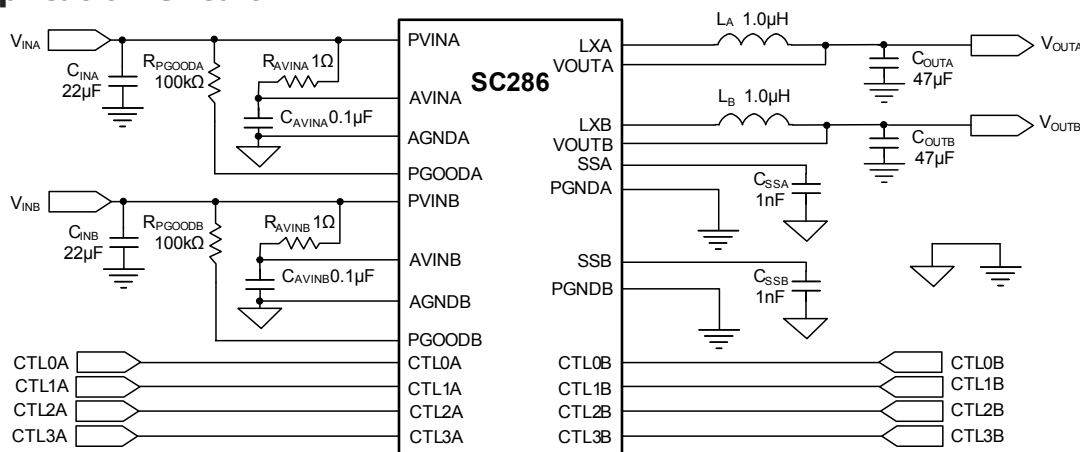
The SC286 is a dual channel 4A synchronous step-down regulator designed to operate with an input voltage range of 2.9V to 5.5V. Each channel offers fifteen pre-determined output voltages via separate control pins programmable from 0.8 to 3.3 Volts. The control pins allow for on-the-fly voltage changes, enabling system designers to implement dynamic power savings. The device is also capable of adjusting output voltage via an external resistor divider.

The SC286 is optimized for maximum efficiency over a wide range of load currents. During full load operation, the device operates in PWM mode with fixed 1.6MHz oscillator frequency, allowing the use of small surface mount external components. As the load decreases, the regulator will transition into Power Save mode maintaining high efficiency.

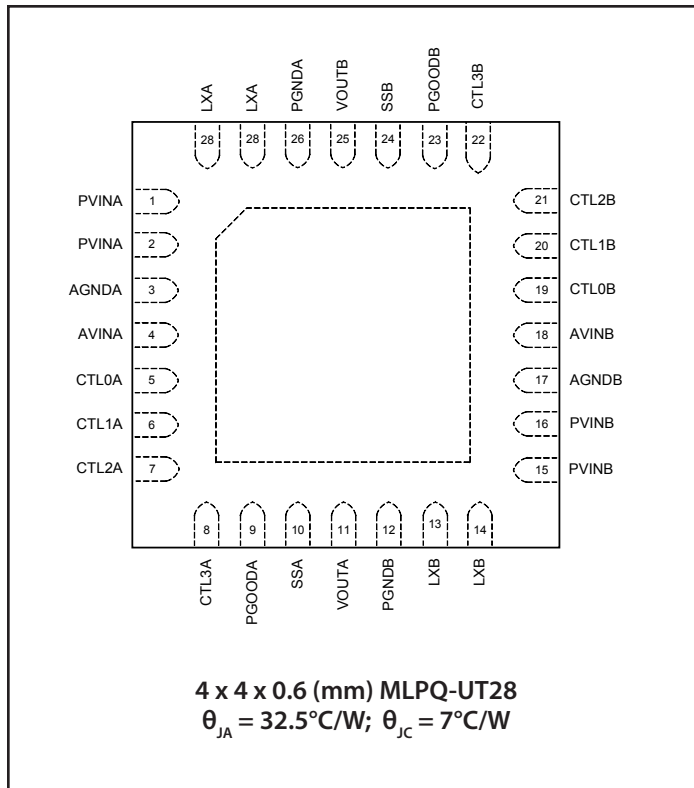
Connecting the control pins to logic low forces the device into shutdown mode reducing the supply current to less than 1 μ A. Connecting any of the control pins to logic high enables the converter and sets the output voltage according to Table 1. Other features include under-voltage lockout, programmable soft-start to limit in-rush current, power good indicator, over-temperature protection, and output short circuit protection.

The SC286 is available in a thermally-enhanced, 4 x 4 x 0.6 (mm) MLPQ-UT28 package and has a rated temperature range of -40 to +85°C.

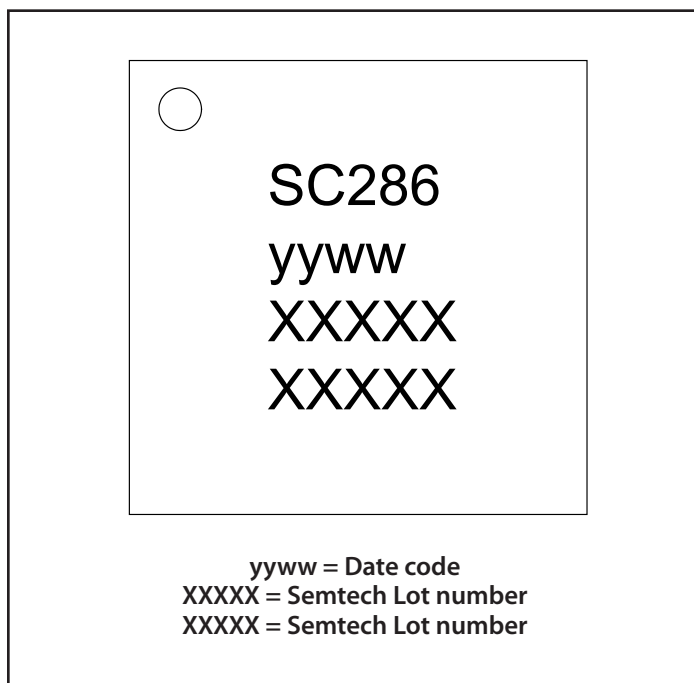
Typical Application Circuit



Pin Configuration



Marking Information



Ordering Information

Device	Package
SC286ULTRT ⁽¹⁾⁽²⁾	4 x 4 x 0.6 (mm) MLPQ-UT28
SC286EVB	Evaluation Board

Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Device is lead-free, Halogen free, and RoHS/WEEE compliant.

Table 1 – Output Voltage Settings for Each Channel

CTL3A/B	CTL2A/B	CTL1A/V	CTL0A/B	Output Voltage
0	0	0	0	Shutdown
0	0	0	1	0.8
0	0	1	0	1.00
0	0	1	1	1.025
0	1	0	0	1.05
0	1	0	1	1.20
0	1	1	0	1.25
0	1	1	1	1.30
1	0	0	0	1.50
1	0	0	1	1.80
1	0	1	0	2.20
1	0	1	1	2.50
1	1	0	0	2.60
1	1	0	1	2.80
1	1	1	0	3.00
1	1	1	1	3.30

Absolute Maximum Ratings

PVINA/B and AVINA/B Supply Voltages (V) ... -0.3 to +6.0
 LXA, LXB (V) ⁽¹⁾ -0.3 to PVIN +0.3V, 6V Max
 VOUTA, VOUTB (V) -0.3 to AVIN + 0.3
 CTLX_A, CTLX_B pins (V) -0.3 to AVIN + 0.3
 VOUTA, VOUTB Short Circuit Duration Continuous
 ESD Protection Level⁽²⁾ (kV) 3

Recommended Operating Conditions

PVINA/B and AVINA/B Supply (V) 2.9 to +5.5
 Maximum Output Current, Each Channel (A) 4.0
 Input Capacitor, Each Channel (μF) 22
 Output Capacitor, Each Channel (μF) 47 or 2 x 22
 Output Inductor, Each Channel (μH) 1.0

Thermal Information

Thermal Resistance, Junction to Ambient⁽³⁾ (°C/W) .. 32.5
 Thermal Resistance, Junction to Case (°C/W) 7
 Maximum Junction Temperature (°C) +150
 Storage Temperature Range (°C) -65 to +150
 Peak IR Reflow Temperature (10s to 30s) (°C) +260

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:

- (1) Due to parasitic board inductance, the transient LX pin voltage at the point of measurement may appear larger than that which exists on silicon. The device is designed to tolerate the short duration transient voltages that will appear on the LX pin due to the deadtime diode conduction, for inductor currents up to the current limit setting of the device.
- (2) Tested according to JEDEC standard JESD22-A114-B.
- (3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: PVIN = AVIN = 5.0V, VOUT = 1.50V, C_{IN} = 22μF, C_{OUT} = 2 x 22μF; L = 1.0μH; -40°C ≤ T_J ≤ +125 °C; Per Channel Unless otherwise noted; Typical values are T_A = +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under-Voltage Lockout	UVLO	Rising AVINA/B; PVINA/B=AVINA/B	2.70	2.80	2.90	V
		Hysteresis		300		mV
Output Voltage Tolerance ⁽¹⁾	ΔV _{OUT}	PVINA/B= AVINA/B= 2.9 to 5.5V; I _{OUT} =0A	-1.25		+1.25	%
Current Limit	I _{LIMIT}	Peak LX current	5.0	6.0	7.0	A
Supply Current	I _Q	I _{OUTA/B} = 0A		100		μA
Shutdown Current	I _{SHDN}	CTL3-0A/B = AGNDA/B		1	10	μA
High Side Switch Resistance ⁽²⁾	R _{DSON_P}	I _{LXA/B} = 100mA, T _J = 25 °C		50		mΩ
Low Side Switch Resistance ⁽²⁾	R _{DSON_N}	I _{LXA/B} = -100mA, T _J = 25 °C		35		
L _X Leakage Current ⁽²⁾	I _{LK(LX)}	PVINA/B = AVINA/B = 5.5V; LXA/B = 0V; CTL3-0A/B = AGNDA/B		1	10	μA
		PVINA/B = AVINA/B = 5.5V; LXA/B = 5.0V; CTL3-0A/B = AGNDA/B	-20	-1		

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Load Regulation	$\Delta V_{\text{LOAD-REG}}$	PVINA/B = AVINA/B = 5.0V, $I_{\text{OUT}}=800\text{mA}$ to 4A		± 0.3		%
Oscillator Frequency	f_{OSC}		1.275	1.600	1.925	MHz
Soft-Start Charging Current ⁽²⁾	I_{SS}			+5		μA
Foldback Holding Current	$I_{\text{CL_HOLD}}$	Average LX Current		1		A
Impedance of PGOOD Low	$R_{\text{PGOOD_LO}}$			10		Ω
PGOOD Threshold	$V_{\text{PG_TH}}$	VOUTA/B rising		90		%
PGOOD Delay	$V_{\text{PG_DLY}}$	Asserted		2		ms
		PGOODA/B= Low		20		μs
CTL _x Delay	$t_{\text{EN_DLY}}$	From CTL _x Input High to SS starts rising		50		μs
CTL _x Input Current ⁽²⁾	I_{CTLx}	CTL _x =AVINA/B or AGNDA/B	-2.0		2.0	μA
CTL _x Input High Threshold	$V_{\text{CTLx_HI}}$		1.2			V
CTL _x Input Low Threshold	$V_{\text{CTLx_LO}}$				0.4	V
V _{OUTA/B} Over Voltage Protection	V_{OVP}		110	115	120	%
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	$T_{\text{SD_HYS}}$			10		°C

Notes:

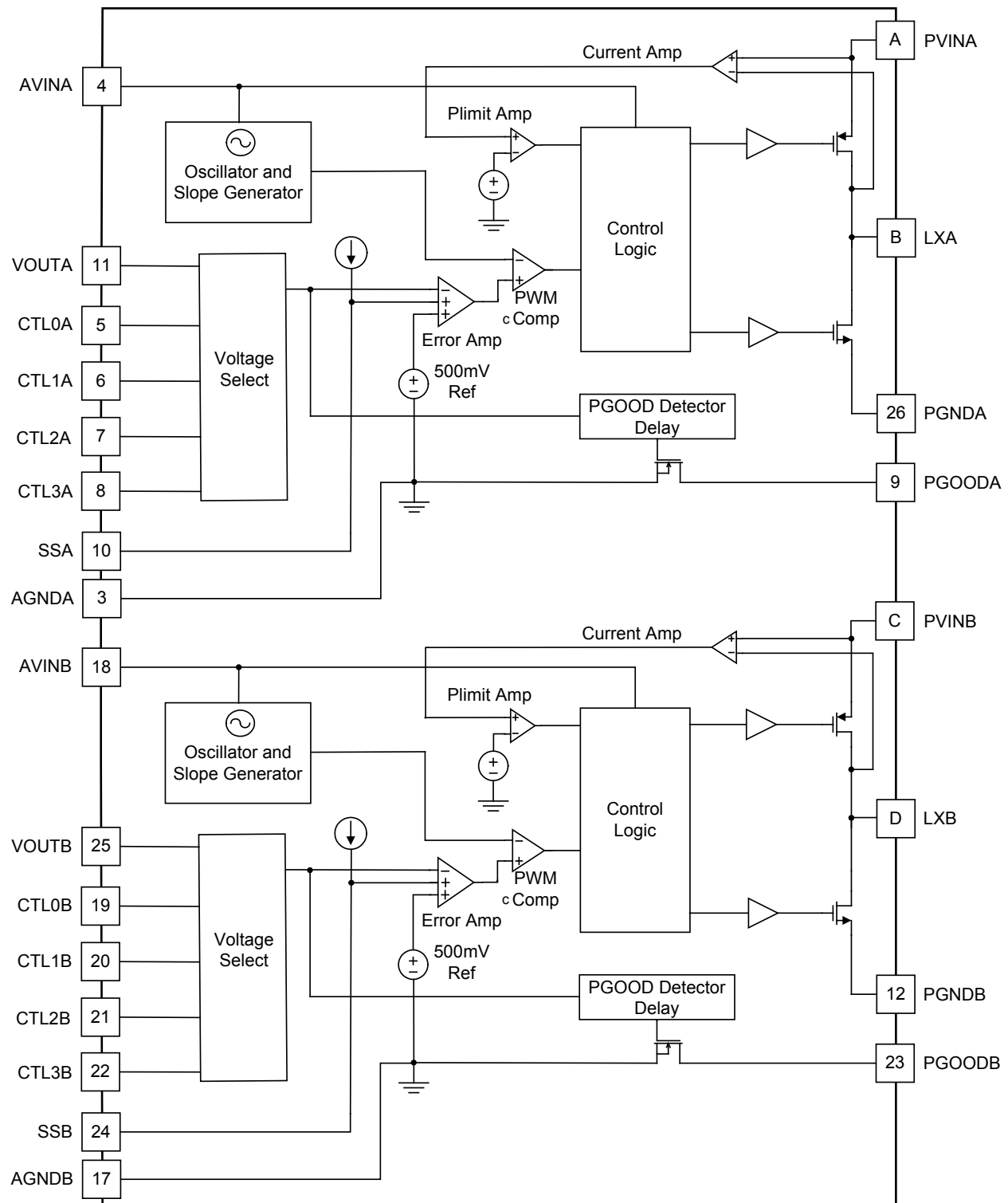
(1) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature and the line regulation.

(2) A negative current means the current flows into the pin and a positive current means the current flows out from the pin.

Pin Descriptions

Pin #	Pin Name	Pin Function
1, 2	PVINA	Input supply voltage for the converter power stage
3	AGNDA	Ground connection for the internal circuitry — AGNDA needs to be connected to PGNDA directly.
4	AVINA	Power supply for the internal circuitry — AVINA is required to be connected to PVINA through an R-C filter of 1Ω and 100nF.
5, 6, 7, 8	CTL _{XA}	Control bit — see Table 1 for decoding. These pins have 500kΩ internal pull-down resistors which are switched into the circuit whenever CTL _{XA} is low or when the part is in under-voltage lockout.
9	PGOODA	Power good indicator — when the output voltage reaches the PGOODA threshold, this pin will be open-drain (after the PGOODA delay), otherwise, it is pulled low internally.
10	SSA	Soft Start — connect a soft-start capacitor to program the soft start time. There is a 5μA charging current flowing out of the pin.
11	VOUTA	Output voltage sense pin
12	PGNDB	Ground connection for converter power stage
13, 14	LXB	Switching node — connect an inductor between this pin and the output capacitor.
15, 16	PVINB	Input supply voltage for the converter power stage
17	AGNDB	Ground connection for the internal circuitry — AGNDB needs to be connected to PGNDB directly.
18	AVINB	Power supply for the internal circuitry — AVINB is required to be connected to PVINB through an R-C filter of 1Ω and 100nF.
19, 20, 21, 22	CTL _{XB}	Control bit — see Table 1 for decoding. These pins have 500kΩ internal pull-down resistors which are switched into the circuit whenever CTL _{XB} is low or when the part is in under-voltage lockout.
23	PGOODB	Power good indicator — when the output voltage reaches the PGOODB threshold, this pin will be open-drain (after the PGOODB delay), otherwise, it is pulled low internally.
24	SSB	Soft Start — connect a soft-start capacitor to program the soft start time. There is a 5μA charging current flowing out of the pin.
25	VOUTB	Output voltage sense pin
26	PGNDA	Ground connection for converter power stage
27, 28	LXA	Switching node — connect an inductor between this pin and the output capacitor.
T	Thermal Pad	Thermal pad for heat sinking purposes — recommend to connect to PGND. It is not connected internally.

Block Diagram



NOTES:

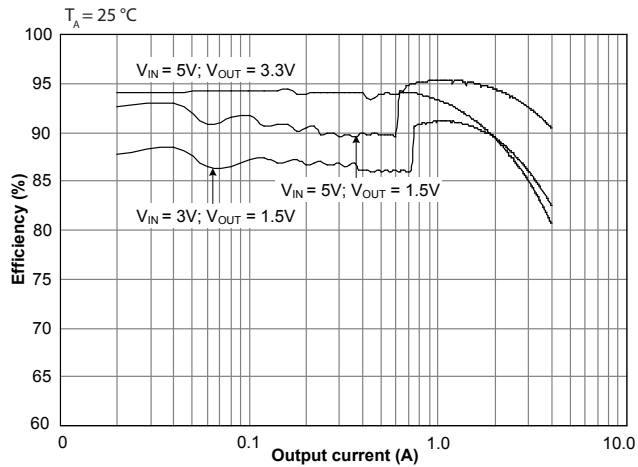
A = Pins 1, 2
B = Pins 27, 28

C = Pins 15, 16
D = Pins 13, 14

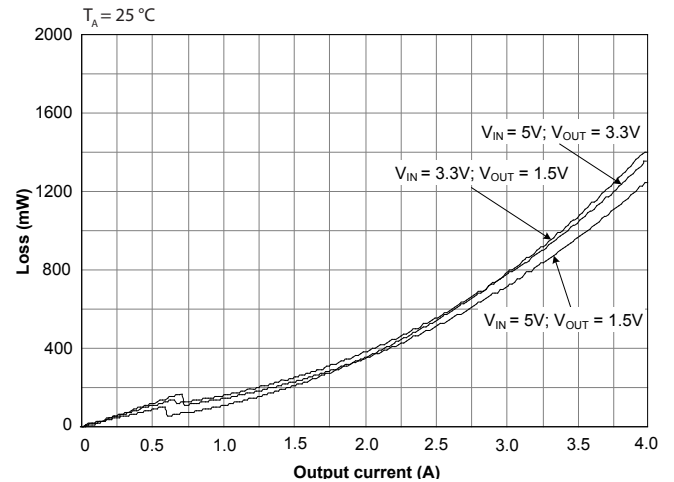
Typical Characteristics

Circuit Conditions: $C_{IN} = 22\mu\text{F}/6.3\text{V}$, $C_{OUT} = 2 \times 22\mu\text{F}/6.3\text{V}$, $C_{SS} = 10\text{nF}$. Unless otherwise noted, $L = 1.0\mu\text{H}$ (TOKO: FDV0530S-1R0), each device

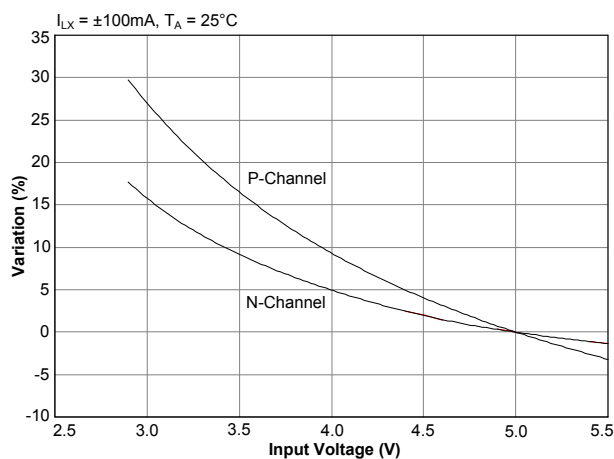
Efficiency



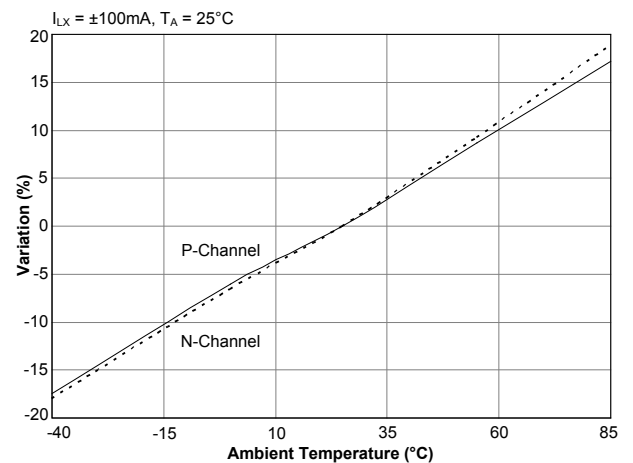
Total Loss



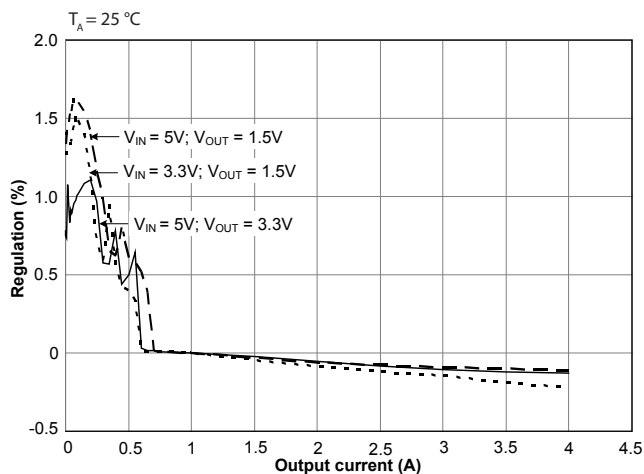
$R_{DS(ON)}$ Variation vs. Input Voltage



$R_{DS(ON)}$ Variation vs. Temperature



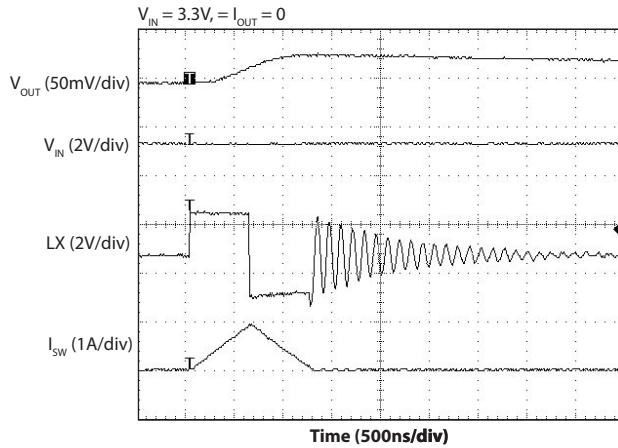
Load Regulation



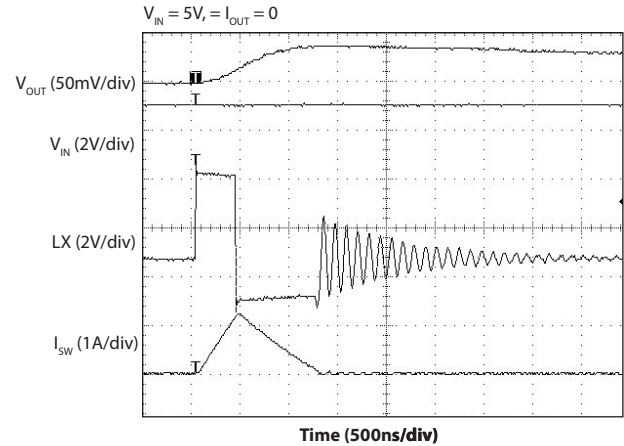
Typical Characteristics (continued)

Circuit Conditions: $C_{IN} = 22\mu\text{F}/6.3\text{V}$, $C_{OUT} = 2 \times 22\mu\text{F}/6.3\text{V}$, $C_{SS} = 10\text{nF}$. Unless otherwise noted, $L = 1.0\mu\text{H}$ (TOKO: FDV0530S-1R0), each device

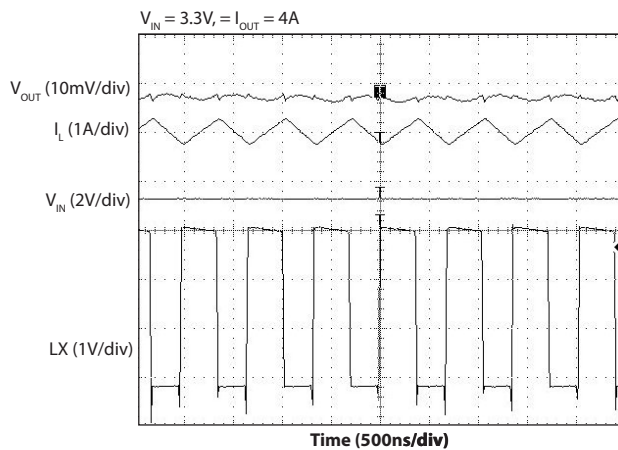
Output Voltage Ripple ($V_{OUT}=1.5\text{V}$)



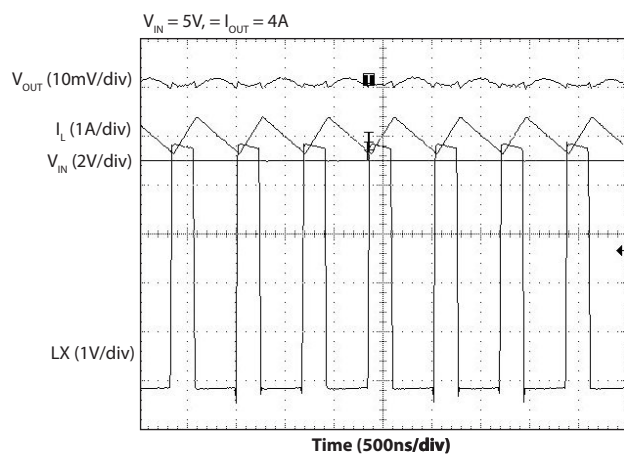
Output Voltage Ripple ($V_{OUT}=1.5\text{V}$)



Output Voltage Ripple ($V_{OUT}=1.5\text{V}$) @ Full Load



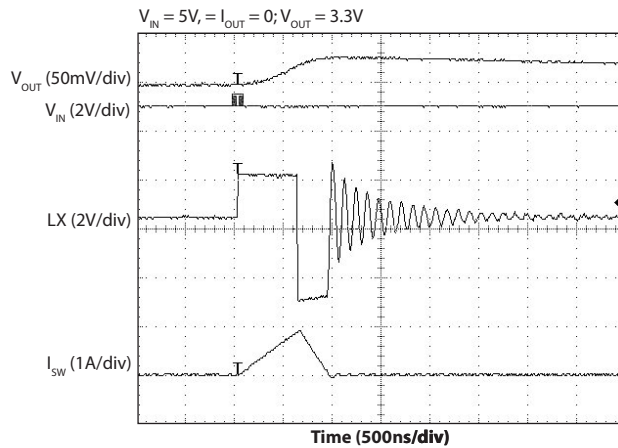
Output Voltage Ripple ($V_{OUT}=1.5\text{V}$) @ Full Load



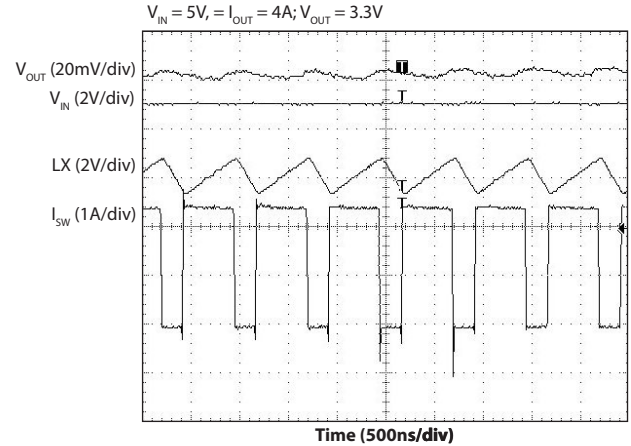
Typical Characteristics (continued)

Circuit Conditions: $C_{IN} = 22\mu\text{F}/6.3\text{V}$, $C_{OUT} = 2 \times 22\mu\text{F}/6.3\text{V}$, $C_{SS} = 10\text{nF}$. Unless otherwise noted, $L = 1.0\mu\text{H}$ (TOKO: FDV0530S-1R0), each device

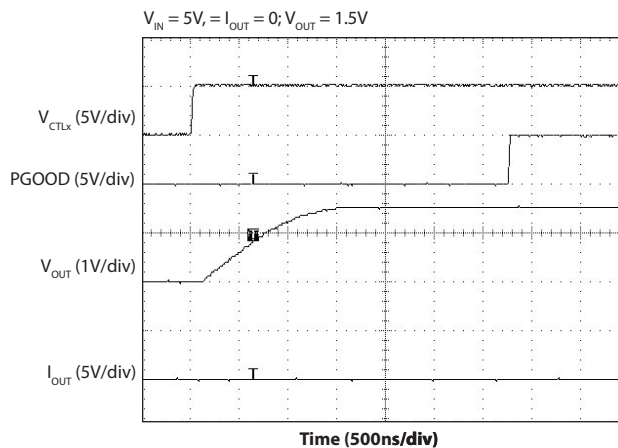
Output Voltage Ripple ($V_{OUT} = 3.3\text{V}$) @ No Load



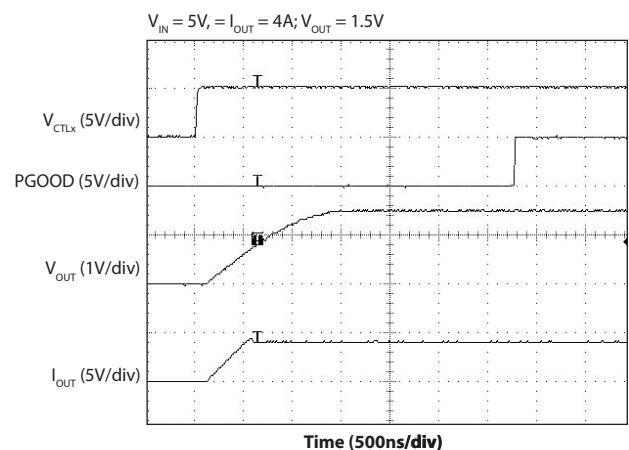
Output Voltage Ripple ($V_{OUT} = 3.3\text{V}$) @ Full Load



Start Up (CTL_X) — No Load



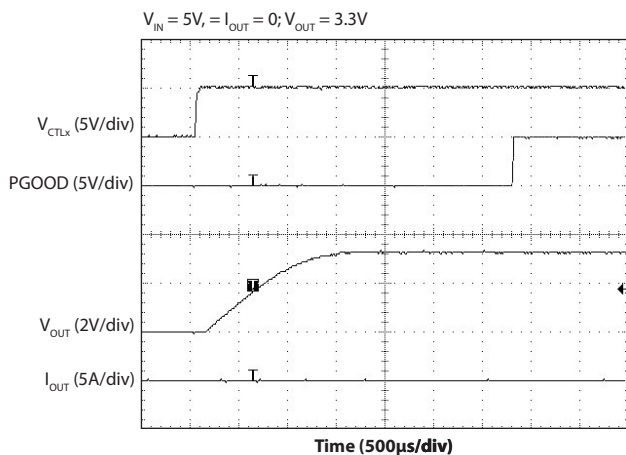
Start Up (CTL_X) — Full Load



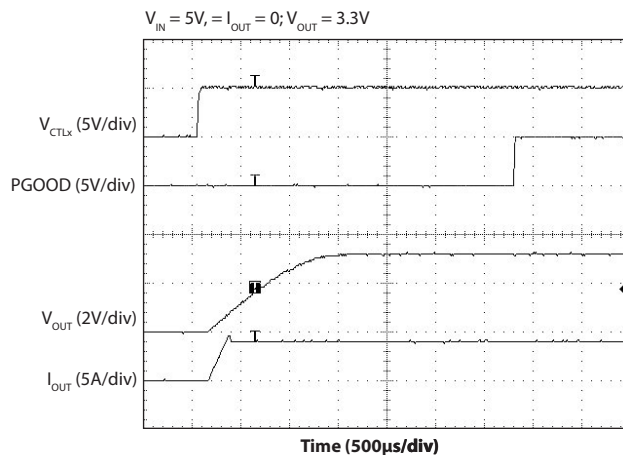
Typical Characteristics (continued)

Circuit Conditions: $C_{IN} = 22\mu\text{F}/6.3\text{V}$, $C_{OUT} = 2 \times 22\mu\text{F}/6.3\text{V}$, $C_{SS} = 10\text{nF}$. Unless otherwise noted, $L = 1.0\mu\text{H}$ (TOKO: FDV0530S-1R0), each device

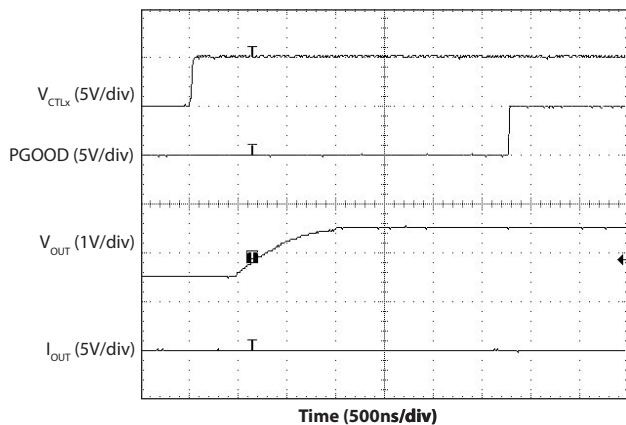
Start Up (CTL_x) — No Load



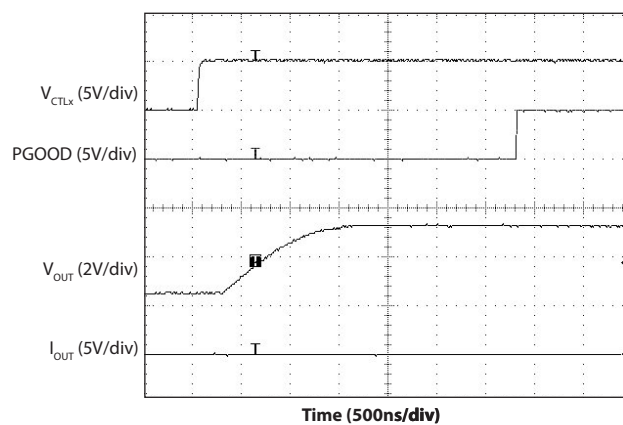
Start Up (CTL_x) — Full Load



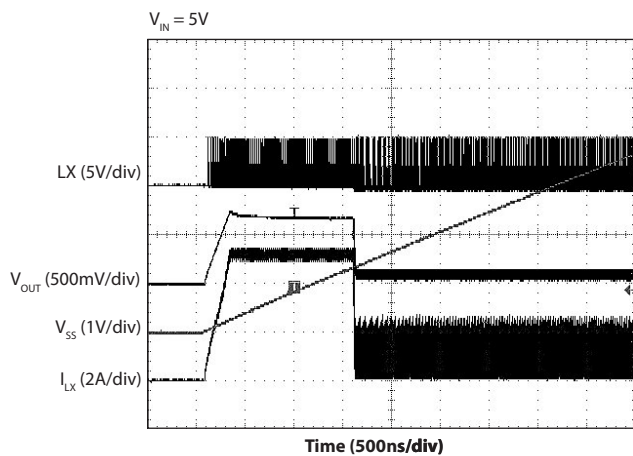
Start Up into Pre-Biased Output ($V_{OUT} = 1.5\text{V}$)



Start Up into Pre-Biased Output ($V_{OUT} = 3.3\text{V}$)



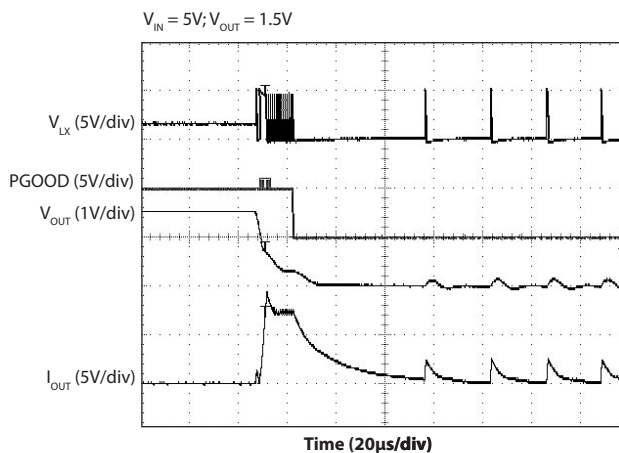
Start Up into Output Short Circuit



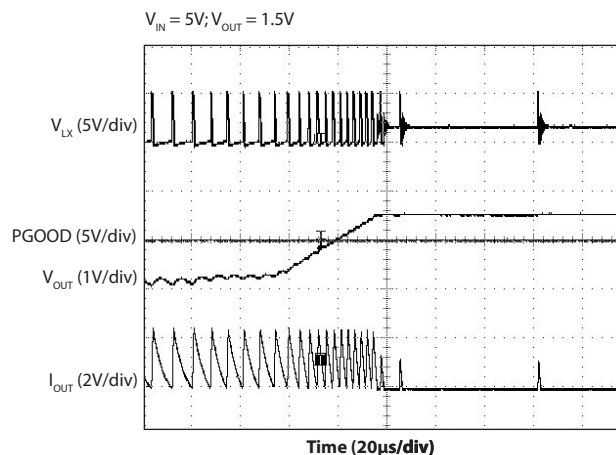
Typical Characteristics (continued)

Circuit Conditions: $C_{IN} = 22\mu F/6.3V$, $C_{OUT} = 2 \times 22\mu F/6.3V$, $C_{SS} = 10nF$. Unless otherwise noted, $L = 1.0\mu H$ (TOKO: FDV0530S-1R0), each device

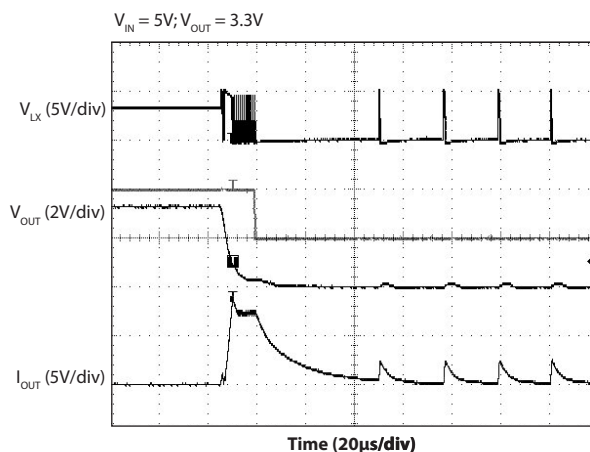
Output Short Circuit



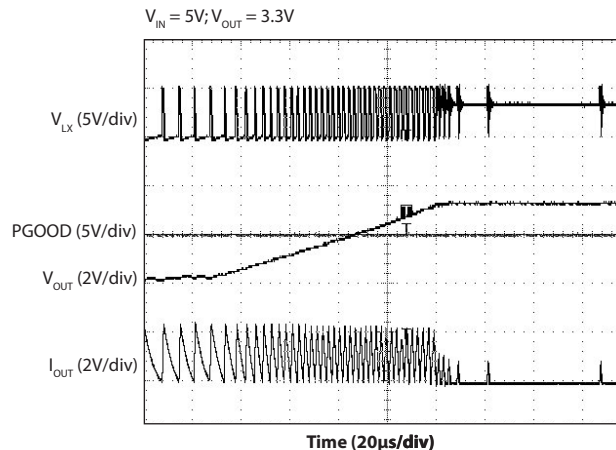
Recovery from Short Circuit



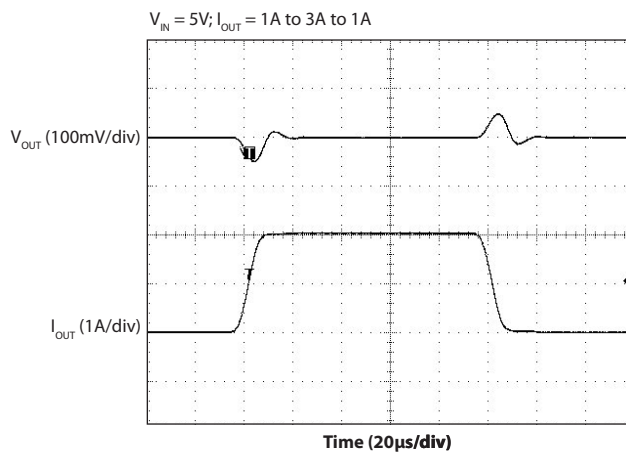
Output Short Circuit



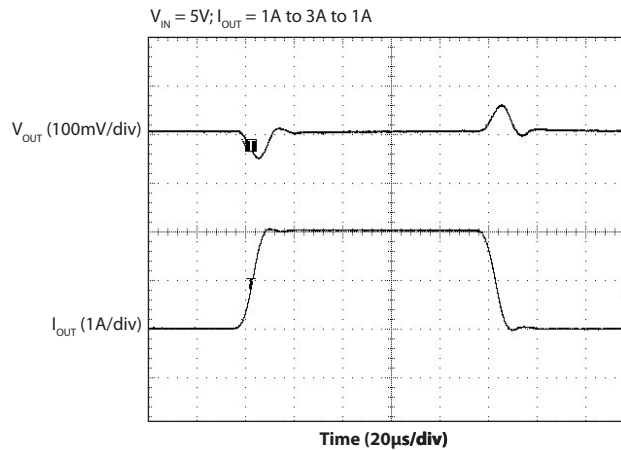
Recovery from Short Circuit



Transient Response ($V_{OUT}=1.5V$, $I_{STEP}=2A$)



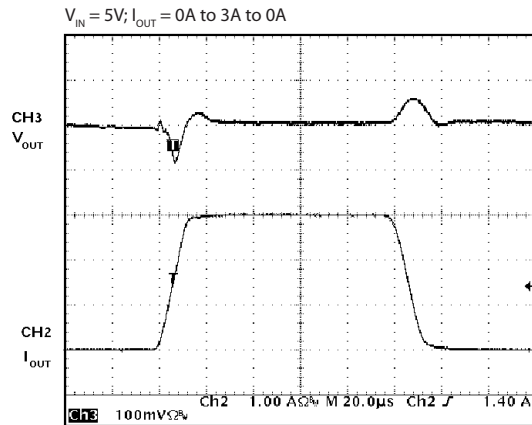
Transient Response ($V_{OUT}=3.3V$, $I_{STEP}=2A$)



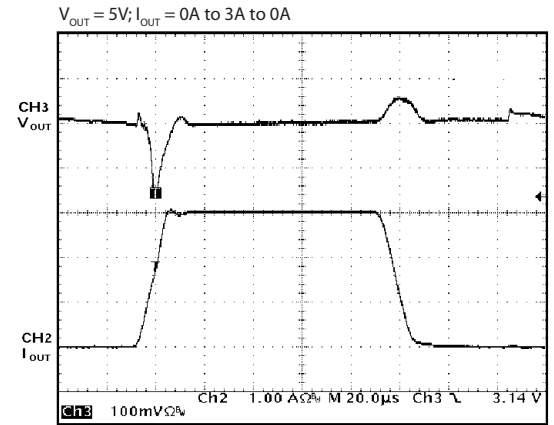
Typical Characteristics (continued)

Circuit Conditions: $C_{IN} = 22\mu\text{F}/6.3\text{V}$, $C_{OUT} = 2 \times 22\mu\text{F}/6.3\text{V}$, $C_{SS} = 10\text{nF}$. Unless otherwise noted, $L = 1.0\mu\text{H}$ (TOKO: FDV0530S-1R0), each device

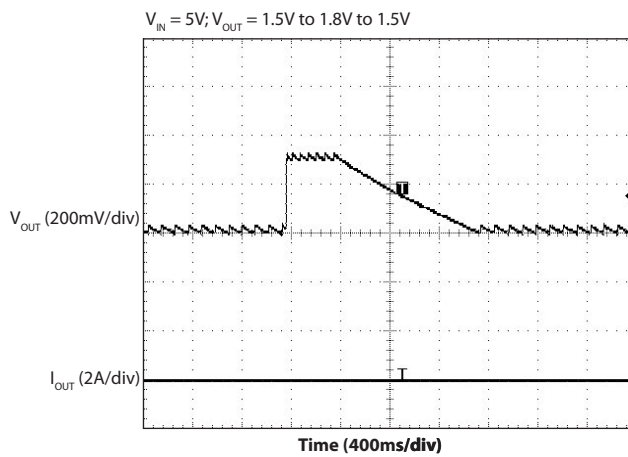
Transient Response ($V_{OUT}=1.5\text{V}$, $I_{STEP}=3\text{A}$)



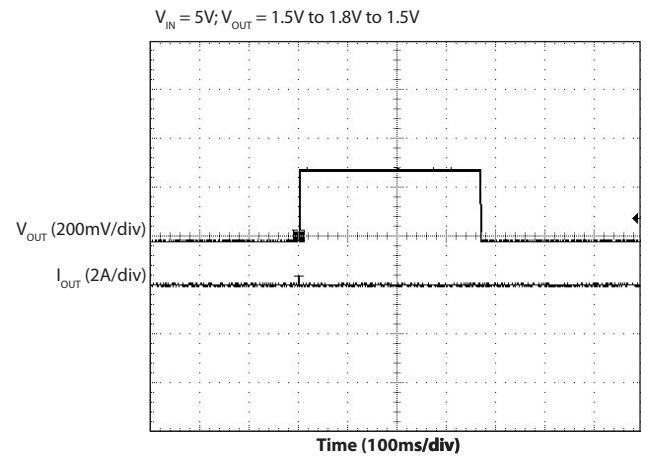
Transient Response ($V_{OUT}=3.3\text{V}$, $I_{STEP}=3\text{A}$)



VID Transition — No Load



VID Transition — Full Load



Applications Information

Detailed Description

The SC286 is a two channel synchronous step-down PWM (Pulse Width Modulated), DC-DC converter utilizing a 1.6MHz fixed-frequency voltage mode architecture. Both channels are designed to operate in fixed-frequency PWM mode and will enter PSAVE (power save) mode at light loads to maximize efficiency. The switching frequency is chosen to minimize the size of the external inductor and capacitors while maintaining high efficiency. Both channels run independently

Operation

During normal operation, the PMOS MOSFET is activated on each rising edge of the internal oscillator. The period is set by the onboard oscillator when in PWM mode. The device has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin. The device operates as a buck converter in PWM mode with a fixed frequency of 1.6MHz at medium to high loads. At light loads the part will enter PSAVE mode to maximize efficiency.

Power Save Mode Operation

When the load current decreases below the PSAVE threshold, PWM switching stops and each channel automatically enters PSAVE mode. This threshold varies depending upon the input voltage and output voltage setting, optimizing efficiency for all possible load currents. While in PSAVE mode, output voltage regulation is controlled by a series of bursts in switching. During a burst, the inductor current is limited to a peak value which controls the on-time of the PMOS switch. After reaching this peak, the PMOS switch is disabled and the inductor current is forced to near 0mA. Switching bursts continue until the output voltage climbs to $V_{OUT} + 2\%$ or until the PSAVE current limit is reached. Switching is then stopped to eliminate switching losses, enhancing overall efficiency. Switching resumes when the output voltage reaches the lower threshold of V_{OUT} and continues until the upper threshold again is reached. Note that the output voltage is regulated hysteretically while in PSAVE mode between V_{OUT} and $V_{OUT} + 2\%$. The period and duty cycle while in PSAVE mode are solely determined by V_{IN} and V_{OUT} until PWM mode resumes. This can result in the switching frequency being much lower than the PWM mode frequency.

If the output load current increases enough to cause V_{OUT} to decrease below the PSAVE exit threshold ($V_{OUT} - 4\%$), the device automatically exits PSAVE and operates in continuous PWM mode. Note that the PSAVE high and low threshold levels are both set at or above V_{OUT} to minimize undershoot when the SC286 exits PSAVE. Figure 1 illustrates the transitions from PWM mode to PSAVE mode and back to PWM mode.

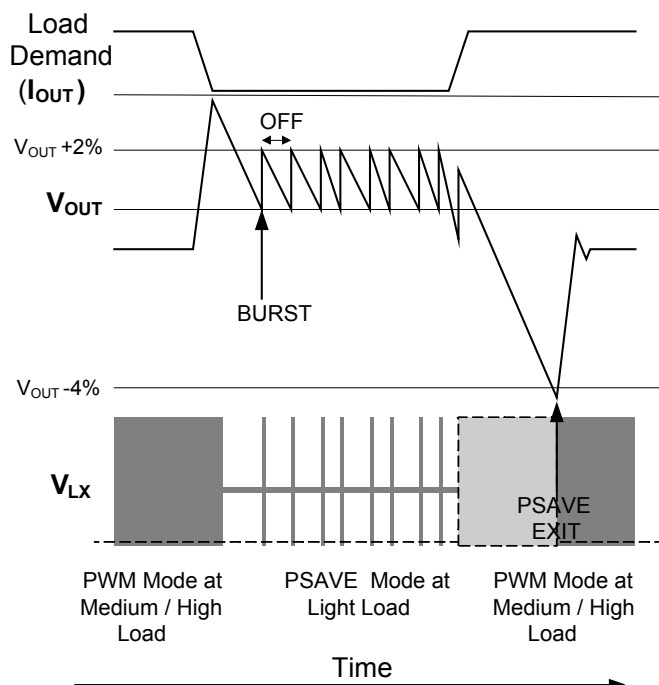


Figure 1 — Transitions between PWM and PSAVE Modes

Protection Features

The SC286 provides the following protection features for each independent channel:

- Current Limit
- Over-Voltage Protection
- Soft-Start Operation
- Thermal Shutdown

Current Limit & OCP

The internal PMOS power device in the switching stage for each channel is protected by a current limit feature. If the inductor current is above the PMOS current limit for 16 consecutive cycles, the part enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) which is approximately 1A.

Applications Information (continued)

Under this condition, the output voltage will be the product of I_{CL_HOLD} and the load resistance. When the load presented falls below the current limit holding level, the output will charge to the upper PSAVE voltage threshold and return to normal operation. The SC286 is capable of sustaining an indefinite short circuit without damage. During soft start, if current limit has occurred before the SS voltage has reached 400mV, the part enters foldback current limit mode. Foldback current limit mode will be disabled during soft-start after the SS voltage is higher than 400mV.

Over-Voltage Protection

In the event of a 15% over-voltage on each independent output, the PWM drive is disabled with the LX pin floating. Switching does not resume until the output voltage falls below the nominal V_{OUT} regulation voltage.

Programmable Output Voltage

The SC286 has fifteen pre-determined output voltage values which can be individually selected for each channel by programming the CTL input pins (see Table 1 — Output Voltage Settings). Each CTL pin has an active 500kΩ internal pull-down resistor. The 500kΩ resistor is switched in circuit whenever the CTL input voltage is below the input threshold, or when the part is in under voltage lockout. It is recommended to tie all high CTL pins together and use an external pull-up resistor to AVIN if there is no enable signal or if the enable input is an open drain/collector signal. The CTL pins may be driven by a microprocessor to allow dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. Avoid all zeros being present on the CTL pins when changing programmable output voltages as this would disable the device.

SC286 is also capable of regulating a different (higher) output voltage, which is not shown in the Table 1, via an external resistor divider for each channel. There will be a typical 2μA current flowing into the VOUTA/B pin. The typical schematic for an adjustable output voltage option from the standard 1.0V with $CTL_{XA/B} = [0010]$, is shown in Figure 2. RFB1A/B and RFB2A/B are used to adjust the desired output voltage. If the RFB2A/B current is such that the 2μA VOUTA/B pin current can be ignored, then RFB1A/B can be found using the next equation. RFB2A/B needs to be low enough in value for the current through the resistor chain to be at least 20μA in order to ignore the VOUTA/B pin current.

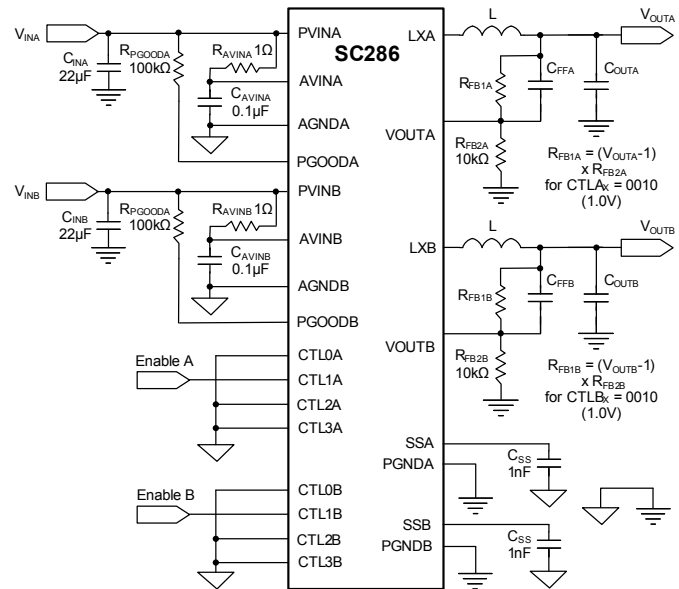


Figure 2 — Output Voltage Programming

$$R_{FB1} = \frac{V_{OUT} - V_{OSTD}}{V_{OSTD}} \times R_{FB2}$$

where V_{OSTD} is the pre-determined output voltage via the CTL pins.

C_{FF} is needed to maintain good transient response performance. The correct value of C_{FF} can be found using the following equation.

$$C_{FF} [nF] = 2.5 \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1} [k\Omega] \times (V_{OUT} - V_{OSTD})} \times \left(\frac{V_{OSTD}}{V_{OSTD} - 0.5} \right)$$

To simplify the design, it is recommended to program the desired output voltage from a standard 1.0V as shown in Figure 2 with a proper C_{FF} calculated from Equation 2. For programming the output voltage from other standard voltages, R_{FB1} , R_{FB2} and C_{FF} need to be adjusted to conform to the previous equations.

Maximum Power Dissipation

Each channel of SC286 has its own Θ_{JA} of 32.5°C/W when only one channel is in operation. Since both channels are within the same package, there is about 50% of the heat generated which will be transferred to the adjacent channel. The equivalent total thermal impedance will be higher when the neighboring channel is also in operation.

Applications Information (continued)

To guarantee an operating junction temperature of less than 125°C, Figure 3 shows the maximum allowable total power loss versus temperature. The curve is based upon the junction temperature of either channel reaching a maximum of 125°C. Each channel of SC286 can support up to 4A load current. Figure 4 shows the maximum allowable power loss in channel B versus power loss in channel A for a range of temperatures.

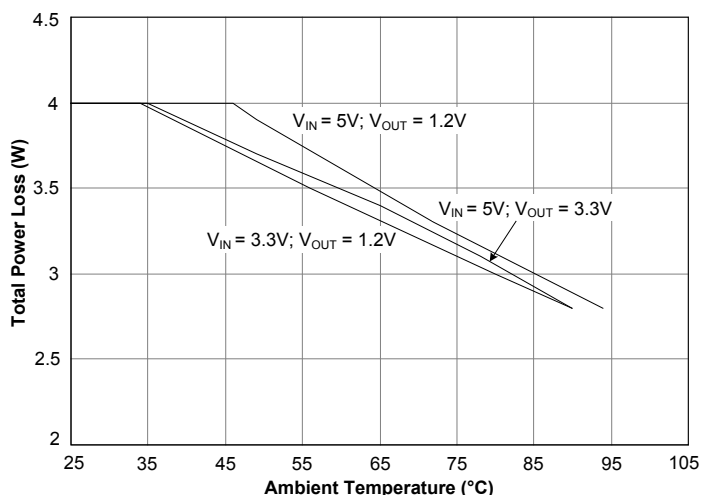


Figure 3 — Maximum allowable total loss versus temperature for a maximum junction temperature of 125°C

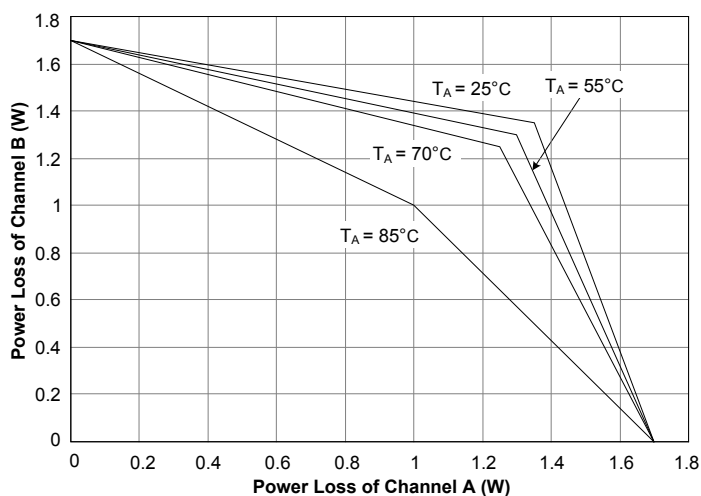


Figure 4 — Maximum allowable power loss in channel B versus power loss in channel A for a range of temperatures (both channels same current)

Shut Down

When all CTL pins for a channel are low, the device will run in shutdown mode, drawing less than 1 μA from the input power supply. The internal switches and band-gap voltage will be immediately turned off.

Thermal Shutdown

The device has an independent thermal shutdown feature for each channel to protect the SC286 if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled, floating the LX output. When the temperature drops by 10°C, it will initiate a soft start cycle to resume normal operation.

Under-Voltage Lockout

Under-Voltage Lockout (UVLO) is enabled when the input voltage for each channel drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 300mV is included to prevent chattering near the threshold. When the AVIN voltage rises back to the turn-on threshold and CTL_x is high, the soft-start mode is initiated.

Power Good

The power good (PGOOD) for each channel is an open-drain output. When the output voltage for each channel drops below 10% of the nominal voltage, the PGOOD pin for that channel is pulled low after a 20 μs delay. During start-up, PGOOD will be asserted 1.8ms (typ.) after the output voltage reaches 90% of the final regulation voltage. The faults of over voltage, fold-back current limit mode and thermal shutdown will force PGOOD low after a 20 μs delay. When recovering from a fault, PGOOD will be asserted 2ms (typ.) after Vout reaches 90% of the final regulation voltage.

Applications Information (continued)

Soft-Start

The soft-start mode is activated for each channel after AVIN reaches its UVLO voltage threshold and $CTL_{XA/B}$ is set high to enable the part. Recovery from a thermal shut-down event will also activate the soft start sequence. The soft-start mode controls the slew-rate of the output voltage during start-up thus limiting in-rush current on the input supply. During start-up, the reference voltage for the error amplifier is clamped by the voltage on SS pin. The output voltage slew rate during soft-start is determined by the value of the external capacitor connected to the SS pin and the internal 5μA charging current. The device requires a minimum soft-start time from enable to final regulation in the order of 200μs, including the 50μs enable delay. As a result the soft start capacitor, C_{ss} , should be higher than 1.5nF. During start up, the chip operates in forced PWM mode.

100% Duty-Cycle Operation

SC286 is capable of operating at 100% duty-cycle. When the difference between the input voltage and output voltage is less than the minimum dropout voltage, the PMOS switch is turned completely on, operating in 100% duty-cycle. The minimum dropout voltage is the output current multiplied by the on-resistance of the internal PMOS switch and the DC-resistance of the inductor when the PMOS switch is on continuously.

Output L-C filter Selection

SC286 has fixed internal loop-gain compensation for each channel. It is optimized for X5R or X7R ceramic output capacitors and an output L-C filter corner frequency of less than 34kHz. The output L-C corner frequency can be determined by the following equation.

$$f_c = \frac{1}{2\pi \sqrt{L \times C_{OUT}}}$$

In general, the inductor is chosen to set the inductor ripple current to approximately 30% of the maximum output current. It is recommended to use a typical inductor value of 1μH to 2.2μH with output ceramic capacitors of 44μF or higher capacitance. Lower inductance should be considered in applications where faster transient response is required. More output capacitance will reduce the output deviation for a particular load transient. When using low inductance, the maximum peak inductor current at any condition (normal operation and start up) can not exceed 5A which is the guaranteed minimum current limit. The saturation current rating of the inductor needs to be at least larger than the peak inductor current which is the maximum output current plus half of inductor ripple current.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 5 shows a recommended top-layer PCB for the SC286 and supporting components. Figure 6 shows the bottom layer for this PCB. Fundamental layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN} (for applicable channel) should be placed within 1mm of the PVIN and PGND pins. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L (for applicable channel) should be connected as close as possible between the LX and PGND pins, with a direct return to the PGND pin from C_{OUT} . The gap between the LX trace and the other traces should be at least 0.25mm (10 mils).
3. Route the output voltage feedback/sense path away from the inductor and LX node to minimize noise and magnetic interference.
4. Use a ground plane referenced to the SC286 PGND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the VOUT and PGND pins to the load (for applicable channel). This will reduce the voltage drop on the ground plane and improve the load regulation. And it will also improve the overall efficiency by reducing the copper losses on the output and ground planes.
6. The filter capacitor, C_{AVIN} , should be placed as close to the AVIN and AGND pins as possible. This reduces noise coupling into the internal circuit.

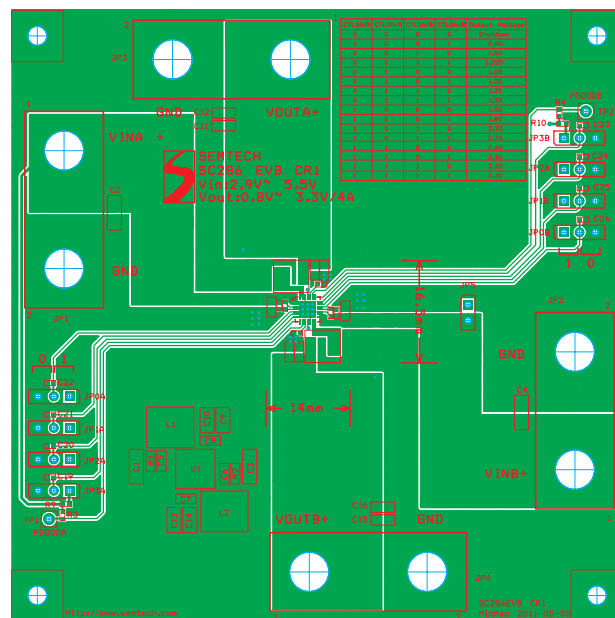


Figure 5 — Recommended PCB Layout (Top Layer)

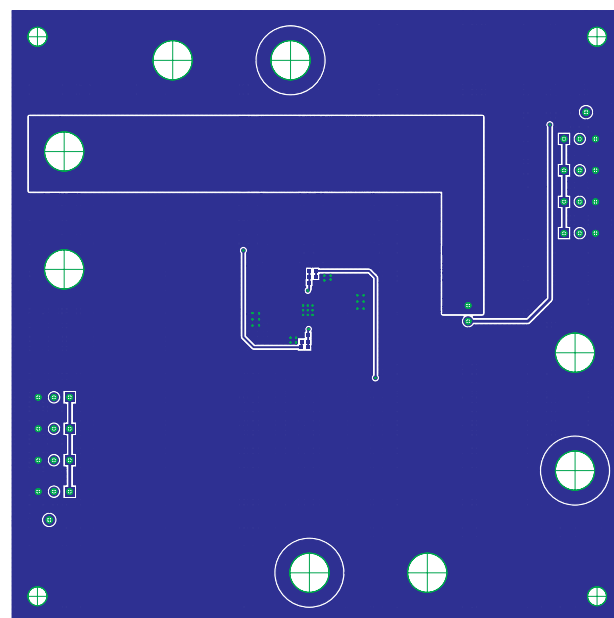
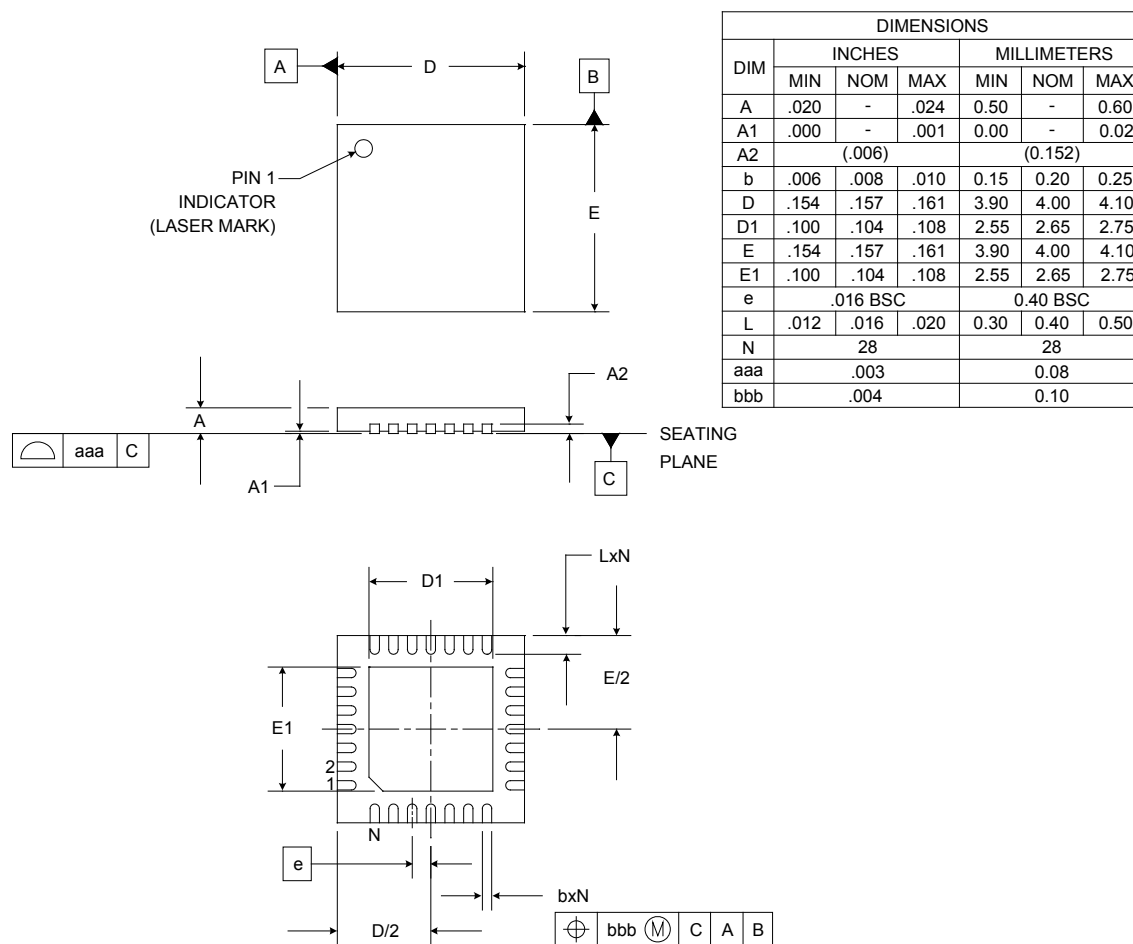


Figure 6 — Recommended PCB Layout (Bottom Layer)

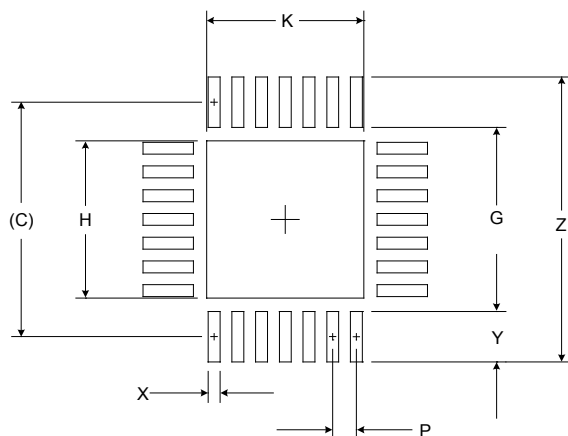
Outline Drawing – 4x4 MLPQ-UT28



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern – 4x4 MLPQ-UT28



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.104	2.65
K	.104	2.65
P	.016	0.40
X	.008	0.20
Y	.033	0.85
Z	.189	4.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

© Semtech 2011

All rights reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights. Semtech assumes no responsibility or liability whatsoever for any failure or unexpected operation resulting from misuse, neglect improper installation, repair or improper handling or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified range.

SEMTECH PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF SEMTECH PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE UNDERTAKEN SOLELY AT THE CUSTOMER'S OWN RISK. Should a customer purchase or use Semtech products for any such unauthorized application, the customer shall indemnify and hold Semtech and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs damages and attorney fees which could arise.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com