

DS26502DK T1/E1/J1/64KCC Bits Element Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26502DK is an easy-to-use evaluation board for the DS26502 T1/E1/J1/64KCC BITS element. The DS26502DK is intended to be used as a stand-alone design kit. The board is complete with a DS26502 BITS element, transformers, termination resistors, FPGA-based configuration switches, and network connectors. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status as well as multiple clock and signal routing configurations.

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DESIGN KIT CONTENTS

DS26502DK Design Kit
CD_ROM Including:

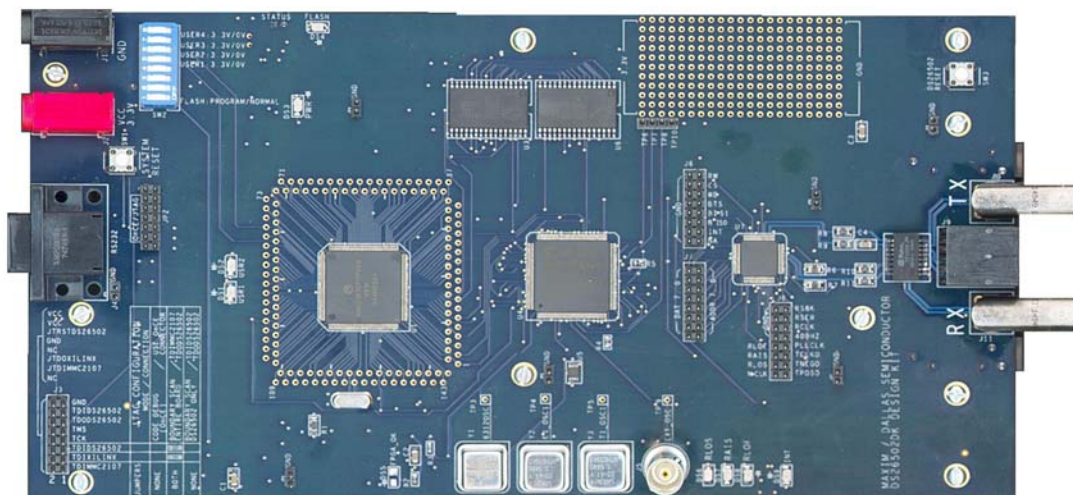
- ChipView Software
- DS26502DK Data Sheet
- DS26502 Data Sheet
- DS26502 Errata Sheet (if applicable)

ORDERING INFORMATION

PART	DESCRIPTION
DS26502DK	Stand-Alone Design Kit for DS26502

FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Demonstrates Key Functions of DS26502 BITS Element
- Includes DS26502 BITS Element, Transformers, BNC, and RJ48 Network Connectors and Termination Passives
- BNC Connections for 75Ω E1
- Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1
- Interface Directly to Windows-Based Computers
- ChipView Software Provides Point-and-Click Access to the DS26502 Register Set
- Software Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-of-Signal and Interrupt Status as well as Indications for Multiple Clock and Signal Routing Configurations
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

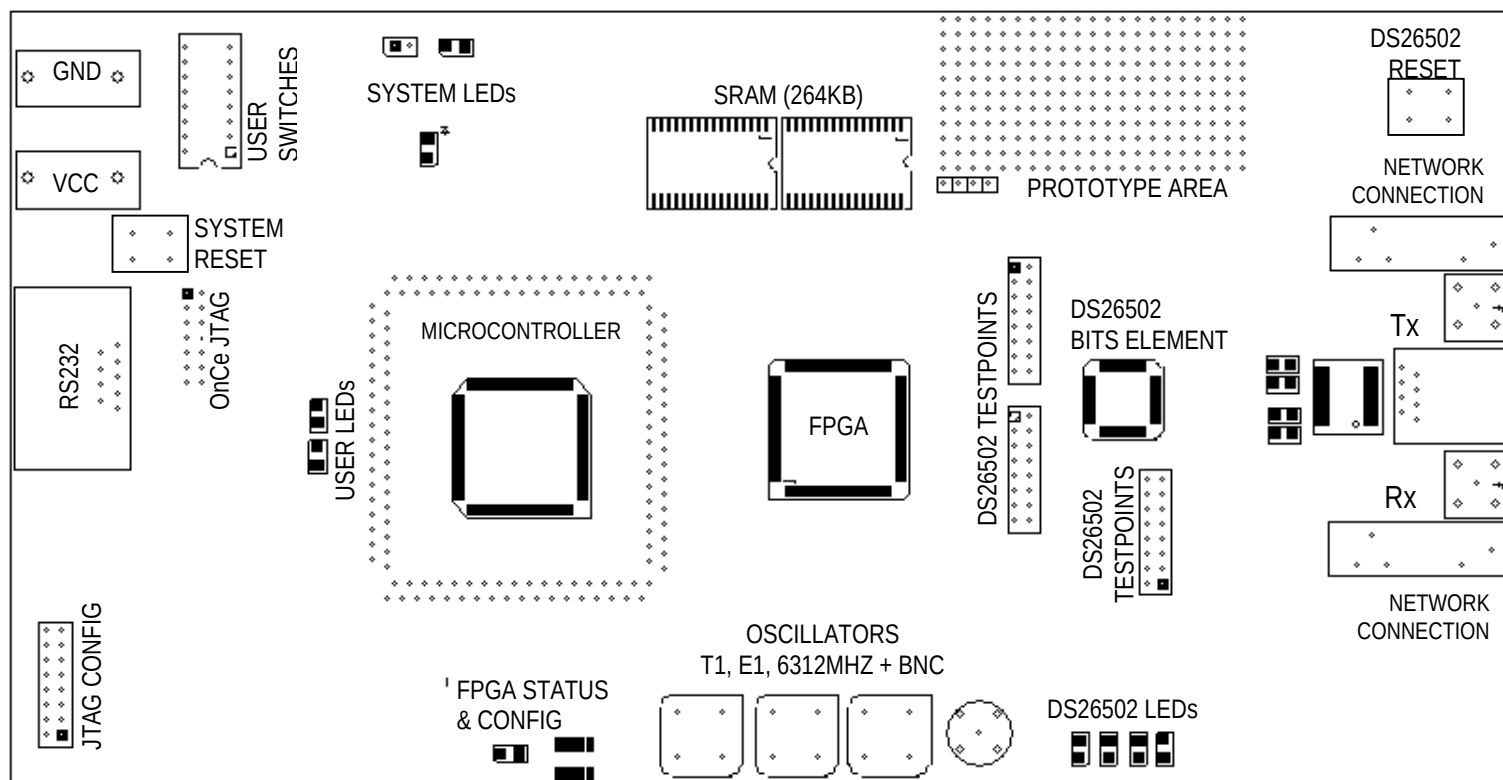


COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C4, C23, C51, C53	5	10 μ F 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
C2–C3, C6–C9, C11, C12, C14, C15, C17, C18, C20, C21, C25–C30, C32, C33, C35, C36, C38, C45–C50, C52, C54, C55, C57–C60, C62, C63, C68	41	1 μ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C5, C10, C22, C24, C31, C34, C37, C39–C41, C43, C65–C67, C69, C70	16	0.1 μ F 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C13, C19, C42, C44, C64	5	10 μ F 20%, 16V tantalum capacitors (B case)	Panasonic	ECS-T1CX106R
C16, C56, C61	3	68 μ F 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
D1	1	1A 50V general-purpose silicon diode	General Semiconductor	1N4001
DS1, DS2, DS6–DS9	6	LED, RED, SMD	Panasonic	LN1251C
DS3	1	LED, GREEN, SMD	Panasonic	LN1351C
DS4	1	LED, AMBER, SMD	Panasonic	LN1451C
DS5	1	LED, GREEN, SMD (Not populated)	Panasonic	LN1351C
DS10	1	LED red/green, 5mm red/green right-angle PCMT	Digi-Key	350-1055-ND
J1	1	Socket, banana plug, horizontal, black	Mouser Electronics	164-6218
J2	1	Socket, banana plug, horizontal, red	Mouser Electronics	164-6219
J3, J6–J8	4	Terminal strip, 16-pin, dual row, vertical	Samtec	TSW-108-07-T-D
J4	1	DB9 right-angle, long case connector	AMP	747459-1
J5	1	L_CONNECTOR BNC 75 Ω vertical 5-pin	Cambridge	CP-BNCP-004
J9	1	L_RJ48 8-pin, single-port connector	MOLEX	15-43-8588
J10, J11	2	BNC connectors, 75 Ω right-angle 5-pin	Kruid	UCBJR220
J12, J13	2	L_CONN, Bantam jack, right-angle	Switchcraft	RTT34B02
JP1, JP3–JP8	7	100-mil, 2 position jumper	labstock	
JP2	1	14-pin header, remove 'missing pin'	labstock	
L1	1	Inductor, 22.0 μ H 2-pin SMT 20%	Coiltronics	UP1B-220
NP1, NP2	2	10pF 5%, 50V tall case ceramic capacitors (1206) Do not populate	Phycomp	1206CG100J9B200
R1, R8–R11	5	0 Ω 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R2, R13, R23, R27, R43, R47, R67–R70	10	330 Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R3, R18–R20, R22, R25, R26, R28–R31, R33–R42, R44–R46, R49, R50, R53, R56, R59, R61, R62, R65, R72	33	10k Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R4, R5, R48, R51, R54, R55, R57, R58	8	30 Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ300V
R6, R7	2	61.9 Ω 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF61R9V
R12	1	51 Ω 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ510V
R14–R17, R21, R24, R63, R64, R66, R71	10	1.0k Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
R32	1	1.0k Ω 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ102V
R52	1	51.1 Ω 1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF51R1V
R60	1	1.0M Ω 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
SW1, SW3	2	Switch MOM 4-pin single pole	Panasonic	EVQPAE04M
SW2	1	Switch 8-position, 16-pin DIP, low profile	AMP	435668-7
T1	1	XFMR 16P SMT	Pulse	TX1099
TP1, TP2	2	Testpoint, 1 plate thru-hole	NA	NA
TP3–TP10	8	Testpoint, 1 plated hole DO NOT STUFF	NA	NA
U1	1	32-bit microcontroller (lab stock)	Avnet	MMC2107CFCV33
U3, U6	2	SRAM 5V, 1Mb SO (in lab stock)	Cypress	CY62128V
U4	1	Xilinx Spartan 2.5V FPGA, 20mm x 20mm 144-pin TQFP	Xilinx	XC2S50-5TQ144C
U5	1	8-Pin μ MAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U7	1	64-pin LQFP T1/E1/J1 BITS element (0°C to +70°C)	Dallas Semiconductor	DS26502L
U8, U9, U13	3	High-speed inverter	Fairchild	NC7SZ86
U10	1	High-speed buffer	Fairchild	NC7SZ86
U11	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	Maxim	MAX3233E
U12	1	1Mb flash-based config mem	Xilinx	XCF01SV020C
U14	1	8-pin SO step-up DC-DC converter 0.5A limit	Maxim	MAX1675EUA
X1	1	Low-profile 8.0MHz crystal	PEI	EC1-8.000M
Y1	1	Oscillator, crystal clock, 3.3V, 6.312MHz	SaRonix	NTH069A3-6.312
Y2	1	Oscillator, crystal clock, 3.3V, 2.048MHz	SaRonix	NTH039A3-2.0480
Y3	1	Oscillator, crystal clock, 3.3V, 1.544MHz	SaRonix	NTH039A3-1.5440

BOARD FLOORPLAN



ERRATA

The design kit errata refer to two difference PC board revisions: the DS26502DK01A0 and DS26502DK01B0. The PC board revision code is found on the bottom of the board in the lower right corner.

DS26502DK01A0 Circuit Boards

- RCLK did not get connected to FPGA. A jumper wire was run from RCLK to TP10 to provide the connection.
- Silkscreen for J3.4 is incorrect. Silkscreen reads "JTDIMMC2107" and should read "JTDOMMC2107."
- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.
- DC blocking capacitor C4 on TTIP too small. A 10 μ F capacitor is recommended; a 1 μ F capacitor was populated.

DS26502DK01B0 Circuit Boards

- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.

ADDITIONS

The following signals have been connected to Testpoints via the FPGA:

- TP6 is driven with data present at the TS_8K_4 pin of the DS26502.
- TP7 is driven with the 400Hz signal mentioned in the TS_8Ksrc register (page 15).
- TP8 is driven with the 8KHz signal mentioned in the TS_8Ksrc register (page 15).

BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/telecom. See the DS26502DK QuickView data sheet for these files.

Hardware Configuration

- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V.
- DIP switches are unused and can be in either the ON or OFF position with exception for the Flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

General

- Upon power-up the RLOS and RLOF LEDs (red) will be lit, the INT LED (red) will not be lit, and Status LED (DS10 red/green bicolor) will be green.

Quick Setup (Register View)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program will then request a definition file. Select DS26502DC_FPGA.def. Through the 'links' section, this will also load DS26502.def.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS26502.
- Predefined Register settings for several functions are available as initialization files.
 - ini files are loaded by selecting the menu File→Reg ini File→Load ini File.
 - Load the ini file "CompositeClock.ini."
 - Load the ini file "DS26502FPGA_2048Clks.ini," which sets the DS26502 in Intel nonmultiplexed mode with MCLK driven at 2.048MHz.
 - After loading the ini files the following may be observed:
 - The RLOS and RLOF LEDs extinguishes upon external loopback.
 - The part begins operating in composite clock mode.

Miscellaneous

- Clock frequencies and certain pin bias levels are provided by a register-mapped FPGA.
- The definition file for this FPGA is named DS26502DC_FPGA.def. The FPGA register definitions are located on page 6. A drop-down menu on the top of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the section marked "BASIC OPERATION."

ADDRESS MAP

Device address space (DS26502 and FPGA) begins at 0x81000000.

All offsets given below are relative to the beginning of the device address space (shown above).

Table 1. Device Address Map

OFFSET	DEVICE	DESCRIPTION
0x0000 to 0x0030	FPGA	Board identification and clock/signal routing
0x8000 to 0x80ff	DS26502 T1/E1/J1 BITS element	DS26502 T1/E1/J1 BITS element

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named “DS26502DC_FPGA.def”.

FPGA Register Map

Table 2. FPGA Register Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x0000	BID	Read only	BOARD ID
0x0001	Unused	—	—
0x0002	XBIDH	Read only	HIGH NIBBLE EXTENDED BOARD ID
0x0003	XBIDM	Read only	MIDDLE NIBBLE EXTENDED BOARD ID
0x0004	XBIDL	Read only	LOW NIBBLE EXTENDED BOARD ID
0x0005	BREV	Read only	BOARD FAB REVISION
0x0006	AREV	Read only	BOARD ASSEMBLY REVISION
0x0007	PREV	Read only	PLD REVISION
0x0007	BUSMO	Read only	BUS MODE INFORMATION
0x09-0x10	Unused	—	—
0x0011	LEVEL1	Control	DS26502 pin settings (THZE, BTS–HBE, BIS1, BIS0)
0x0012	LEVEL2	Control	DS26502 pin settings (RMODE3, RMODE2, RMODE1, RMODE0)
0x0013	LEVEL3	Control	DS26502 pin settings (RSM, RITD)
0x0014	LEVEL4	Control	DS26502 pin settings (TSM, TITD)
0x0015	LEVEL5	Control	DS26502 pin settings (TCSS1, TCSS0)
0x0016	LEVEL6	Control	DS26502 pin settings (TMODE3, TMODE2, TMODE1, TMODE0)
0x0017	LEVEL7	Control	DS26502 pin settings (L2, L1, L0)
0x0018	LEVEL8	Control	DS26502 pin settings (TAIS, RLB)
0x0019	LEVEL9	Control	DS26502 pin settings (MPS1, MPS0)
0x001A	LEVEL10	Control	DS26502 pin settings (JAMUX, E1TS)
0x001B	Unused	—	—
0x001C	TSERsrc	Control	DS26502 TSER source selection
0x001D	MCLKsrc	Control	DS26502 MCLK source selection
0x001E	TCLK	Control	DS26502 TCLK source selection
0x001F	TS_8K	Control	DS26502 TS_8K source selection
0x0020	Unused	—	—
0x0021	Unused	—	—

FPGA ID Registers

BID: BOARD ID (Offset = 0x0000)

BID is read only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0x0002)

XBIDH is read only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0x0003)

XBIDM is read only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0x0004)

XBIDL is read only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0x0005).

BREV is read only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0x0006)

AREV is read only and displays the current assembly revision.

PREV: PLD REVISION (Offset = 0x0007)

PREV is read only and displays the current PLD firmware revision.

FPGA Status Registers

Register Name: **BUSMO**

Register Description: **DS26502 Bus Mode**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	LevCPOL	LevCPHA	HW	SPI	INMUX	IMUX	MNMUX	MMUX
Default	—	—	—	—	—	—	—	—

The FPGA derives values in the BUSMO register from the levels present at the DS26502 pins.

Bit 7: LevCPOL. When set the DS26502 CPOL pin is high. Note: This pin is called A3/CPOL/L1 in parallel/serial/hardware modes.

Bit 6: LevCPHA. When set the DS26502 CPHA pin is high. Note: This pin is called A2/CPHA/L0 in parallel/serial/hardware modes.

Bit 5: HW. When set the DS26502 is in hardware mode.

Bit 4: SPI. When set the DS26502 is in SPI (3-wire) mode.

Bit 3: INMUX. When set the DS26502 is in Intel nonmultiplexed mode.

Bit 2: IMUX. When set the DS26502 is in Intel multiplexed mode.

Bit 1: MNMUX. When set the DS26502 is in Motorola nonmultiplexed mode.

Bit 0: MMUX. When set the DS26502 is in Motorola multiplexed mode.

FPGA Control Registers

The FPGA register set consists of two types of registers: level setting and clock multiplexing. There are 10 registers for tri-state and level-control setting when in hardware mode. The level-setting registers are only valid when the DS26502 is in hardware mode (BIS1:0 = 11). When in nonhardware mode, the FPGA pins affected by the level registers are automatically either tri-stated, or assume an alternate function (e.g., they function as address databus pins or SPI pins). Exceptions are given with the register descriptions.

Register Name: **LEVEL1**

Register Description: **DS26502 Pin Settings (THZE, BTS, BIS1, BIS0)**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	THZEtri	THZE_Lev	BTStri	BTS_Lev	BIS1tri	BIS1_Lev	BIS0tri	BIS0_Lev
Default	0	0	0	0	0	0	0	1

Note: This register is only valid in ALL modes (many of the level registers are only valid in hardware mode).

Bits 7 and 6: DS26502 THZE Tri-State and Level (THZEtri and THZE_Lev)

- 00 = FPGA drives THZE with 0V
- 01 = FPGA drives THZE with 3.3V
- 1x = FPGA tri-states THZE pin

Bit 5 and 4: DS26502 BTS Tri-State and Level (BTStri and BTS_Lev)

- 00 = FPGA drives BTS with 0V
- 01 = FPGA drives BTS with 3.3V
- 1x = FPGA tri-states BTS pin

Bits 3 and 2: DS26502 BIS1 Tri-State and Level (BIS1tri and BIS1_Lev)

- 00 = FPGA drives BIS1 with 0V
- 01 = FPGA drives BIS1 with 3.3V
- 1x = FPGA tri-states BIS1 pin

Bits 1 and 0: DS26502 BIS0 Tri-State and Level (BIS0tri and BIS0_Lev)

- 00 = FPGA drives BIS0 with 0V
- 01 = FPGA drives BIS0 with 3.3V
- 1x = FPGA tri-states BIS0 pin

Register Name: **LEVEL2**

Register Description: **DS26502 Pin Settings (RMODE3, RMODE2, RMODE1, RMODE0)**

Register Offset: **0x0012**

Bit #	7	6	5	4	3	2	1	0
Name	RMODE3 tri	RMODE3 _Lev	RMODE2 tri	RMODE2 _Lev	RMODE1 tri	RMODE1 _Lev	RMODE0 tri	RMODE0 _Lev
Default	0	0	0	0	0	0	0	0

Note: This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

Bits 7 and 6: DS26502 RMODE3 Tri-State and Level (RMODE3tri and RMODE3_Lev)

00 = FPGA drives RMODE3 with 0V
 01 = FPGA drives RMODE3 with 3.3V
 1x = FPGA tri-states RMODE3 pin

Bits 5 and 4: DS26502 RMODE2 Tri-State and Level (RMODE2tri and RMODE2_Lev)

00 = FPGA drives RMODE2 with 0V
 01 = FPGA drives RMODE2 with 3.3V
 1x = FPGA tri-states RMODE2 pin

Bits 3 and 2: DS26502 RMODE1 Tri-State and Level (RMODE1tri and RMODE1_Lev)

00 = FPGA drives RMODE1 with 0V
 01 = FPGA drives RMODE1 with 3.3V
 1x = FPGA tri-states RMODE1 pin

Bits 1 and 0: DS26502 RMODE0 Tri-State and Level (RMODE0tri and RMODE0_Lev)

00 = FPGA drives RMODE0 with 0V
 01 = FPGA drives RMODE0 with 3.3V
 1x = FPGA tri-states RMODE0 pin

Register Name: **LEVEL3**

Register Description: **DS26502 Pin Settings (RSM, RITD)**

Register Offset: **0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RSMtri	RSM_Lev	—	—	RITDtri	RITD_Lev
Default	0	0	0	0	0	0	0	0

Note: This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

Bits 5 and 4: DS26502 RSM Tri-State and Level (RSMtri and RSM_Lev)

00 = FPGA drives RSM with 0V
 01 = FPGA drives RSM with 3.3V
 1x = FPGA tri-states RSM pin

Bits 1 and 0: DS26502 RITD Tri-State and Level (RITDtri and RITD_Lev)

00 = FPGA drives RITD with 0V
 01 = FPGA drives RITD with 3.3V
 1x = FPGA Tristates RITD pin

Register Name: **LEVEL4**

Register Description: **DS26502 Pin Settings (TSM, TITD)**

Register Offset: **0x0014**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TSMtri	TSM_Lev	—	—	TITDtri	TITD_Lev
Default	0	0	0	0	0	0	0	0

Note: This register is only valid in hardware mode ($BIS[1:0] = 11$), and is ignored for other modes.

Bits 5 and 4: DS26502 TSM Tri-State and Level (TSMtri and TSM_Lev)

00 = FPGA drives TSM with 0V

01 = FPGA drives TSM with 3.3V

1x = FPGA tri-states TSM pin

Bits 1 and 0: DS26502 TITD Tri-State and Level (TITDtri and TITD_Lev)

00 = FPGA drives TITD with 0V

01 = FPGA drives TITD with 3.3V

1x = FPGA tri-states TITD pin

Register Name: **LEVEL5**

Register Description: **DS26502 Pin Settings (TCSS1, TCSS0)**

Register Offset: **0x0015**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TCSS1tri	TCSS1_Lev	—	—	TCSS0tri	TCSS0_Lev
Default	0	0	0	0	0	0	0	0

Note: This register is only valid in hardware mode ($BIS[1:0] = 11$), and is ignored for other modes.

Bits 5 and 4: DS26502 TCSS1 Tri-State and Level (TCSS1tri and TCSS1_Lev)

00 = FPGA drives TCSS1 with 0V

01 = FPGA drives TCSS1 with 3.3V

1x = FPGA tri-states TCSS1 pin

Bits 1 and 0: DS26502 TCSS0 Tri-State and Level (TCSS0tri and TCSS0_Lev)

00 = FPGA drives TCSS0 with 0V

01 = FPGA drives TCSS0 with 3.3V

1x = FPGA tri-states TCSS0 pin

Register Name: **LEVEL6**

Register Description: **DS26502 Pin Settings (TMODE3, TMODE2, TMODE1, TMODE0)**

Register Offset: **0x0016**

Bit #	7	6	5	4	3	2	1	0
Name	TMODE3 tri	TMODE3 _Lev	TMODE2 tri	TMODE2 _Lev	TMODE1 tri	TMODE1 _Lev	TMODE0 tri	TMODE0 _Lev
Default	0	0	0	0	0	0	0	0

Note: This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

Bits 7 and 6: DS26502 TMODE3 Tri-State and Level (TMODE3tri and TMODE3_Lev)

00 = FPGA drives TMODE3 with 0V

01 = FPGA drives TMODE3 with 3.3V

1x = FPGA tri-states TMODE3 pin

Bits 5 and 4: DS26502 TMODE2 Tri-State and Level (TMODE2tri and TMODE2_Lev)

00 = FPGA drives TMODE2 with 0V

01 = FPGA drives TMODE2 with 3.3V

1x = FPGA tri-states TMODE2 pin

Bits 3 and 2: DS26502 TMODE1 Tri-State and Level (TMODE1tri and TMODE1_Lev)

00 = FPGA drives TMODE1 with 0V

01 = FPGA drives TMODE1 with 3.3V

1x = FPGA tri-states TMODE1 pin

Bits 1 and 0: DS26502 TMODE0 Tri-State and Level (TMODE0tri and TMODE0_Lev)

00 = FPGA drives TMODE0 with 0V

01 = FPGA drives TMODE0 with 3.3V

1x = FPGA tri-states TMODE0 pin

Register Name: **LEVEL7**

Register Description: **DS26502 Pin Settings (L2, L1, L0)**

Register Offset: **0x0017**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	L2tri	L2_Lev	L1tri	L1_Lev	L0tri	L0_Lev
Default	0	0	0	0	0	0	0	0

Note: Settings for L2 are only valid in hardware mode ($BIS[1:0] = 11$), and ignored for other modes. In serial mode ($BIS[1:0] = 10$), L0 and L1 are used to set levels for CPHA and CPOL, respectively.

Bits 5 and 4: DS26502 L2 Tri-State and Level (L2tri and L2_Lev)

- 00 = FPGA drives L2 with 0V
- 01 = FPGA drives L2 with 3.3V
- 1x = FPGA tri-states L2 pin

Bits 3 and 2: DS26502 L1 Tri-State and Level (L1tri and L1_Lev)

- 00 = FPGA drives L1 with 0V
- 01 = FPGA drives L1 with 3.3V
- 1x = FPGA tri-states L1 pin

Bits 1 and 0: DS26502 L0 Tri-State and Level (L0tri and L0_Lev)

- 00 = FPGA drives L0 with 0V
- 01 = FPGA drives L0 with 3.3V
- 1x = FPGA tri-states L0 pin

Register Name: **LEVEL8**

Register Description: **DS26502 Pin Settings (TAIS, RLB)**

Register Offset: **0x0018**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TAIS tri	TAIS_Lev	—	—	RLBtri	RLB_Lev
Default	0	0	0	0	0	0	0	0

Note: This register is only valid in hardware mode ($BIS[1:0] = 11$), and is ignored for other modes.

Bits 5 and 4: DS26502 TAIS Tri-State and Level (TAIS tri and TAIS_Lev)

- 00 = FPGA drives TAIS with 0V
- 01 = FPGA drives TAIS with 3.3V
- 1x = FPGA tri-states TAIS pin

Bits 1 and 0: DS26502 RLB Tri-State and Level (RLBtri and RLB_Lev)

- 00 = FPGA drives RLB with 0V
- 01 = FPGA drives RLB with 3.3V
- 1x = FPGA tri-states RLB pin

Register Name: **LEVEL9**

Register Description: **DS26502 Pin Settings (MPS1, MPS0)**

Register Offset: **0x0019**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	MPS1tri	MPS1_Lev	—	—	MPSOtri	MPSO_Lev
Default	0	0	0	0	0	0	0	0

Bits 5 and 4: DS26502 MPS1 Tri-State and Level (MPS1tri and MPS1_Lev)

00 = FPGA drives MPS1 with 0V

01 = FPGA drives MPS1 with 3.3V

1x = FPGA tri-states MPS1 pin

Bits 1 and 0: DS26502 MPS0 Tri-State and Level (MPSOtri and MPSO_Lev)

00 = FPGA drives MPS0 with 0V

01 = FPGA drives MPS0 with 3.3V

1x = FPGA tri-states MPS0 pin

Register Name: **LEVEL10**

Register Description: **DS26502 Pin Settings (JAMUX, E1TS)**

Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	JAMUXtri	JAMUX_Lev	—	—	E1Tstri	E1TS_Lev
Default	0	0	0	0	0	0	0	0

Note: This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

Bits 5 and 4: DS26502 JAMUX Tri-State and Level (JAMUXtri and JAMUX_Lev)

00 = FPGA drives JAMUX with 0V

01 = FPGA drives JAMUX with 3.3V

1x = FPGA tri-states JAMUX pin

Bits 1 and 0: DS26502 E1TS Tri-State and Level (E1Tstri and E1TS_Lev)

00 = FPGA drives E1TS with 0V

01 = FPGA drives E1TS with 3.3V

1x = FPGA tri-states E1TS pin

Register Name: **TSERsrc**

Register Description: **DS26502 TSER Pin Source**

Register Offset: **0x001C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	ZEROS	ONES	RSER
Default	0	0	0	0	0	0	1	0

Note: Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TSER. Setting to 0 also tri-states this pin.

Bit 2: ZEROS. When set DS26502_TSER $\leftarrow$ 0.0V.

Bit 1: ONES. When set DS26502_TSER $\leftarrow$ 3.3V.

Bit 0: RSER. When set DS26502_TSER $\leftarrow$ DS26502_RSER.

Register Name: **MCLKsrc**

Register Description: **DS26502 MCLK Pin Source**

Register Offset: **0x001D**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	ZERO	EXT	T1	E1
Default	0	0	0	0	0	0	1	0

Note: Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to MCLK. Setting to 0 also tri-states this pin.

Bit 3: ZERO. When set DS26502_MCLK $\leftarrow$ 0.0V.

Bit 2: EXT. When set DS26502_MCLK $\leftarrow$ External_Osc (BNC connector).

Bit 1: T1. When set DS26502_MCLK $\leftarrow$ T1_OSC (1.544MHz).

Bit 0: E1. When set DS26502_MCLK $\leftarrow$ E1_OSC (2.048MHz).

Register Name: **TCLKsrc**

Register Description: **DS26502 TCLK Pin Source**

Register Offset: **0x001E**

Bit #	7	6	5	4	3	2	1	0
Name	—	EXT	T1	E1	64KHZ	6312	PLL	RCLK
Default	0	0	1	0	0	0	0	0

Note: Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TCLK. Setting to 0 also tri-states this pin.

Bit 6: EXT. When set DS26502_TCLK ← External_Osc (BNC connector).

Bit 5: T1. When set DS26502_TCLK ← T1_OSC (1.544MHz).

Bit 4: E1. When set DS26502_TCLK ← E1_OSC (2.048MHz).

Bit 3: 64KHZ. When set DS26502_TCLK ← 64kHz clock.

Bit 2: 6312. When set DS26502_TCLK ← 6312kHz clock.

Bit 1: PLL. When set DS26502_TCLK ← DS26502_PLL.

Bit 0: RCLK. When set DS26502_TCLK ← DS26502_RCLK.

Register Name: **TS_8Ksrc**

Register Description: **DS26502 TS_8K Pin Source**

Register Offset: **0x001F**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	EXT	_8KHz	400HZ	400HZ_502	RS_8K
Default	0	0	0	0	0	0	1	0

Note: Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TS_8K. Setting to 0 also tri-states this pin.

Bit 4: EXT. When set DS26502_TS_8K ← External_Osc (BNC connector).

Bit 3: _8KHz. When set DS26502_TS_8K ← 8kHz (derived by FPGA).

Bit 2: 400HZ. When set DS26502_TS_8K ← 400Hz clock (derived by FPGA).

Bit 1: 4KHZ_502. When set DS26502_TS_8K ← DS26502_400hz.

Bit 0: RS_8K. When set DS26502_TS_8K ← DS26502_RS_8K.

DS26502 INFORMATION

For more information about the DS26502, consult the DS26502 data sheet available on our website at www.maxim-ic.com/DS26502. Software downloads are also available for this design kit.

DS26502DK INFORMATION

For more information about the DS26502DK, including software downloads, consult the DS26502DK data sheet available on our website at www.maxim-ic.com/DS26502DK.

TECHNICAL SUPPORT

For additional technical support, go to www.maxim-ic.com/support.

SCHEMATICS

The DS26502DK schematics are featured in the following pages.

DOCUMENT REVISION HISTORY

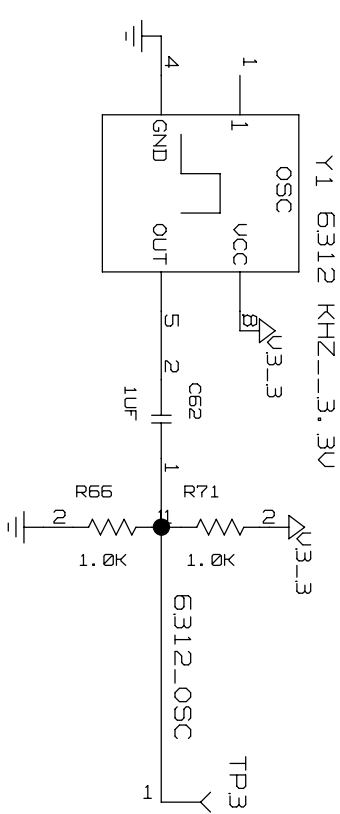
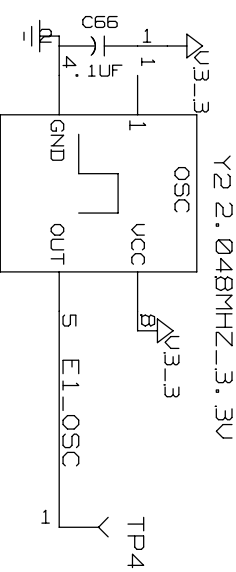
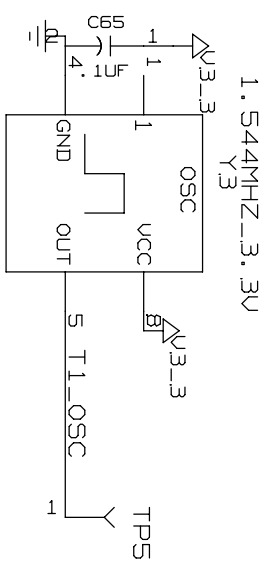
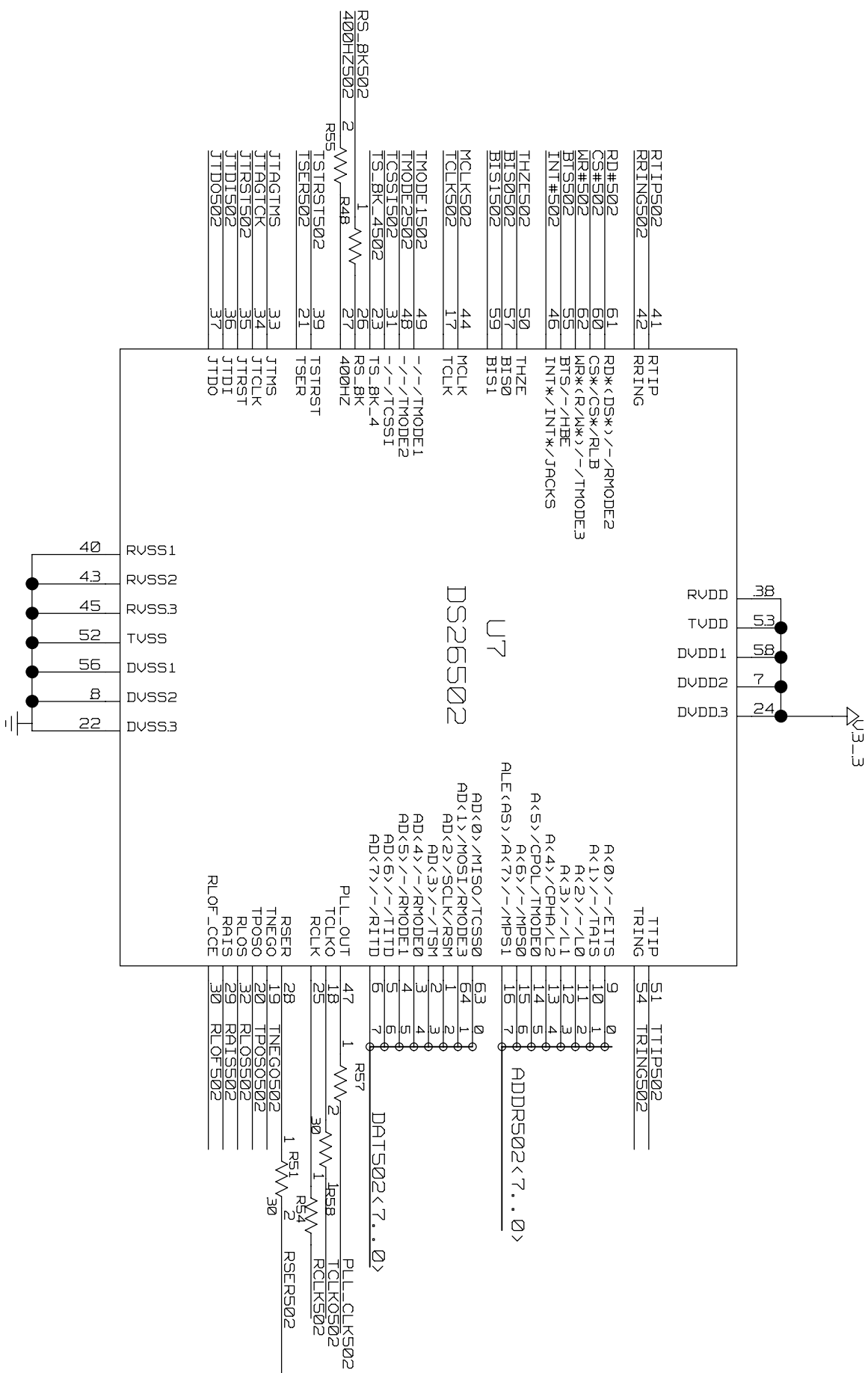
REVISION DATE	DESCRIPTION
030705	Initial DS26502DK data sheet release.
070505	Updated <i>Features</i> , <i>Component List</i> (lines 1 and 2), and <i>Errata</i> sections.
071006	Updated descriptions for FPGA Control Registers LEVEL1 to LEVEL10.
110106	Updated schematics.
031507	Corrected typo on Bit 0 of TSERsrc register Corrected typo on Bit 0 of TS_8Ksrc register

DS26502 DESIGN KIT

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- 2. DS26502 AND OSCILLATORS
- 3. DS26502 LINE BUILD OUT
- 4. XILINX CLOCK MUX AND BUS CONVERSION
- 5. TEST POINTS FOR DS26502
- 6. MMC2107 PROCESSOR
- 7. PROCESSOR CONFIGURATION
- 8. XILINX CONFIGURATION AND CORE VOLTAGE
- 9. SERIAL PORTS AND JTAG CONFIGURATION
- 10. MEMORY
- 11. PROCESSOR TEST POINTS
- 12. FLASH VOLTAGE AND DECOUPLING
- 13. SIGNAL CROSS REFERENCE
- 14. PART CROSS REFERENCE AND REVISION HISTORY

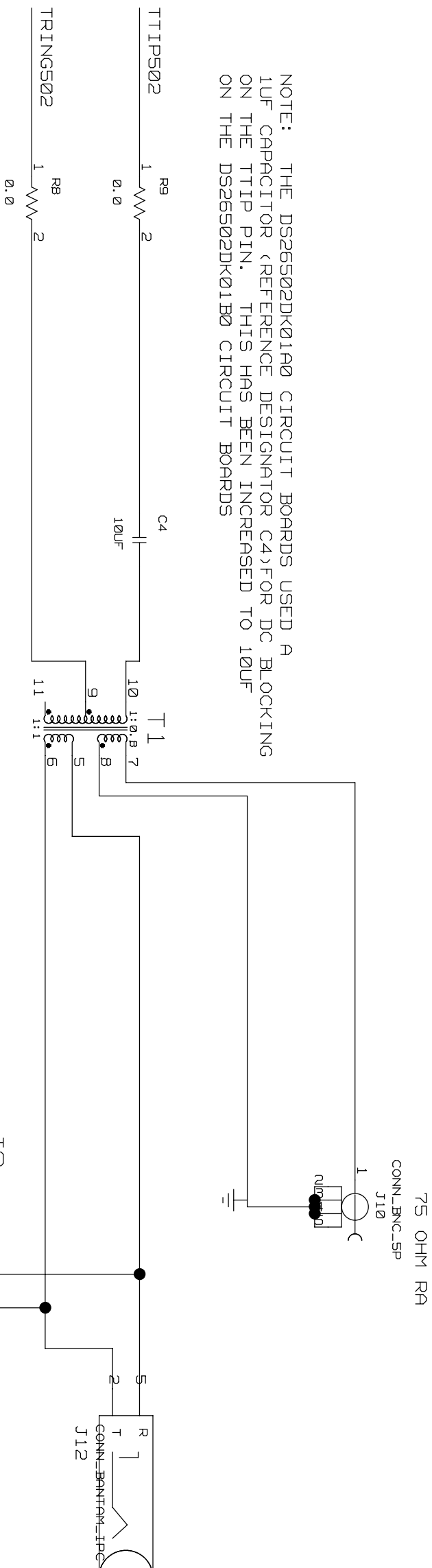
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TITLE:	DS26502DK01B0	DATE:	041205
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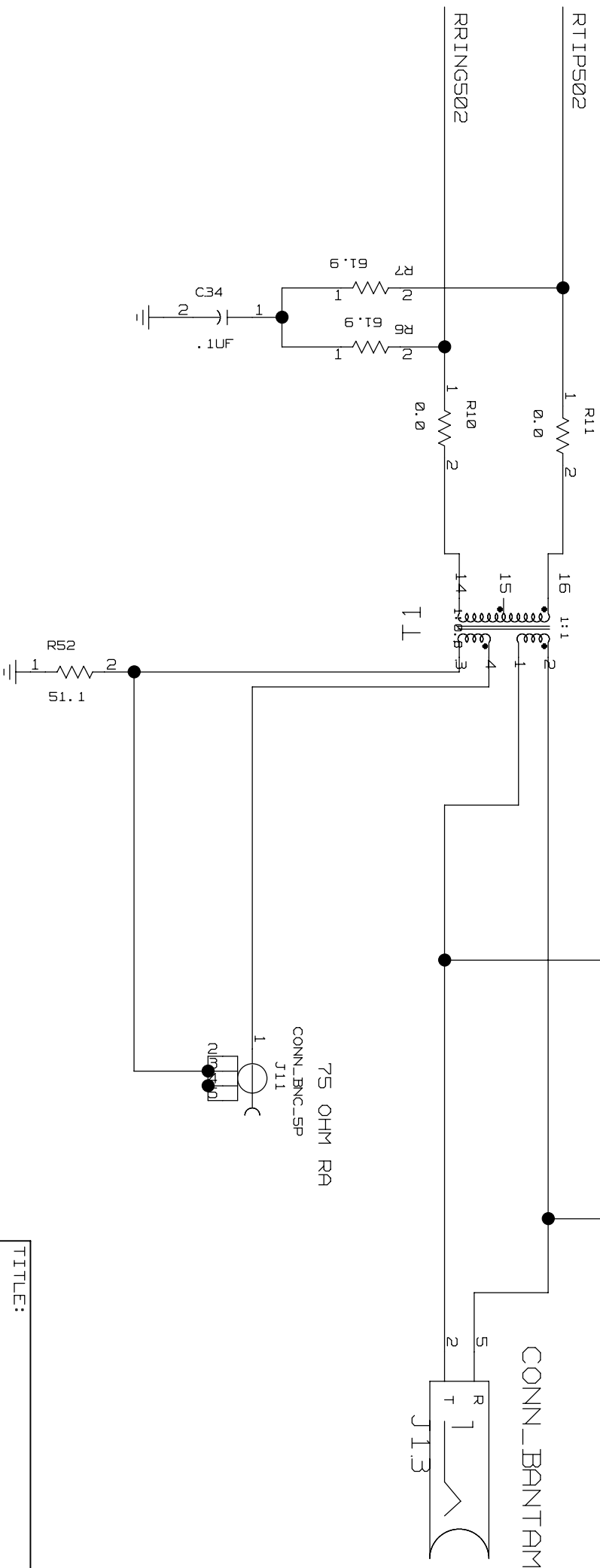


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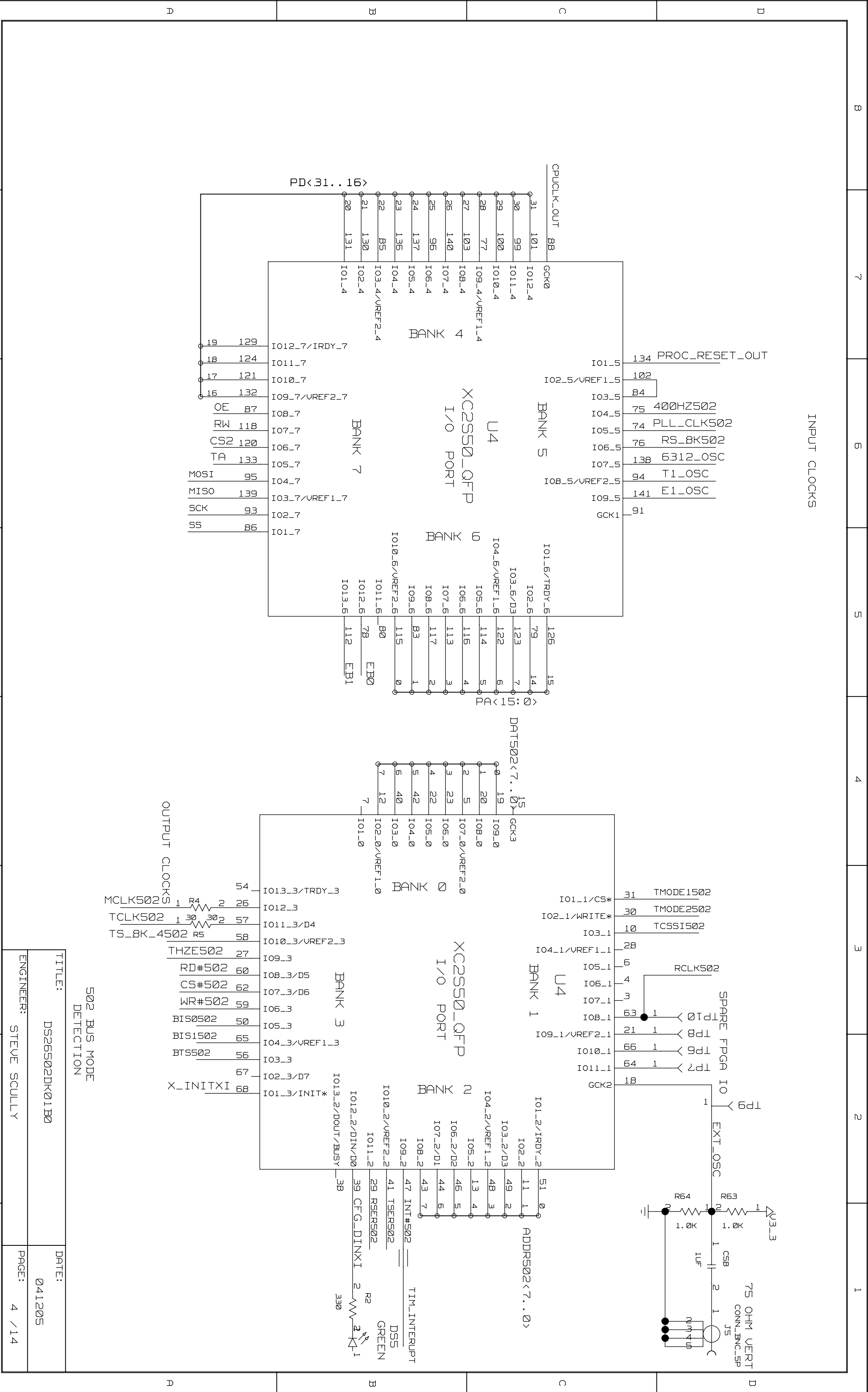
NOTE: THE DS26502DK01A0 CIRCUIT BOARDS USED A 1UF CAPACITOR (REFERENCE DESIGNATOR C4)FOR DC BLOCKING ON THE TTIP PIN. THIS HAS BEEN INCREASED TO 10UF ON THE DS26502DK01B0 CIRCUIT BOARDS

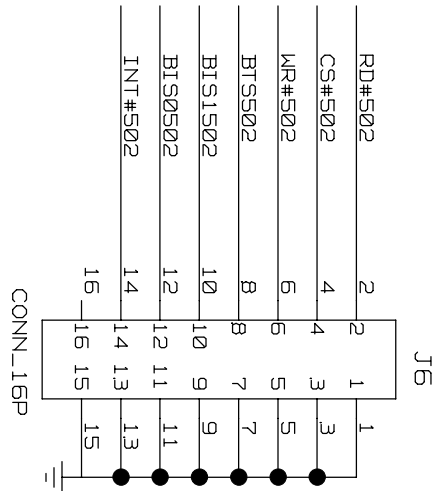
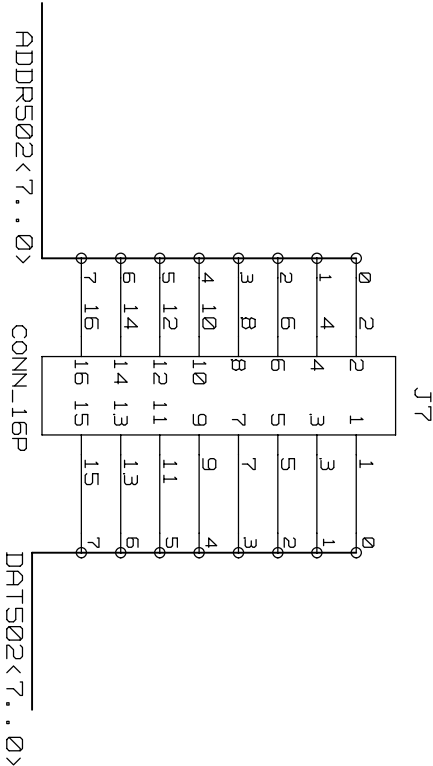
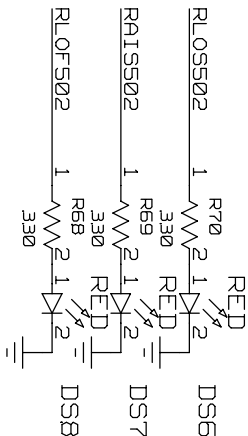
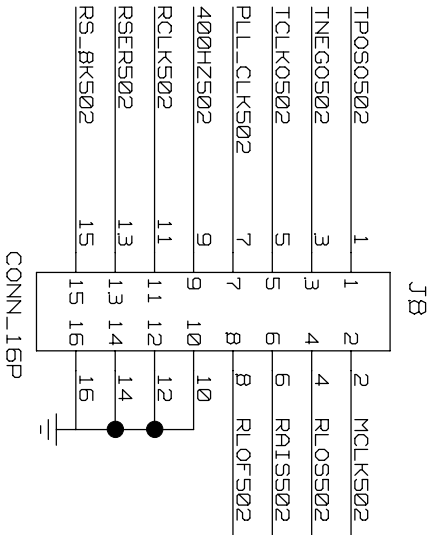
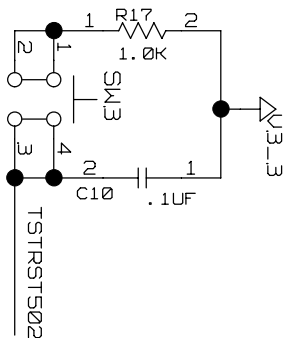


NOTE: BOARD REVISIONS DS26502DK01A0 AND DS26502DK01B0 DO NOT USE THE CORRECT PIN NUMBERS ON THE RJ48 CONNECTOR (REFERENCE DESIGNATOR J9). THE RJ48 CONNECTOR SHOULD BE REMOVED SINCE IT HAS NON-STANDARD CONNECTION. THE SCHEMATIC HAS BEEN UPDATED AND IS CORRECT.

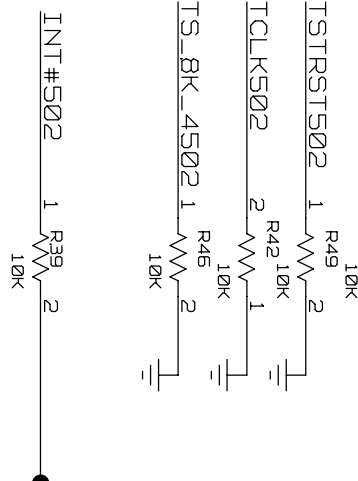
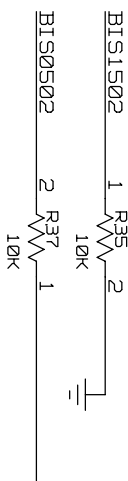


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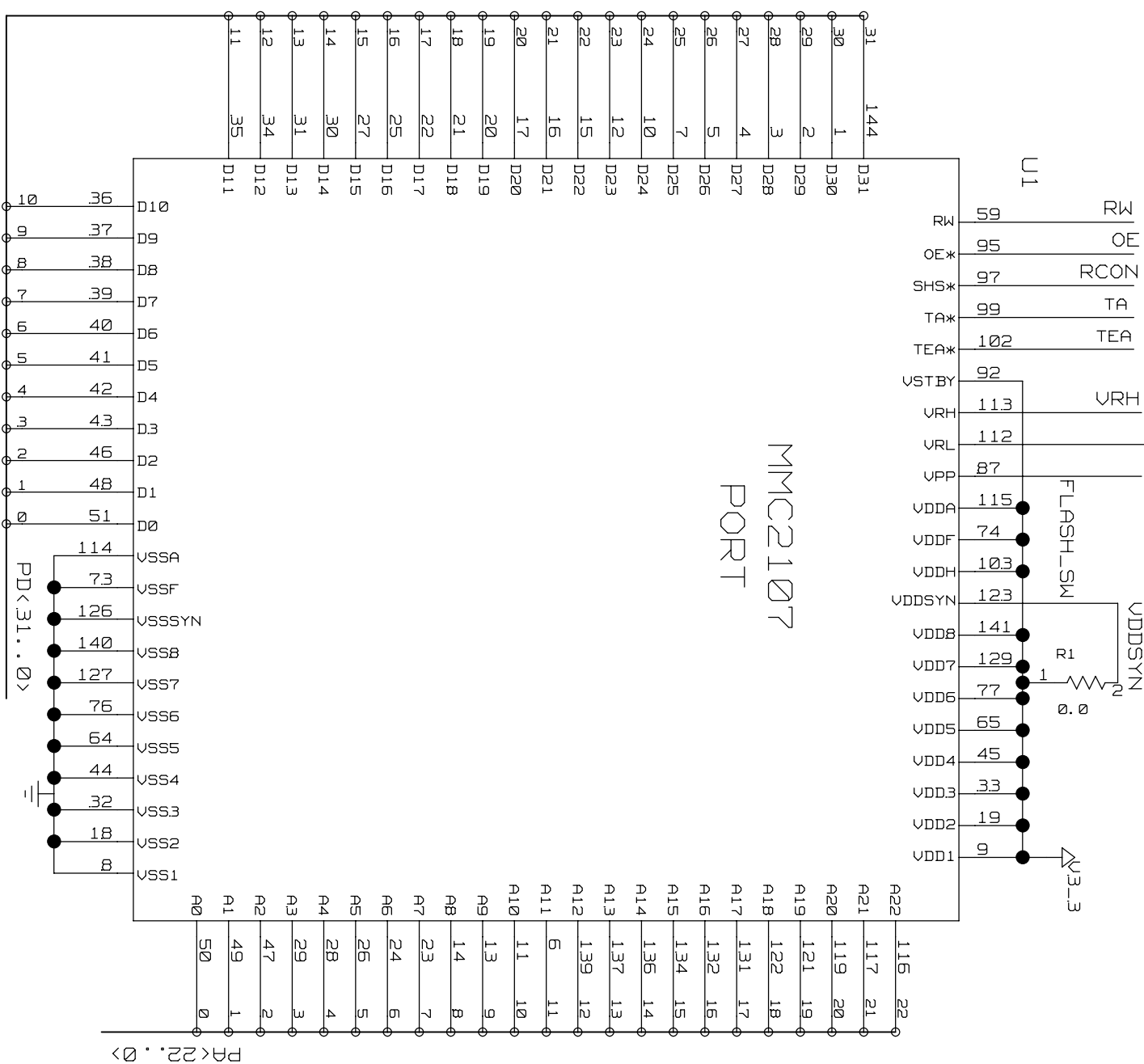
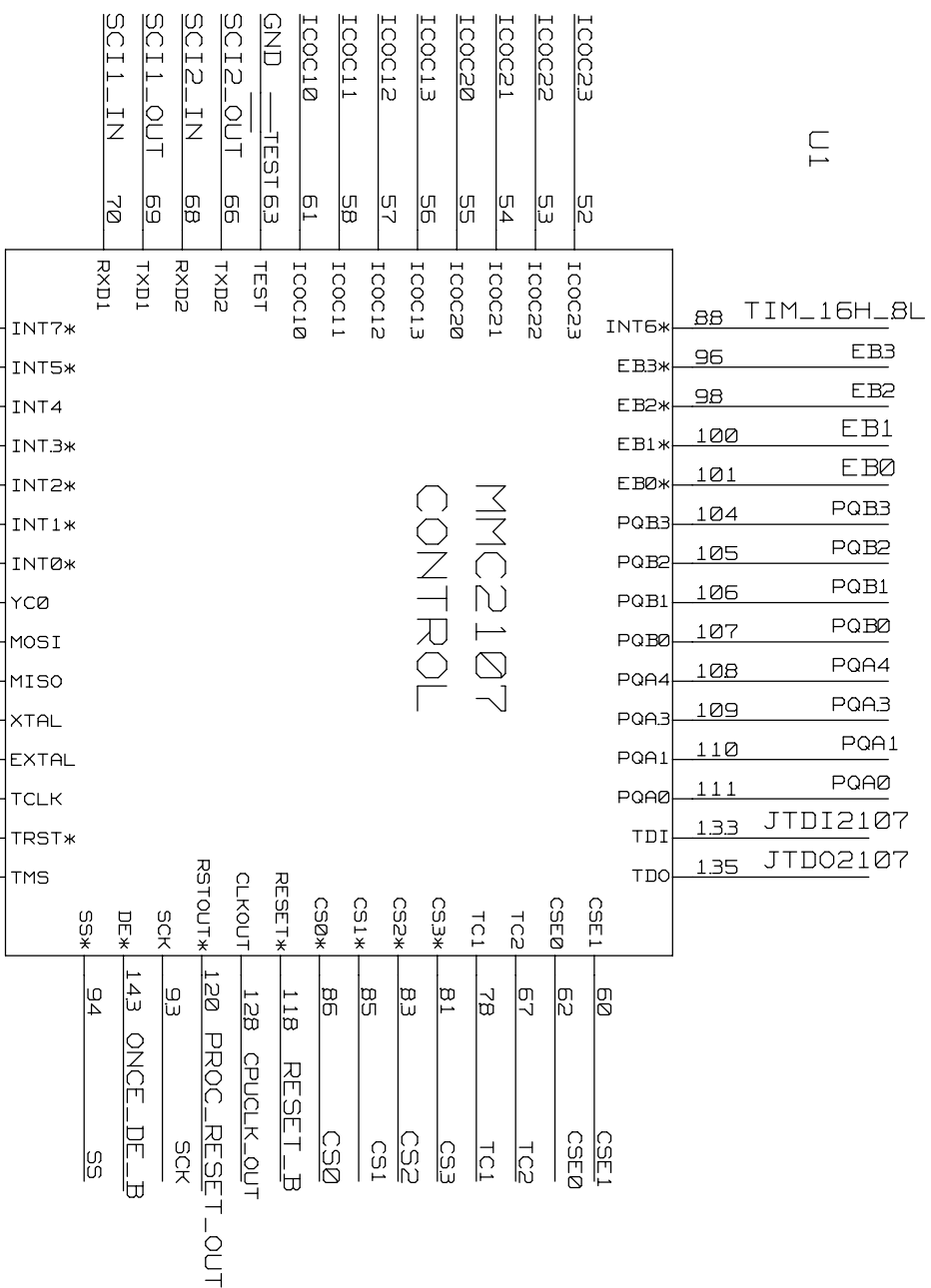




BISCI:0J : 01 = PARALLEL PORT MODE
DEFAULT MODE (NON-MULTIPILEXED)

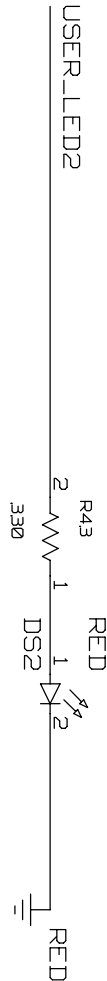
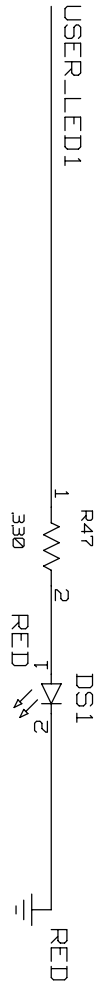
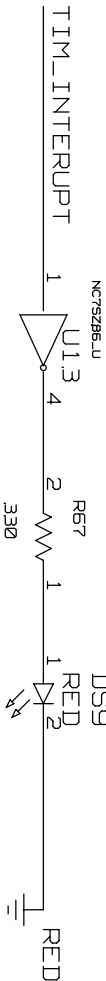
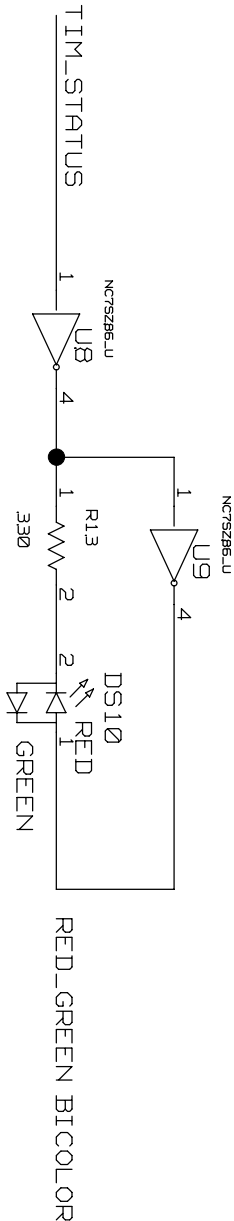
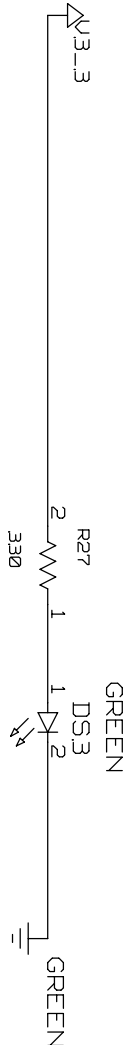
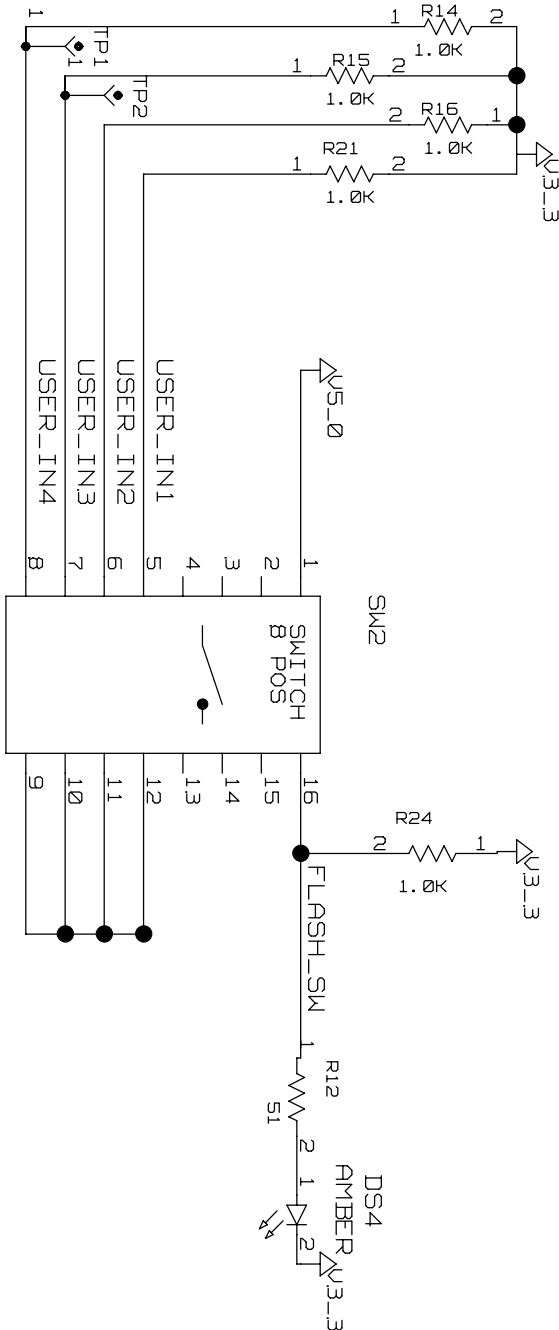
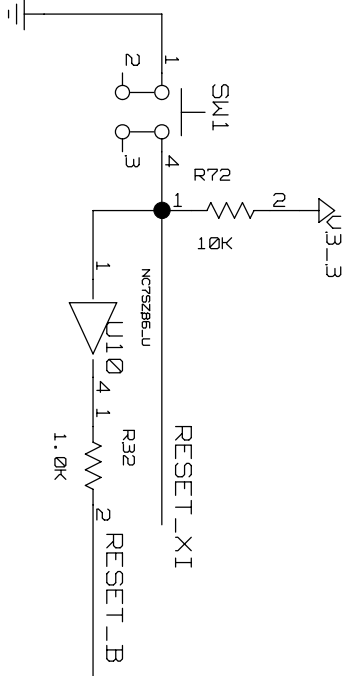
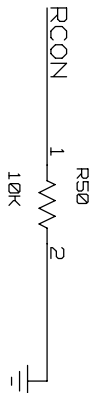
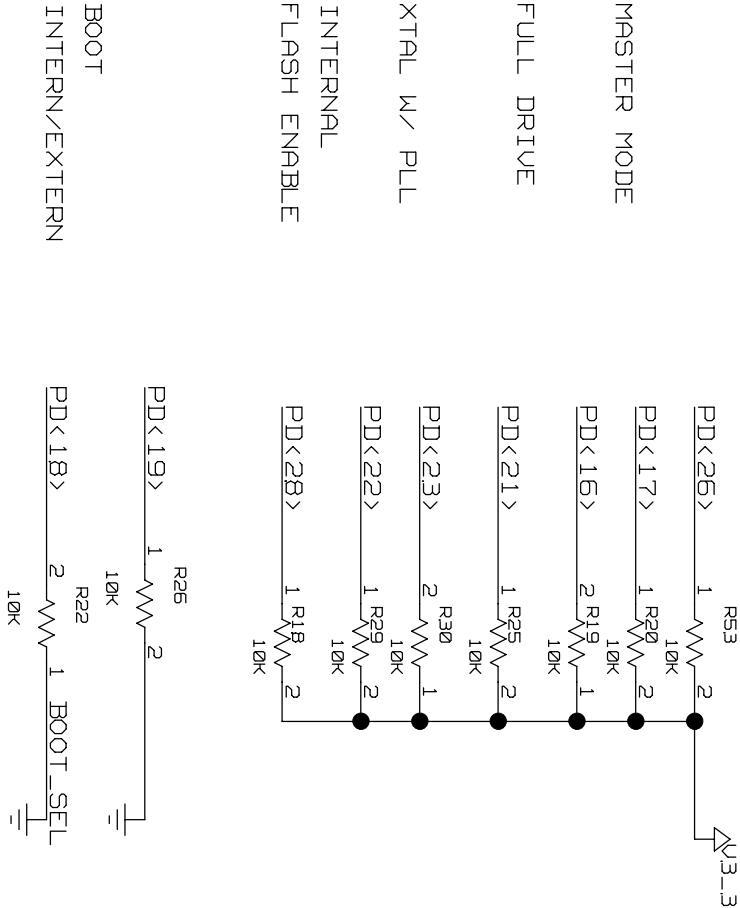


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DS26S02DK01B0	041205
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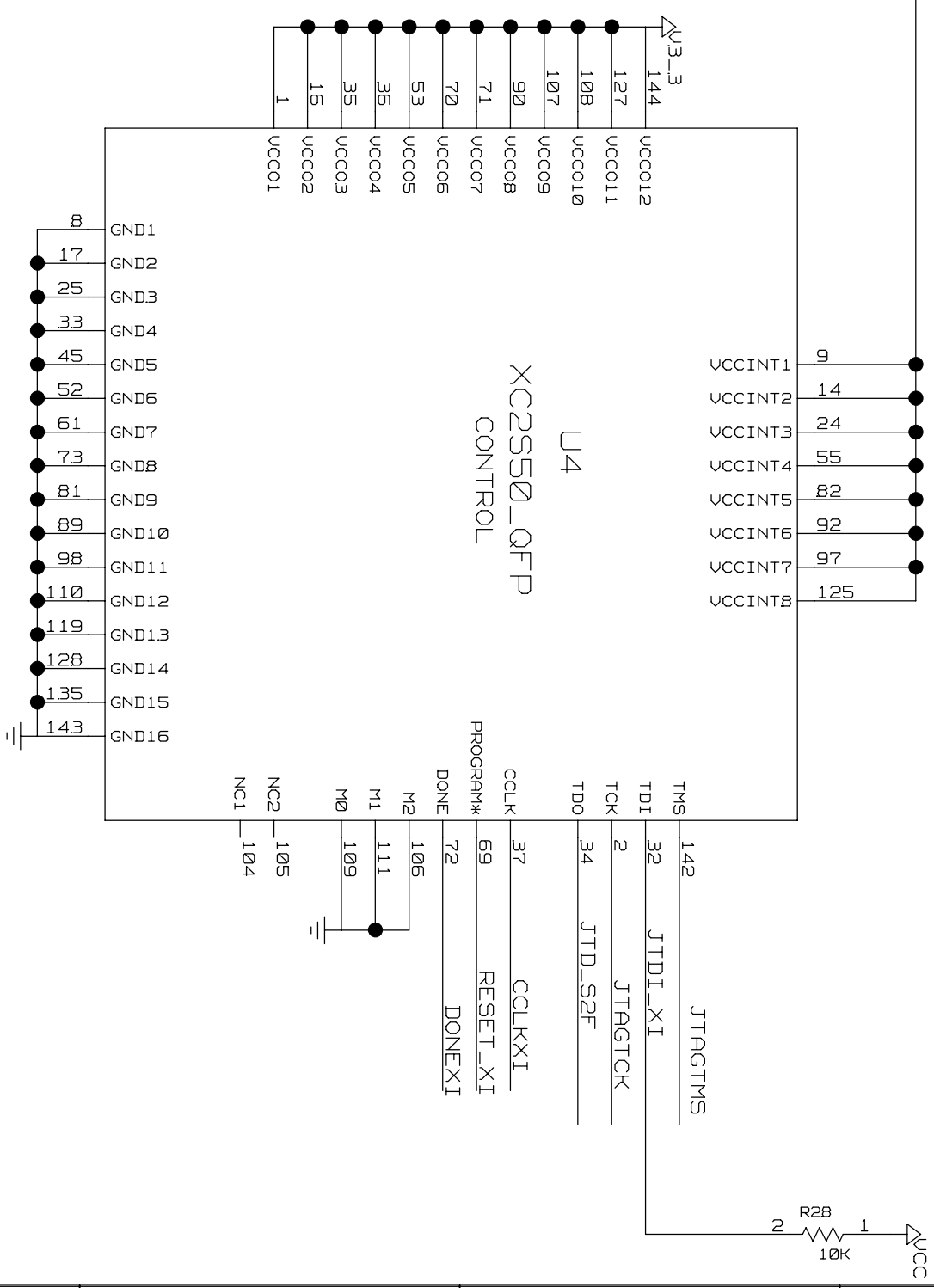
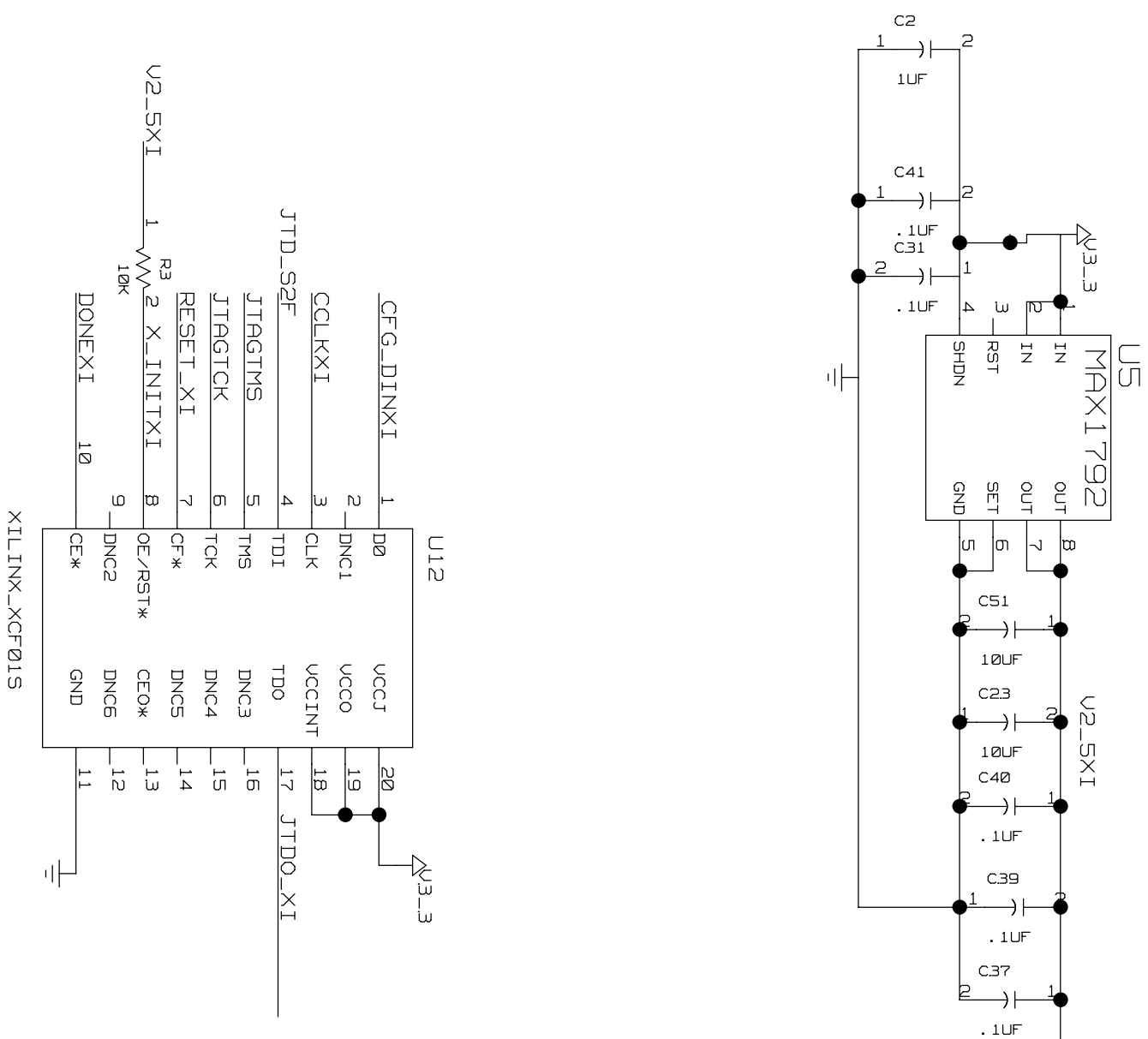
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DS26502DK01B0	041205
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RESET CONFIGURATION



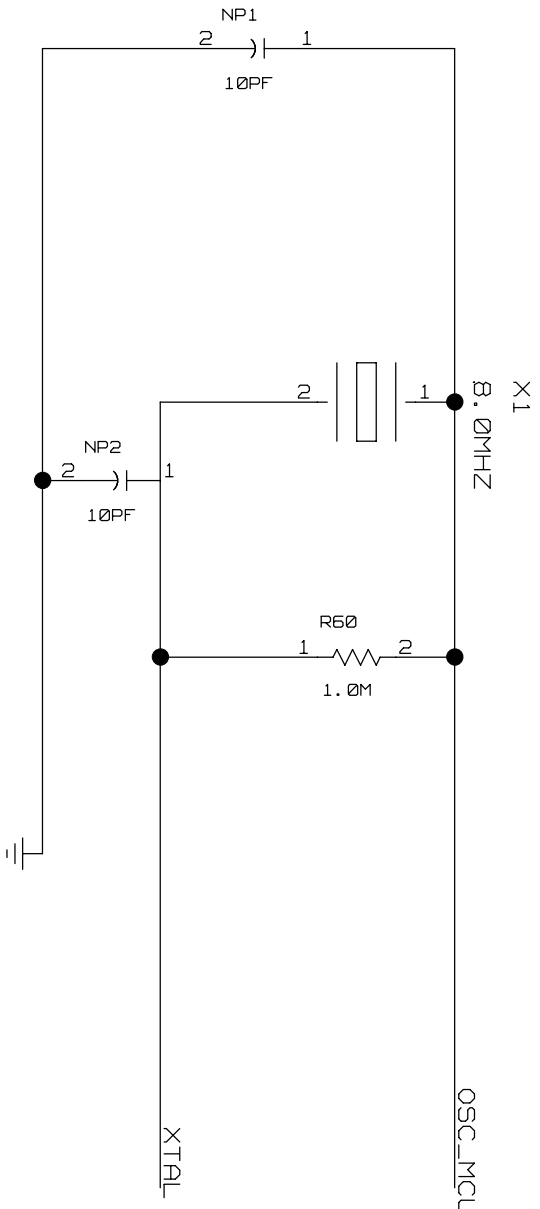
RESET AND CHIP CONFIGURATION

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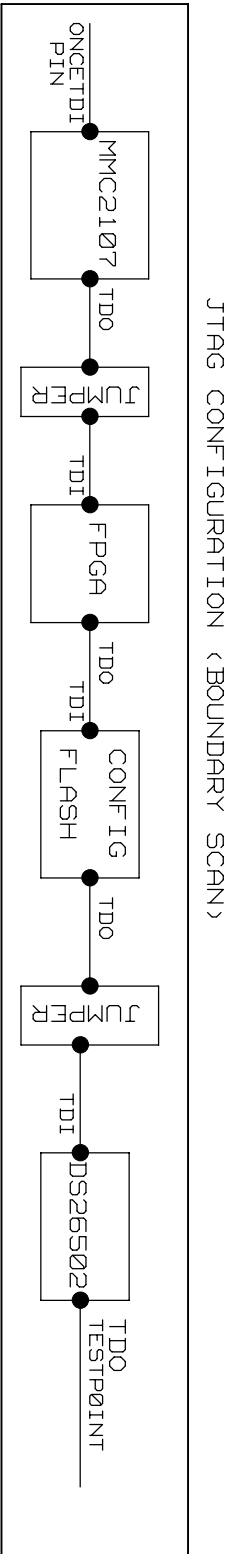
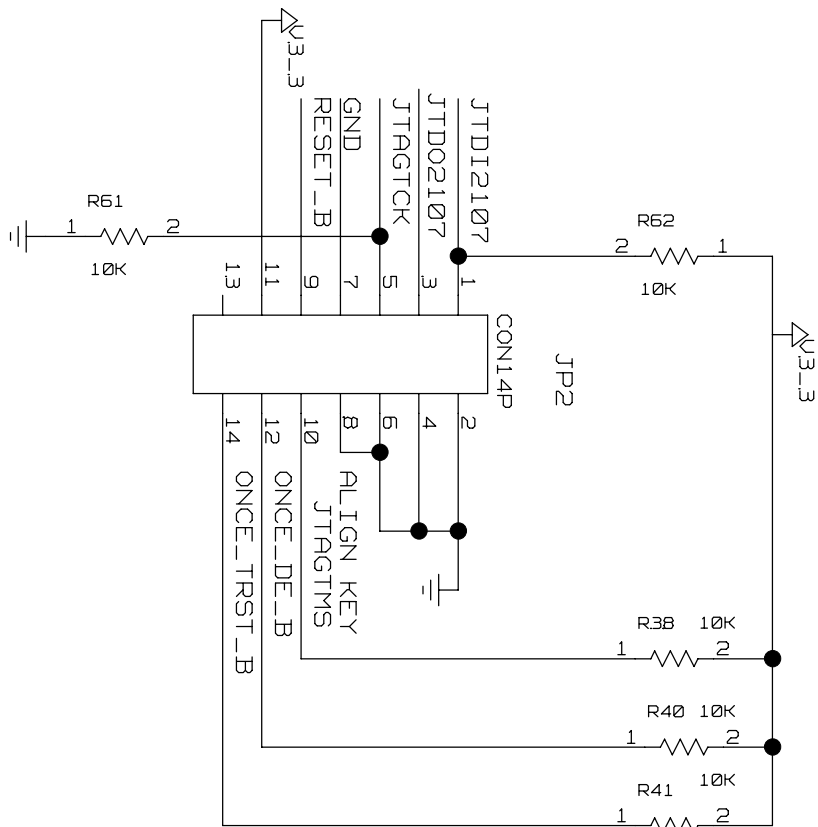
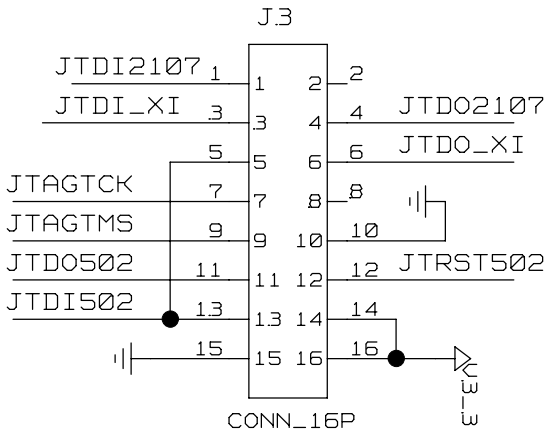
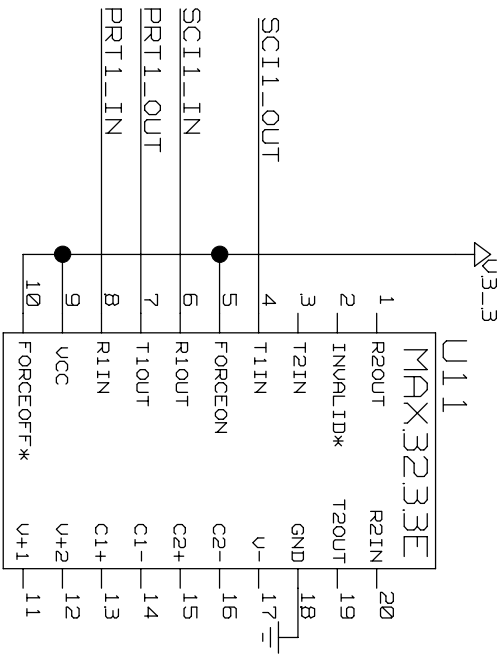


CLOCKS

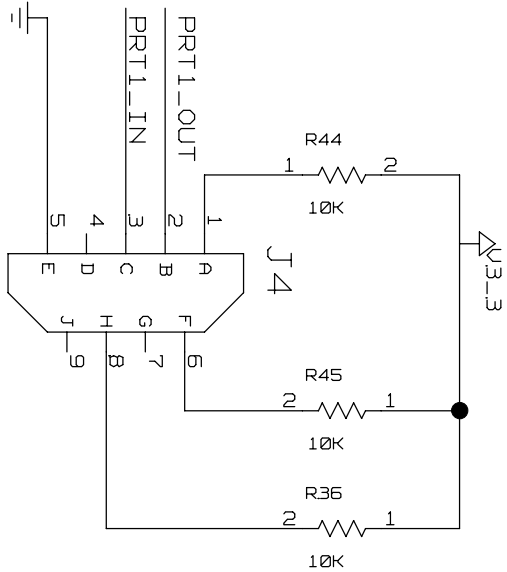
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DS26502DK01B0	041205
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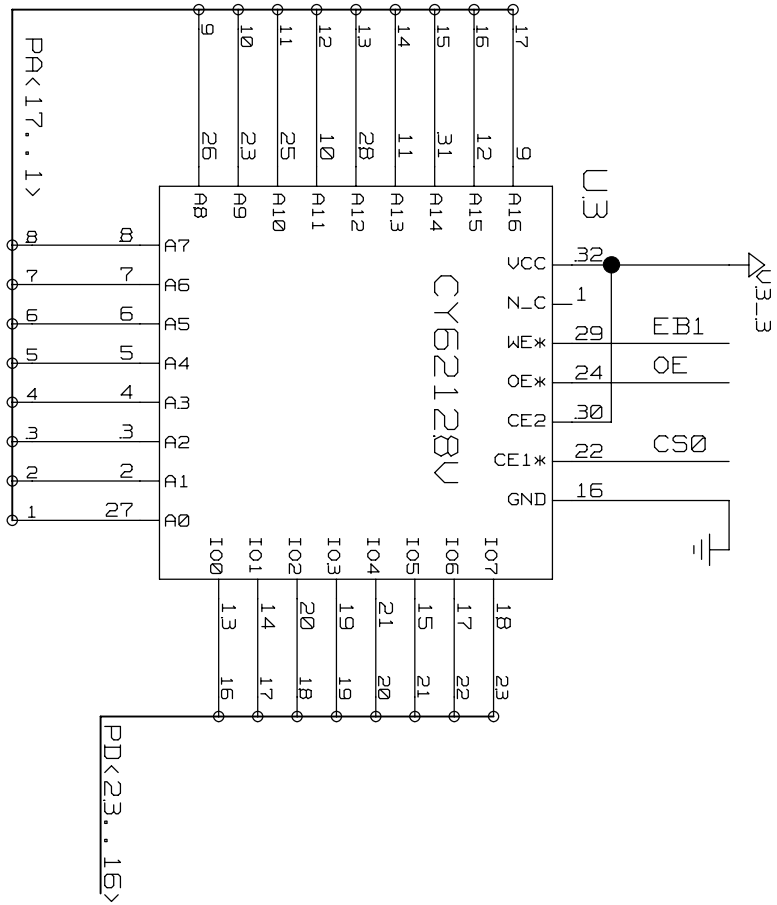
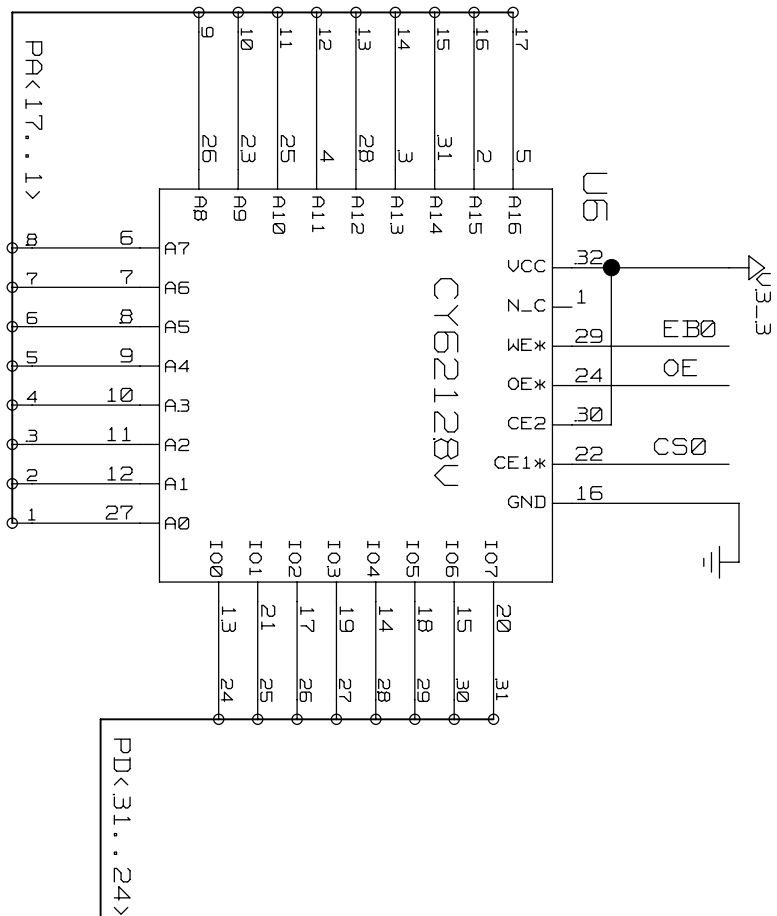
JTAG / ONCE
DEBUG SELECTION



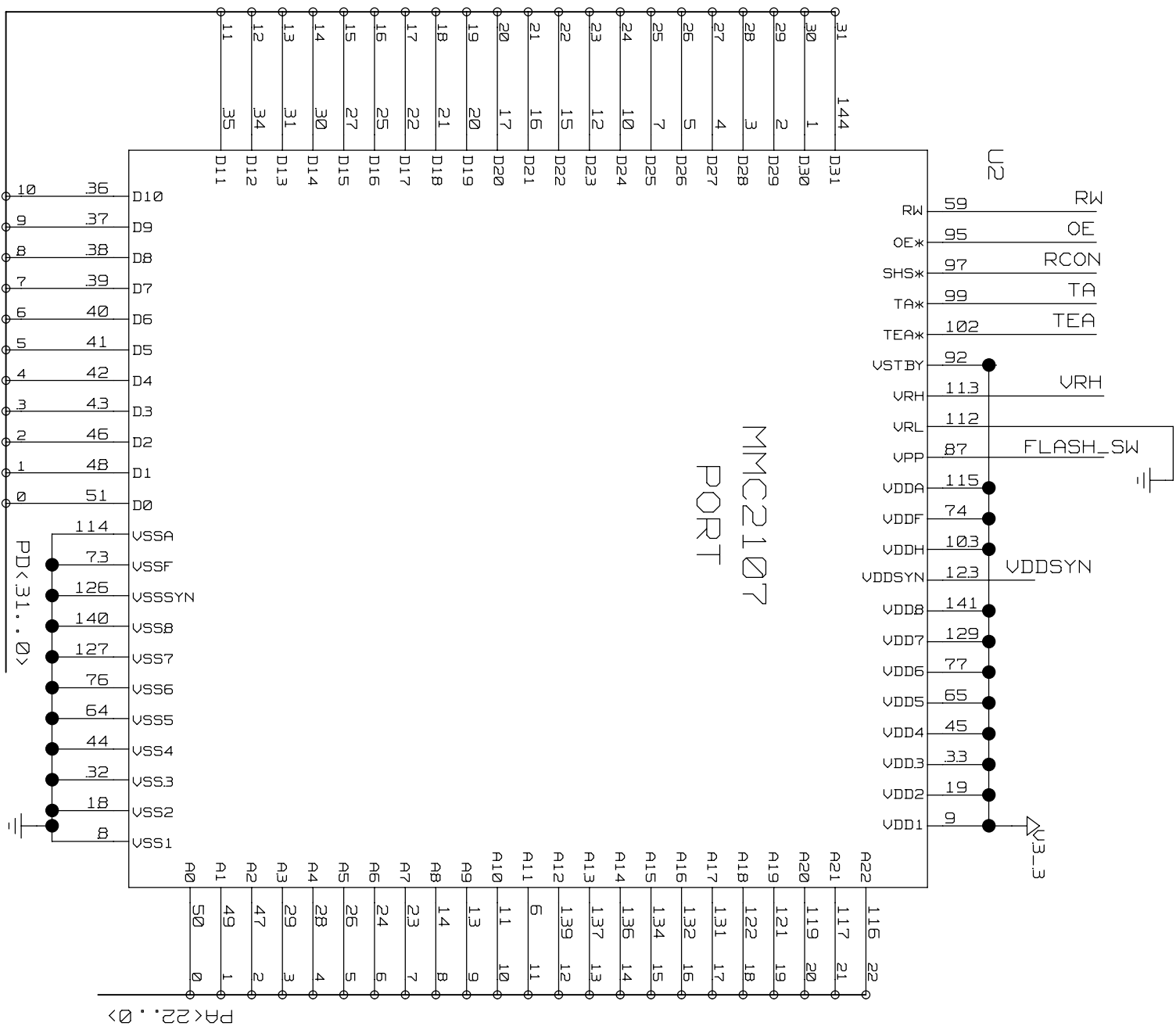
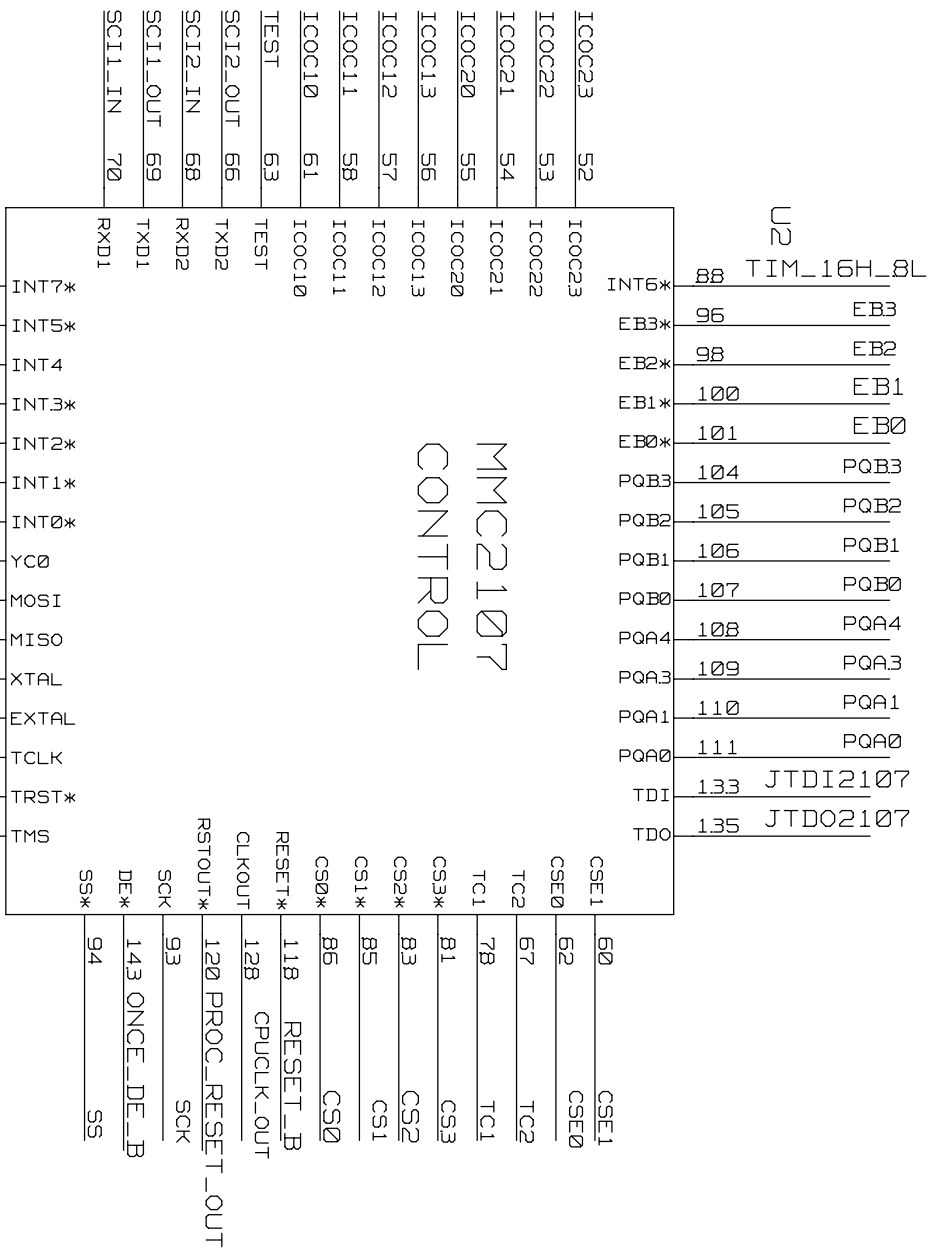
PROCESSOR DEBUG CONFIGURATION (ONCE)



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TEST-POINTS FOR PROCESSOR

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