ANALOG MULTIPLIER

■ GENERAL DESCRIPTION

The NJM4200 is the industry's first integrated circuit multiplier to have complete compensation for nonlinearity, the primary source of error and distortion. This is also the first IC mustiplier to have three on-board operational amplifiers designed specifically for use in multiplier logging circuits. These specially-designed amplifiers are frequency compensated for optimum AC response in a logging circuit; the heart of a multiplier, and can therefore provide superior AC response in comparison to other analog multipliers.

Versatility is unprecedented; this is the first IC multiplier that can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, one-quadrant division or square-rooting, and RMS-to-DC conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very low tempco on accuracy.

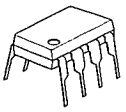
The excellent linearity and versatility were achieved through circuit design rather than special grading or trimming therefore unit cost is very low. Analog multipliers can now be used in application where price was previously an inhibiting factor.

The NJM4200 is ideal for use in low-distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

■ FEATURES

- High accuracy
  Non-linearity (0.3% max.)
  Temperature coefficient (0.005%/℃ typ.)
- Multiple functions
  Multiply, divide, square, square root, RMS-to-DC conversion, AGC, and modulate/demodulate
- Wide bandwidth (4MHz typ.)
- Package Outline DIP8, DMP8
- Bipolar Technology

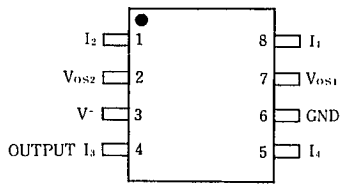
■ PACKAGE OUTLINE



NJM4200D

NJM4200M

■ CONNECTION DIAGRAM



NJM4200D
NJM4200M

6

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^-	−22	V
Power Dissipation	P_D	(DIP8) 500	mW
		(DMP8) 300	mW
Input Current	I_{IN}	−5	mA
Operating Temperature Range	T_{opr}	−40～+85	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^-=−15V)

PARAMETER	SYMBOL	TEST CONDITION	NJM4200			UNIT
			MIN.	TYP.	MAX.	
Input range(I_1,I_2 and I_4)	I_{IN}		1.0	—	1000	μA
Total error as multiplier						
Untrimmed	—		—	—	±3.0	%
With external trim	—		—	—	±0.5	%
Versus temperature	—	Operational Temperature Range	—	±0.005	—	%/°C
Versus Supply	—	V^-=−9V～−18V	—	±0.1	—	%/V
Nonlinearity	—	50μA<I<250μA	—	—	±0.3	%
Input offset voltage	V_{IO}	I_1=I_2=I_4=150μA	—	—	±10	mV
Input bias current	I_B	I_1=I_2=I_4=150μA	—	—	500	nA
Average temperature coefficient of input offset voltage	—	I_1=I_2=I_4=150μA	—	—	±100	μV/°C
Output current range(I_3)	I_0	(Note 1)	1.0	—	1000	μA
Frequency response, −3 dB	f_R		—	4	—	MHz
Operating voltage	V^-		−9	−15	−18	V
Operating Current	I_{CC}	I_1=I_2=I_4=150μA, Ta=25℃	—	—	4	mA

Note 1: These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700 ohms and must be pulled up to a positive supply such that the voltage on pin (3) stays within a range of 0 to +5V.

■ FUNCTION DESCRIPTION

The NJM4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in Figure 1. The nominal relationship between the three inputs and the output is:

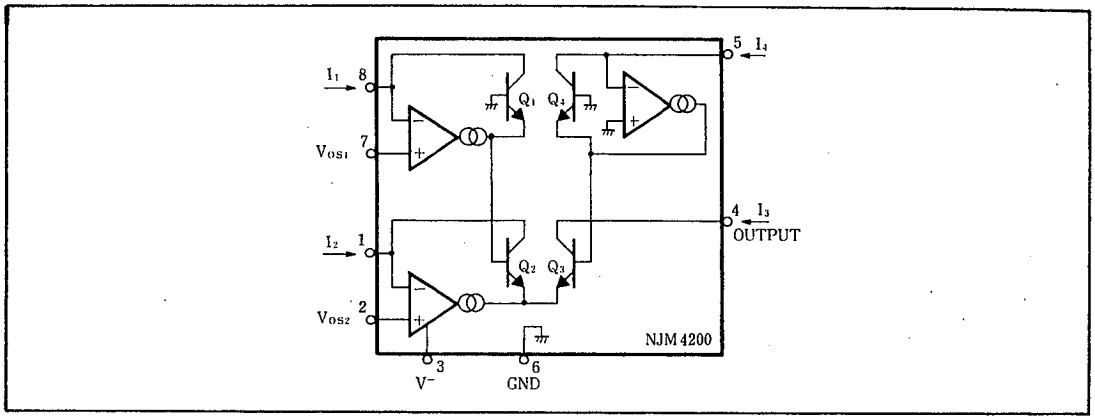


Figure 1. 4200 Multiplier Functional Diagram

$$I_3=\frac{I_1 I_2}{I_4} \qquad (1)$$

All four currents must be positive and restricted to a range of 1μA to 1mA. The three input currents go into the multiplier chip at op-amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op-amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op-amps make the collector currents of transistors Q_1, Q_2, and Q_4 equal to their respective input currents (I_1, I_2, and I_4). These op-amps are designed with current-source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op-amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op-amps operate on a single-supply voltage (nominally −15V) and total quiescent current drain is less than 4mA. These special op-amps provide significantly improved performance in comparison to 741-type op-amps.

The actual multiplication is done within the log-antilog configuration of the Q_1–Q_4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship.

$$V_{BEN}=\frac{kT}{q}\ln\frac{I_{CN}}{I_{SN}} \qquad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above quation; the collector current times the emitter resistance. This $I_C r_E$ term can cause significant linearity error. In four-quadrant multiplier circuits, this added $I_C r_E$ term introduces a parabolic nonlinearity even with matched transistors. New JRC has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this New JRC-developed circuit technique compensates linearity error over temperature changes. The nonlinearity-versus-temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{kT}{q}\left[\ln\frac{I_1}{I_{S1}}+\ln\frac{I_2}{I_{S2}}-\ln\frac{I_3}{I_{S3}}-\ln\frac{I_4}{I_{S4}}\right]=0 \qquad (3)$$

The equation reduces to: $$\frac{I_1 I_2}{I_3 I_4}=\frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \qquad (4)$$

The ratio of reverse saturation currents, $I_{S1}I_{S2}/I_{S3}I_{S4}$ depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the ratio is very close to unity, typically 1.0±1%. The final result is the desired relationship:

$$I_3=\frac{I_1 I_2}{I_4} \qquad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Applications

Four-Quadrant, General-Purpose Multiplier

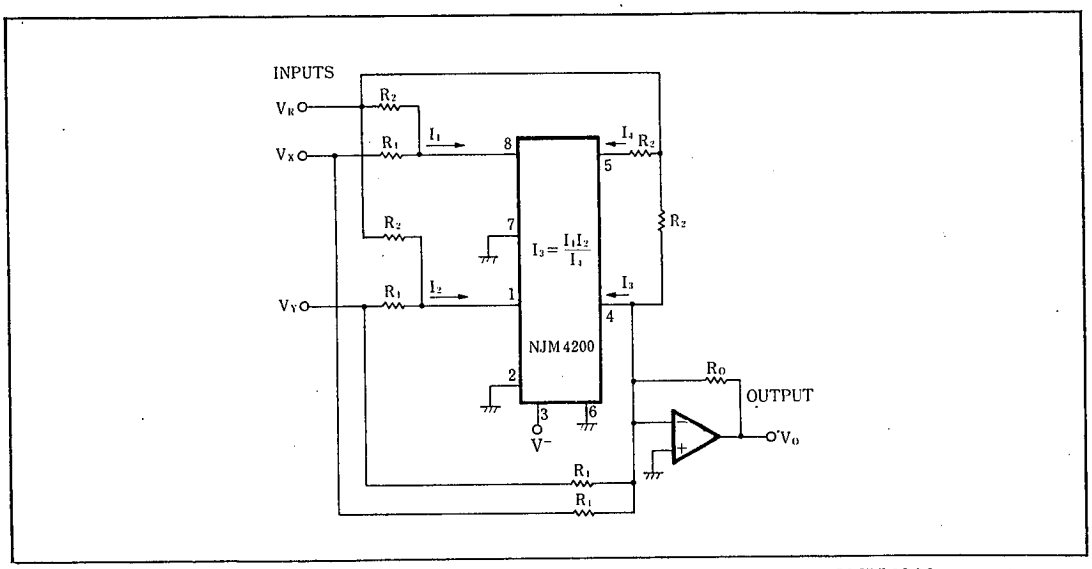


Figure 2. Four-Quadrant General Purpose Multiplier Using the NJM4200

The general schematic for a four-quadrant multiplier using the NJM4200 IC is shown in Figure 2. A positive reference voltage, V_R, is used to offset the multiplier chip. To stay within the most linear operating range, it is necessary that V_R/R_2 plus V_X/R_1 be limited to a range of 50μA to 250μA. Within the operating range, input and output currents are given by the following equations:

$$I_1=\frac{V_X}{R_1}+\frac{V_R}{R_2} \qquad I_2=\frac{V_Y}{R_1}+\frac{V_R}{R_2} \qquad I_3=\frac{V_X}{R_1}+\frac{V_Y}{R_1}+\frac{V_R}{R_2}+\frac{V_0}{R_0} \qquad I_4=\frac{V_R}{R_2}$$

Combining these relationships through the equation $I_3=I_1I_2/I_4$ yields:

$$V_0=\frac{R_0R_2}{R_1^2}\frac{V_XV_Y}{V_R}$$

The reference voltage V_R must be positive, but V_X and V_Y can be AC voltages. The positive supply voltage can be used as the reference in many applications where a well-regulated +15V is available. Some typical values for a multiplier scaled at $V_XV_Y/10$ are calculated below:

Given: V_X and V_Y have range of −10V to +10V
Desired scaling is $V_0=V_XV_Y/10$
Reference voltage V_R is +15V

Calculation:

(1) Choose $R_1=100k\Omega$

From requirement of +50μA minimum

$$\frac{-10V}{100K}+\frac{15V}{R_2}\geq 50\mu A$$

(2) Calculate R_0 from $\frac{R_0R_2}{R_1^2}\frac{1}{V_R}=\frac{1}{10}$

$$R_0=\frac{R_1^2}{R_2^2}\frac{V_R}{10}$$

$$R_0=(100k\Omega)15/10$$

$$R_0=150k\Omega$$

Results:

$$V_0=\frac{V_XV_Y}{10} \text{ with } V_R=+15V$$

$R_1, R_2=100k\Omega$

$R_0=150k\Omega$

These values cause a range on I_1 and I_2 of 50μA to 250μA to for V_X and V_Y of −10V to +10V.

While the choice of values for R_1,R_2 and R_0 are arbitrary, best results are obtained by operating I_1 and I_2 over a range of approximately 50μA to 250μA.

Accuracy of the four-quadrant multiplier is dependent upon both the NJM4200 chip and the external components. AC feedthrough, which is the undesired output when multiplying one AC input by zero on the other input, is dependent on op amp offsets and on the matching of the R_1 and R_2 resistor sets. Gain accuracy depends on the external reference voltage V_R, the resistor ratio R_0R_2/R_1^2, and the multiplier chip. Linearity depends almost entirely upon the multiplier IC. The linear error terms can all be nulled externally by trimming resistor ratios or offsets. A four-quadrant multiplier with provision for external trimming of linear error components is shown in Figure 3. The optimum mix of component tolerances, trimming range, and cost is very application dependent. With moderate-cost components and no external trimming, the NJM4200 is more accurate than many of the complete IC multipliers. With precision components and external trimming as shown in Figure 3, the NJM4200 is capable of performance comparable to the best hybrid or modular multipliers.

The error analysis is most easily done by separately considering resistor match, offsets, and gain; then superimposing the results.

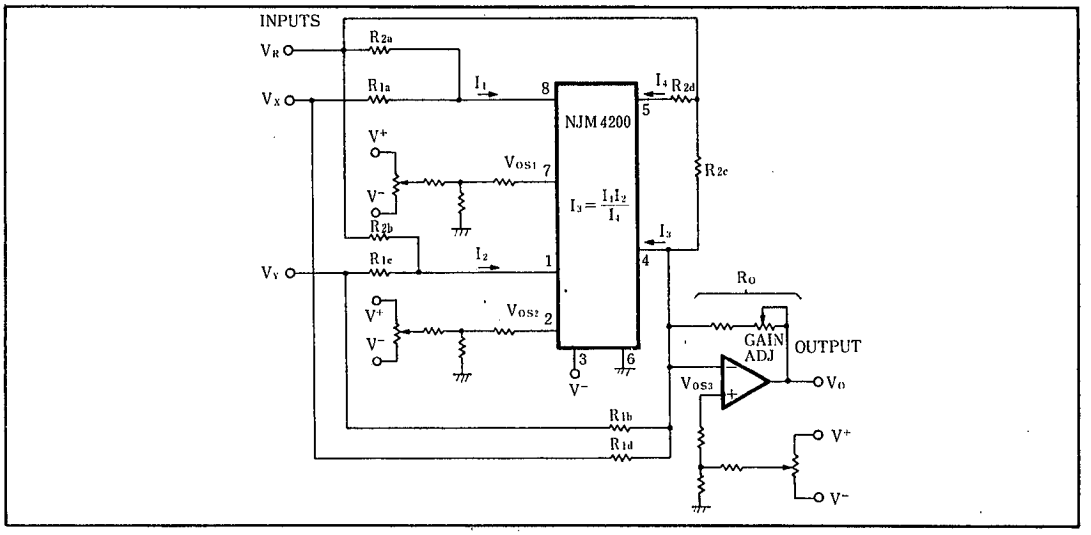


Figure 3. Four-Quadrant, General-Purpose Multiplier with Offset Adjustments

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Resistor Matching

Assuming no op amp offsets and no error due to the multiplier chip, then the output would be the sum of the items given below:

$$\text{Desired Output} = \frac{R_0 R_{2d}}{R_{1a} R_{1c}} \frac{V_X V_Y}{V_R} \qquad V_Y \text{ Feedthrough} = \frac{R_0}{R_{1c}} \left(\frac{R_{2d}}{R_{2a}} - \frac{R_{1c}}{R_{1b}} \right) V_Y$$

$$V_X \text{ Feedthrough} = \frac{R_0}{R_{1a}} \left(\frac{R_{2d}}{R_{2b}} - \frac{R_{1a}}{R_{1d}} \right) V_X \qquad \text{Output Offset} = \frac{R_0}{R_{2a}} \left(\frac{R_{2d}}{R_{2b}} - \frac{R_{2a}}{R_{2c}} \right) V_R^2$$

The AC feedthrough is directly proportional to the matching of the R_2 resistor set and the R_1 resistor set. AC feedthrough on the X or Y input is related to resistor tolerance as:

$$\text{AC Feedthrough} \sim R_0/R_1 \times 2 \times \text{Res. Tol.} \times V_{IN}$$

For example, if R_0/R_1 were 1.5 as in the example given previously and the resistors were matched to within 1%, then the maximum AC feedthrough due to resistor mismatch would be 3% of the V_X or V_Y input voltage. This AC feedthrough can be nulled directly by trimming the resistor sets or indirectly by trimming offsets.

Effect of Op Amp Offsets

In a multiplier, the offsets are cross multiplied and can thus cause AC feedthrough. When one input is zero and the other is a large AC signal, then the output will be the offset of the "zero" input times the AC signal. To quantify this effect, consider the circuit as shown in Figure 3. The offsets of each amplifier are due to both input offset voltage for the op amp and the input offset current times the source resistance.

These offsets can be lumped together into a single V_{OS} term. For this analysis, assume that the external resistors are perfectly matched (R_1's and R_2's all matched). The set of equations below must be combined to see their interaction:

$$I_1=\frac{V_X-V_{OS1}}{R_1}+\frac{V_R-V_{OS1}}{R_2}$$

$$I_2=\frac{V_Y-V_{OS2}}{R_1}+\frac{V_R-V_{OS2}}{R_2}$$

$$I_3=\frac{V_X-V_{OS3}}{R_1}+\frac{V_Y-V_{OS3}}{R_1}+\frac{V_R-V_{OS3}}{R_2}+\frac{V_0-V_{OS3}}{R_0}$$

$$I_4=\frac{V_R-V_{OS4}}{R_2} \qquad I_3=\frac{I_1 I_2}{I_4}$$

$$\text{Desired Output}=\frac{R_0 R_2}{R_1^2}\frac{V_X V_Y}{V_R}$$

$$V_Y \text{ Feedthrough}=\frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4}-\left(\frac{R_2}{R_1}+1\right)V_{OS1}\right]V_Y$$

$$V_X \text{ Feedthrough}=\frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4}-\left(\frac{R_2}{R_1}+1\right)V_{OS2}\right]V_X$$

$$\text{Output Offset}=\left(\frac{2R_0}{R_1}+\frac{R_0}{R_2}+1\right)V_{OS3}-\left(\frac{R_0}{R_1}+\frac{R_0}{R_2}\right)(V_{OS1}+V_{OS2})$$

For simplicity, V_{OS}^2 terms and gain-error factors on error terms can be dropped. The output voltage would then be the sum of the terms given above:

To estimate magnitudes, consider the previous example where R_0=150kΩ,R_1 and R_2 were 100kΩ, and V_R=15V. Then,

V_Y Feedthrough=1/10($V_{OS4}-2V_{OS1}$)V_Y

V_X Feedthrough =1/10($V_{OS4}-2V_{OS2}$)V_X

Output Offset=5.5$V_{OS3}-3(V_{OS1}+V_{OS2})$

To carry this example further, let each V_{OS} term have a maximum value of ±10mV. The worst-case combination would then be a feedthrough of 0.003V_Y and 0.003V_X. Output offset could be as high as 115mV, but would generally be less.

The trimming procedure is straight-forward when done in the following recommended sequence.

1. Apply a full-scale AC voltage To V_Y and make V_X zero. Trim V_{OS1} for output null (V_O=0).
2. Apply the same full scale AC voltage to V_X and V_Y zero. Trim V_{OS2} for output null (V_O=0).
3. Apply zero to both inputs(V_X=0 and V_Y=0). Trim V_{OS3} for output null (V_O=0).
4. Adjust scale factor with R_0. Always adjust the input offsets before setting the scale factor.

In most application, the offset adjustments are used to compensate for the R_1 and R_2 resistor network mismatch as well as the op amp offsets. Thus, the range of offset adjustment is usually chosen to encompass both error terms. For example, the V_Y feedthrough is:

$$\left\{\frac{R_0}{R_1}\left(\frac{R_{2a}}{R_{2b}}-\frac{R_{1a}}{R_{1b}}\right)+\frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4}-\left(\frac{R_2}{R_1}+1\right)V_{OS1}\right]\right\}V_Y$$

Varying V_{OS1} over sufficient range can compensate for both offset and resistor mismatch.

One Quadrant Divider

Division is very easily implemented with the NJM4200 multiplier when the inputs are all positive. The circuit for one-quant division is shown in Figure 4. The inputs V_X, V_Z, and V_R must be positive and the input currents I_1, I_2 and I_4 must be restricted in range. Within the rated range, I_1 I_2 will equal I_3 I_4 and therefore:

$$\left(\frac{V_X}{R_1}\right)\times\left(\frac{V_R}{R_2}\right)=\left(\frac{V_0}{R_0}\right)\times\left(\frac{V_Z}{R_4}\right)$$

$$V_0=\frac{R_0 R_4}{R_1 R_2}V_R\frac{V_X}{V_Z}$$

The reference input V_R is generally fixed and the ratio of R_0R_4/R_1R_2 is usually chosen to make V_O=10V at the maximum value of V_X/V_Z. For example, if V_R=6.2V and V_X/V_Z maximum is one, then choose R_0R_4/R_1R_2 of 10/6.2 which is 1.613. The output would then be:

$$V_0=10\frac{V_X}{V_Z},\quad \text{where}\ \frac{V_X}{V_Z}\leqq 1$$

As with the four-quadrant multiplier circuit, op amp offsets cross-multiply with the inputs.

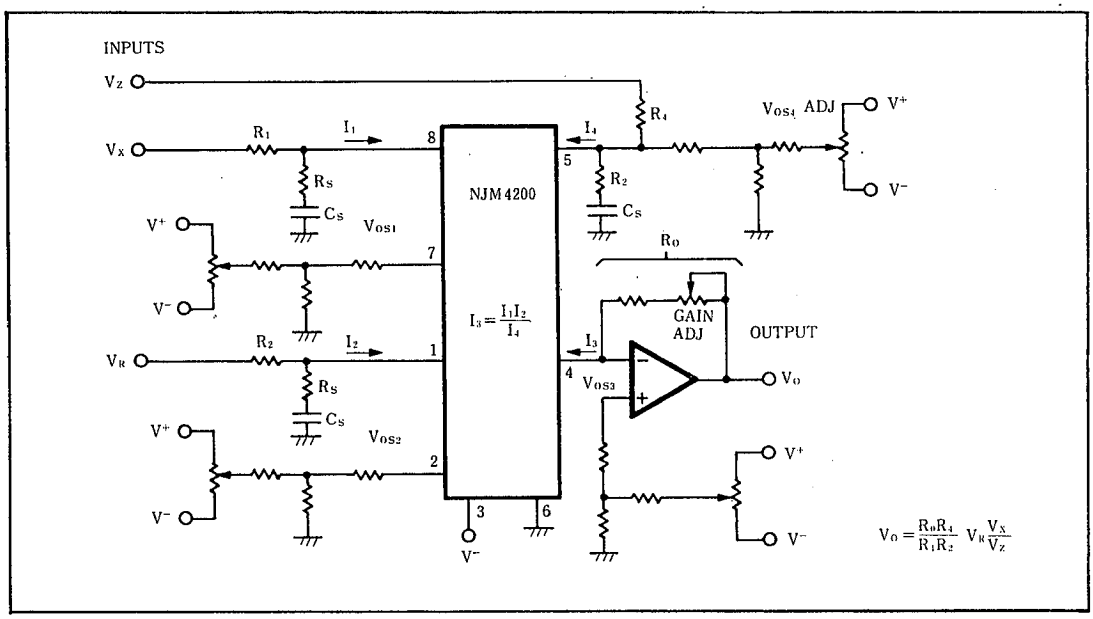


Figure 4. One-Quadrant Divider

These offsets should be nulled to obtain best accuracy. The output voltage with offsets considered, but neglecting V_{OS}^2 terms, is given by:

Ideal Error Terms

$$V_0=\overbrace{\frac{R_4R_0}{R_1R_2}V_R\frac{V_X}{V_Z}}+\overbrace{\frac{R_4R_0}{R_1R_2}\left[\frac{V_RV_X}{V_Z^2}V_{OS4}-\frac{V_X}{V_Z}V_{OS2}-\frac{V_R}{V_Z}V_{OS1}\right]+V_{OS3}}$$

Because the offsets and signals are interactive, the recommended procedure for adjustment is the following:

1. Monitor the offsets at pins (8) and (1) directly and adjust V_{OS1}, V_{OS2} to null them. This removes the V_{OS1} and V_{OS2} error terms.
2. Make $V_X=V_Z$ and sweep over their full dynamic range. The output should be constant; vary the V_{OS4} ADJ pot for a constant output of $R_4R_0\ V_R/R_1R_2$ plus V_{OS3}.
3. Apply the minimum value of V_X/V_Z and adjust V_{OS3} to obtain the proper V_0.
4. Apply the maximum value of V_X/V_Z and adjust R_0 for proper V_0.

The accuracy will be limited only by the nonlinearity, which for the NJM4200 is very small.

Square-Rooting

The circuit for implementing the square-rooting function is shown in Figure 5. An input voltage V_X multiplied by a reference voltage V_R is made equal to the square of the output voltage. The relationship $I_1I_2=I_3I_4$ becomes:

$$\frac{V_XV_R}{R_1R_2}=\frac{V_0^2}{R_0R_4}$$

The input voltage must be positive. Scaling is determined by the external resistor network and reference voltage V_R. The output voltage is given by:

$$V_0=\sqrt{\frac{R_0R_4}{R_1R_2}V_RV_X}$$

In most applications, the resistors should be comparable in value and V_R should be in the range of 5V to 15V. A scale factor of 10 is very convenient and provides an output range of 0.3V to 10V for an input range of 10mV to 10V. In equation form:

$$V_0=\sqrt{10V_X},\quad 10mV<V_X<10V$$

The offsets can be externally trimmed as needed. The nonlinear nature of the square-rooting function makes the error due to offsets very small for large inputs and very large at low input levels. With offsets included, the output voltage is:

$$V_0=\left[\frac{R_0R_4}{R_1R_2}V_R\left(1-\frac{V_{OS2}}{V_R}\right)V_X-\frac{R_0R_4}{R_1R_2}V_RV_{OS1}+V_0(V_{OS3}+V_{OS4})\right]^{1/2}$$

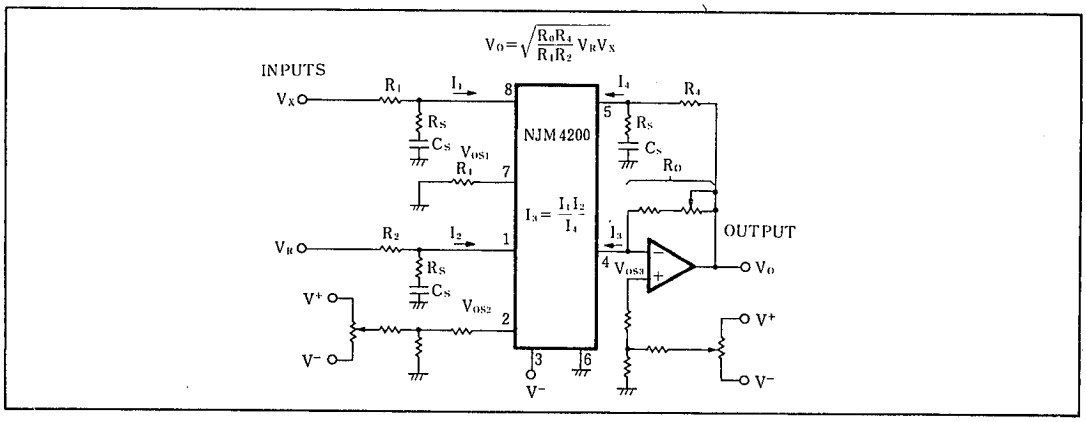


Figure 5. Square-Rooting Circuit

The term V_{OS2}/V_R affects gain only and is constant, therefore varying Ro can compensate for the V_{OS2} error term. The effect of V_{OS3} and V_{OS4} is additive and only one of these offsets are advisable to be adjusted. The V_{OS1} term should be trimmed to zero. The recommended trimming sequence is as follows:

1. Adjust V_{OS3} to zero directly by monitoring pin(4).
2. Apply minimum value of V_X and adjust V_{OS1} for correct V_0.
3. Apply maximum value of V_X and adjust R_0 for correct V_0.

The square-rooting circuit can easily be designed for overall accuracy of ±0.2% when using the NJM4200 IC multiplier.

RMS-to-DC Converter

The root-mean-square value of a complex waveform can be computed directly by squaring, integrating, and then square rooting. The NJM4200 is idealy suited to this computation and the entire RMS-to-DC conversion can be implemented with a single device.

A functional diagram is shown in Figure 6. An absolute-value circuit, or precision rectifier, first converts the AC input into a rectified positive voltage. Input currents I_1 and I_2 are made equal and will be $|V_{IN}|/R_1$. The remaining input current, I_4, is made equal to V_0/R_0 plus a derivative term, $C_0 dV_0/dt$. Combining these relationships according to $I_1 I_2 = I_3 I_4$,

$$\frac{V_{IN}^2}{R_1^2} = \frac{V_0^2}{R_1^2} + C_1 \frac{dV_0}{dt} \frac{V_0}{R_1}$$

This equation is equivalent to

$$V_0^2 + \frac{R_1 C_1}{2} \frac{d}{dt}\left(V_0^2\right) = V_{IN}^2$$

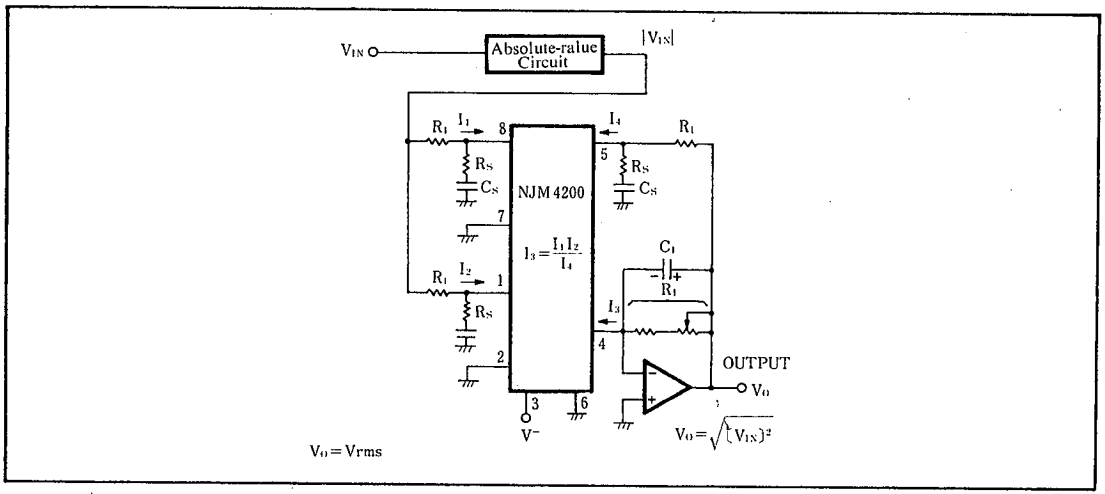


Figure 6. RMS-to-DC Converter

The output voltage squared is the exponentially-weighted average of the input-voltage squared. Square-rooting both sides of the equation, and considering the polarity constraints inherent in this implementation, gives the desired results:

$$V_0 = \sqrt{[V_{IN}(t)]^2}$$

This is the true RMS value of V_{IN} within the frequency range where the averaging time constant $R_1C_1/2$ is of sufficient magnitude for low-pass filtering. Capacitor C_1 must be large enough in value to adequately average the signal at its minimum frequency.

Various practical considerations limit performance for very small input signals, so this circuit is usually designed for a specific input voltage range. As with the divide and squre-root modes of operation, the NJM4200 may require a stabilizing R_SC_S at the input summing junctions (pins 8, 1, and 5).

The specific component values and external adjustments needed depends on the particular application.

Design Considerations

Frequency Response and Stability

The op amps within the NJM4200 multiplier are stabilized for optimum performance in the four-quadrant multiplier configuration. At extremes of input current, the stability becomes marginal and external phase compensation may be required. The possibility of undesired oscillations should be considered for input currents of less than 50μA or greater than 500μA. Dividing and square-rooting operations often require a wide dynamic range on the input currents.

Two techniques are very helpful for assuring frequency stability and minimizing noise under a wide range of conditions:

1. Connect a series $R_S C_S$ from input summing junction to ground as shown in Figure 7. This network has the effect of attenuating the feedback at high frequencies and thereby stabilizing the op amp. Loop gain at high frequencies is sacrificed, but this is seldom of concern in dividing or square-rooting applications. Recommended values are 10kΩ for R_S and 0.005μF for C_S
2. The resistor on the noninverting input can be bypassed as shown in Figure 7. This helps to reduce noise.

The need for these frequency compensating techniques will depend on the application, particularly the input current range and input signal characteristics.

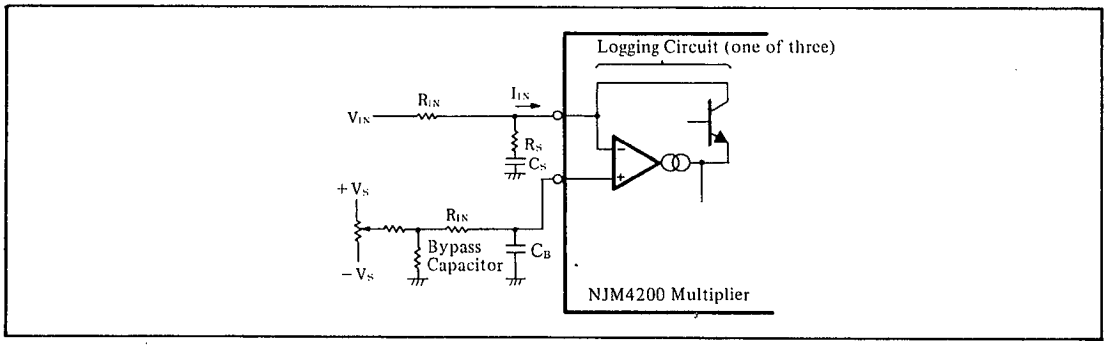


Figure 7. Optional Frequency Stability Components R_S,C_S and C_B

Gain Stability

This type of multiplier is very sensitive to temperature gradients across the transistor quad (Q_1 to Q_4 and Q_2 to Q_3). The ambient temperature tends to affect offsets, but temperature gradients will cause a gain error. Several steps can be taken to minimize this effect:

1. Keep the multiplier physically remote from power dissipating components.
2. When using printed-circuit boards, make pad sizes and layout pattern as symmetrical as possible.
3. Head sinking or epoxy potting can be used if necessary. This will tend to prevent rapid changes in temperature gradient.

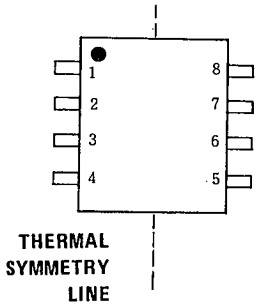
Power drain within the multiplier chip itself is relatively low, therefore the gain stability can be very good if the IC is not exposed to temperature gradients.

Offset Stability

Input offset voltage of the op amps can be easily trimmed if desired. The effects of input bias current drift can be minimized by making the impedance approximately equal on the inverting and noninverting inputs. The equivalent input offset will then depend only on the difference in bias currents rather than the absolute values.

■ THERMAL SYMMETRY

The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that sources generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.



MEMO