

Structure : Silicon Monolithic Integrated Circuit
 Product Name : Power Driver For DVD Players

Device Name : **BA5956FM**

Features :

- 2CHs for current driving-type BTL drivers to drive two-axis actuators
- 1CH for a voltage driving-type BTL driver for a feed motor
- 1CH for a voltage driving-type BTL driver for a loading motor
- 1CH for a voltage driving-type BTL driver for a spindle motor
- Use of the HSOP-M36 power package achieves downsizing of the set.
- A wide dynamic range
- A built-in thermal shutdown circuit installed.
- A built-in mute circuit installed. (This circuit can mute the outputs of the drivers except for those for loading motors.)
- The power supplies for PreVcc, the actuator part, the loading part, and PowVcc of the feed motor part/spindle motor part are provided independently to achieve an efficient drive.

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	PreVcc , PowVcc	18	V
Power Dissipation	Pd	2.2 ^{*1}	W
Maximum Output Current	Iomax	1 ^{*2}	A
Operating Temperature Range	Topr	-35 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

*1 When mounted on the glass/epoxy board with the size: 70 mm×70 mm, the thickness: 1.6 mm, and the rate of copper foil occupancy area: 3% or less.

Over Ta=25°C, derating at the rate of 17.6mW/°C.

*2 The power dissipation should be specified within the ASO range.

○ RECOMMENDED OPERATING CONDITIONS

(To determine a power supply voltage, the power dissipation must be taken into consideration.)

PreVcc	4.5 to 14 (V)
PowVcc	4.5 to PreVcc (V)

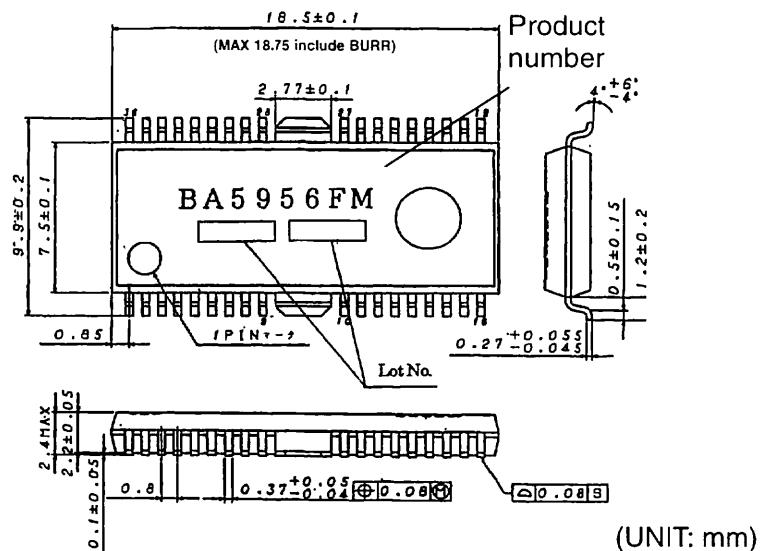
This product has not been checked for the strategic materials (or service) defined in the Foreign Exchange and Foreign Trade Control Law of Japan so that a verification work is required before exporting it.

Not designed for radiation resistance.

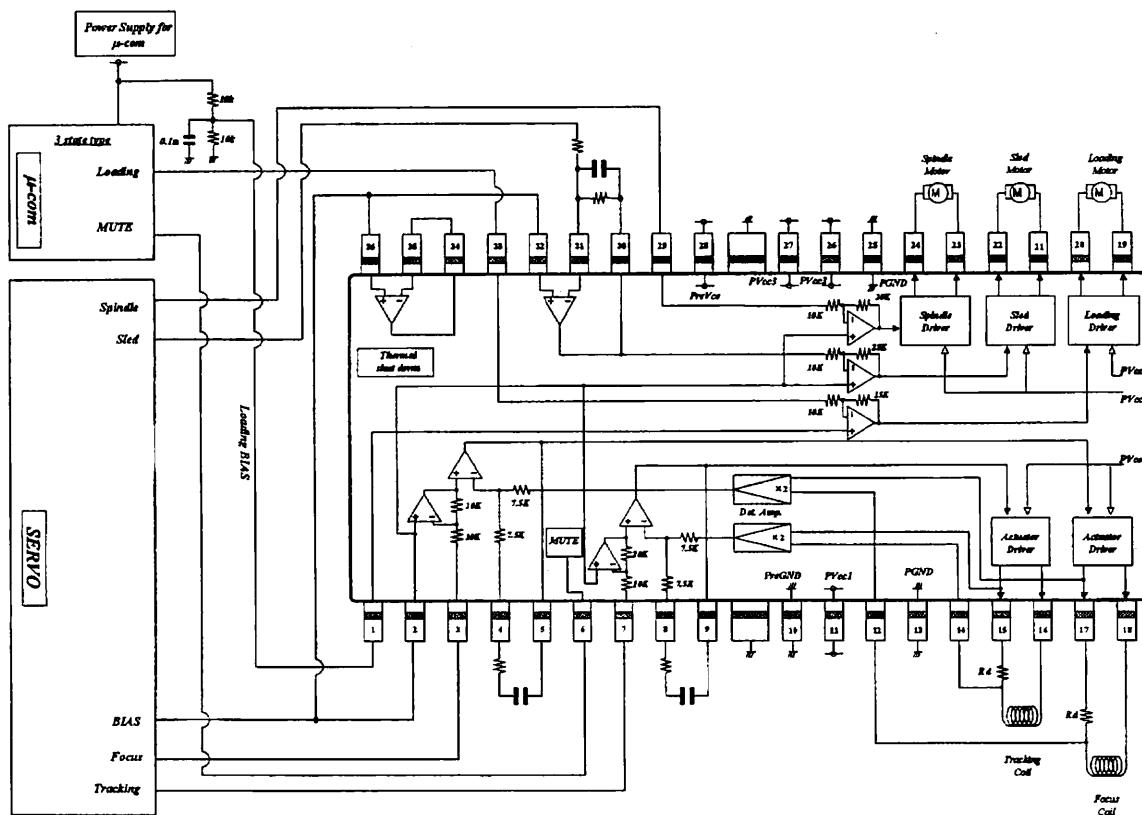
- ELECTRIC CHARACTERISTICS (Ta=25°C, PreVcc=PowVcc3=12V, PowVcc1=PowVcc2=5V, BIAS=1.65V, RL=8Ω, Rd=0.5Ω, C=100pF, unless otherwise noted.)

Parameter	Symbol	MIN	TYP	MAX	Unit	Condition
Consumption Current (at no signal)	IQ	-	34	44	mA	No load applied
Mute ON Voltage	VMON	0	-	0.5	V	
Mute OFF Voltage	VMOFF	2.0	-	-	V	
<Actuator Driver>						
Output Offset Current	IOOF	-6	0	6	mA	
Maximum Output Amplitude	VOM	3.6	4.0	-	V	VIN=±1.65V
Transfer Gain	Gvc	1.5	1.8	2.1	A/V	VIN=BIAS±0.2V
<Feed Motor Driver>						
Input Op-amp Common Mode Input Range	VICM	0.5	-	10.5	V	
Input Bias Current	IBOP	-	-	300	nA	
Low-level Output Voltage	VOLOP	-	0.2	0.5	V	
Maximum Output Source Current	ISO	0.5	-	-	mA	
Maximum Output Sink Current	ISI	0.5	-	-	mA	
Output Offset Voltage	VOOFS _L	-50	0	50	mV	
Maximum Output Amplitude	VOMSL	8.0	9.5	-	V	VIN=±1.65V
Closed Circuit Voltage Gain	GVSL	17.6	19.6	21.6	dB	VIN=±0.2V
<Loading Driver>						
Offset Voltage	VOOFL _D	-50	0	50	mV	
Maximum Output Amplitude	VOMLD	3.5	4.0	-	V	VIN=±1.65V
Voltage Gain	GVLD	15.7	17.7	19.7	dB	VIN=BIAS±0.2V
<Spindle Driver>						
Offset Voltage	VOOFS _P	-50	0	50	mV	
Maximum Output Amplitude	VOMS	8.0	9.5	-	V	VIN=±1.65V
Voltage Gain	GVSP	15.7	17.7	19.7	dB	VIN=BIAS±0.2V

OUTLINE DIMENSIONS, SYMBOLS



○ APPLICATION CIRCUIT DIAGRAM



Resistance unit: [Ω]

○ PIN NUMBERS, PIN NAMES

No	Pin Name	Description	No	Pin Name	Description
1	LDBIAS	Loading unit bias input	19	VOLD(-)	Loading driver output (-)
2	BIAS	Bias input	20	VOLD(+)	Loading driver output (+)
3	FCIN	Focus driver input	21	VOSL(-)	Sled driver output (-)
4	CFCerr1	Capacitor connection terminal 1 for error amp filter	22	VOSL(+)	Sled driver output (+)
5	CFCerr2	Capacitor connection terminal 2 for error amp filter	23	VOSP(-)	Spindle driver output (-)
6	MUTE	Mute terminal	24	VOSP(+)	Spindle driver output (+)
7	TKIN	Tracking driver input	25	PGND2	Power GND2
8	CTKerr1	Capacitor connection terminal 1 for error amp filter	26	PVcc2	Power Vcc2
9	CTKerr2	Capacitor connection terminal 2 for error amp filter	27	PVcc3	Power Vcc3
10	PreGND	Pre GND	28	PreVcc	Pre Vcc
11	PVcc1	Power Vcc1	29	SPIN	Spindle driver input
12	VNFFC	Focus driver feedback terminal	30	OPOUTSL	Sled pre-stage amp output terminal
13	PGND1	Power GND1	31	OPINSL(-)	Sled pre-stage amp inverted input terminal
14	VNFTK	Tracking driver feedback terminal	32	OPINSL(+)	Sled pre-stage amp non-inverted input terminal
15	VOTK(-)	Tracking driver output (-)	33	LDIN	Loading driver input
16	VOTK(+)	Tracking driver output (+)	34	OPOUT	OP-amp output terminal
17	VOFC(-)	Focus driver output (-)	35	OPIN(-)	OP-amp inverted input terminal
18	VOFC(+)	Focus driver output (+)	36	OPIN(+)	OP-amp non-inverted input terminal

Notes: The polarity signs shown in the output terminal names indicate the polarities when corresponding input pins are set to (+).

○ CAUTIONS ON USE

- (1) Setting the voltage on the Mute terminal to open or 0.5V or less will activate a mute function for the CH1, 2, 4, and 5.
Under conditions of normal use, the Mute terminal should be pulled-up to 2.0V or above.
- (2) When the power supply voltage drops to 3.5V (Typ.) or less, the mute function will be activated and, when recovering to 3.7V (Typ.) or above, the circuit will startup again.
- (3) On the Bias terminal (pin 1, 2), the applied voltage of 1.0V (Typ.) or less will activate a mute function.
Under conditions of normal use, it should be set to 1.2V or above.
- (4) Connecting a capacitive load to the OP-AMP output results in a phase margin reduction of the amp and may cause an oscillation or a peak. When connecting a capacitive load, a resistance must be inserted in series between the output and the capacitive load. And after careful consideration of the frequency characteristics, the device should be used within the range where no problem is found in actual use.
- (5) The radiating fin must be connected to the external GND.
- (6) Short-circuit between output pin -VCC (supply fault), output pin-GND (ground fault), or output terminals (load short) must be avoided. Placing ICs in wrong orientations may damage the ICs or produce smoke.
- (7) Basically, applying a voltage below the IC sub-potential to any terminals must be avoided.
Due to a counter electromotive force of the load, if the output on each driver has dropped to the IC sub-potential (GND) or less, an operation margin must be considered and examined.
- (8) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.
- (9) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.
- (10) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.
- (11) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.
- (12) About operations in a strong electric field
When used in a strong electric field, note that a malfunction may occur.
- (13) ASO
When using this IC, the output Tr must be set not to exceed the values specified in the absolute maximum ratings and ASO.
- (14) Thermal shutdown circuit
This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open.
The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.
Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

- (15) About earth wiring patterns

When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being

affected by a voltage change caused by the resistance of the pattern wiring and the large current. Make sure that the GND wiring patterns of the external components will not change, too.

(16) This IC is a monolithic IC which has a P⁺ isolations and P substrate to isolate elements each other. This P layer and an N layer in each element form a PN junction to construct various parasitic elements. Due to the IC structure, the parasitic elements are inevitably created by the potential relationship. Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage. Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than the ground level (GND, P substrate) to the input terminals. In addition, do not apply the voltage to input terminals without applying the power supply voltage to the IC. Also while applying the power supply voltage, the voltage of each input terminal must not be over the power supply voltage, or within the guaranteed values in the electric characteristics.

<Supplemental Remarks>

Current feedback driver

The transfer gain (output current / input current) can be determined by the following equation:

$$g_m = \frac{1}{R_d + R_{WIRE}} \text{ (A/V)}$$

Where R_{WIRE} represents a gold wire resistance inside the package, measuring approximately 0.075Ω (±0.05Ω) (Typ.)

Appendix

Notes

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(Contact address for overseas customers in Japan)

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