

MAC15M, MAC15N

Preferred Device

Triacs

Silicon Bidirectional Thyristors

Designed for high performance full-wave AC control applications where high noise immunity and high commutating di/dt are required.

Features

- Blocking Voltage to 800 Volts
- On-State Current Rating of 15 Amperes RMS at 80°C
- Uniform Gate Trigger Currents in Three Modes
- High Immunity to dv/dt – 250 V/μs minimum at 125°C
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220AB Package
- High Commutating di/dt – 9.0 A/ms minimum at 125°C
- Operational in Three Quadrants, Q1, Q2, and Q3
- Pb-Free Packages are Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (–40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) MAC15M MAC15N	V _{DRM} , V _{RRM}	600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T _C = 80°C)	I _{T(RMS)}	15	A
Peak Non-repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T _J = 125°C)	I _{TSM}	150	A
Circuit Fusing Consideration (t = 8.3 ms)	I ² t	93	A ² s
Peak Gate Power (Pulse Width ≤ 1.0 μs, T _C = 80°C)	P _{GM}	20	W
Average Gate Power (t = 8.3 ms, T _C = 80°C)	P _{G(AV)}	0.5	W
Operating Junction Temperature Range	T _J	–40 to +125	°C
Storage Temperature Range	T _{stg}	–40 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

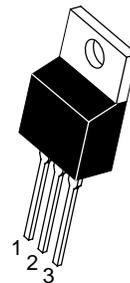
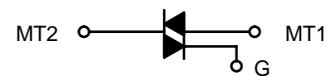
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

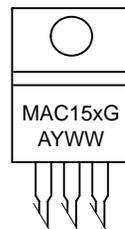
http://onsemi.com

TRIACS
15 AMPERES RMS
600 thru 800 VOLTS



TO-220AB
CASE 221A-09
STYLE 4

MARKING DIAGRAM



- x = M or N
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

PIN ASSIGNMENT

Pin	Assignment
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
MAC15M	TO-220AB	50 Units / Rail
MAC15MG	TO-220AB (Pb-Free)	50 Units / Rail
MAC15N	TO-220AB	50 Units / Rail
MAC15NG	TO-220AB (Pb-Free)	50 Units / Rail

Preferred devices are recommended choices for future use and best overall value.

MAC15M, MAC15N

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.0	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{DRM}, V_{RRM}; \text{ Gate Open}$)	I_{DRM}, I_{RRM}	-	-	0.01	mA
		-	-	2.0	

ON CHARACTERISTICS

Peak On-State Voltage (Note 2) ($I_{TM} = \pm 21 \text{ A Peak}$)	V_{TM}	-	1.2	1.6	V
Gate Trigger Current (Continuous DC) ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	I_{GT}	5.0	13	35	mA
MT2(+), G(+)		5.0	16	35	
MT2(+), G(-)		5.0	18	35	
MT2(-), G(-)					
Hold Current ($V_D = 12 \text{ Vdc}, \text{ Gate Open}, \text{ Initiating Current} = \pm 150 \text{ mA}$)	I_H	-	20	40	mA
Latching Current ($V_D = 24 \text{ V}, I_G = 35 \text{ mA}$)	I_L	-	33	50	mA
MT2(+), G(+)		-	36	80	
MT2(+), G(-)		-	33	50	
MT2(-), G(-)					
Gate Trigger Voltage ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	V_{GT}	0.5	0.75	1.5	V
MT2(+), G(+)		0.5	0.72	1.5	
MT2(+), G(-)		0.5	0.82	1.5	
MT2(-), G(-)					

DYNAMIC CHARACTERISTICS

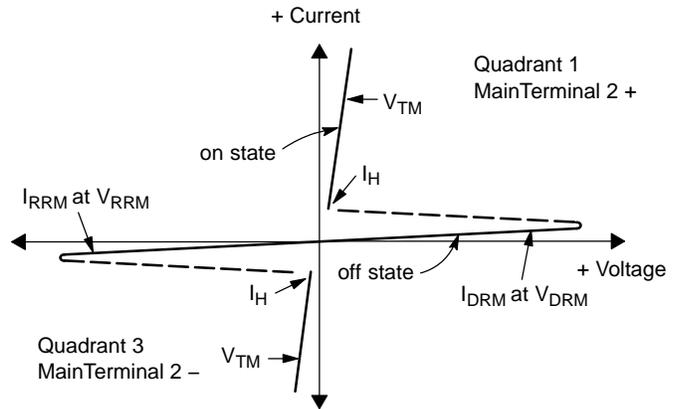
Rate of Change of Commutating Current; See Figure 10. ($V_D = 400 \text{ V}, I_{TM} = 6.0 \text{ A}, \text{ Commutating } dv/dt = 24 \text{ V}/\mu\text{s},$ Gate Open, $T_J = 125^{\circ}\text{C}, f = 250 \text{ Hz}, \text{ No Snubber}$)	$(di/dt)_C$	9.0	-	-	A/ms
Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}, \text{ Exponential Waveform}, \text{ Gate Open}, T_J = 125^{\circ}\text{C}$)	dv/dt	250	-	-	V/ μs

2. Pulse Test: Pulse Width $\leq 2.0 \text{ ms}$, Duty Cycle $\leq 2\%$.

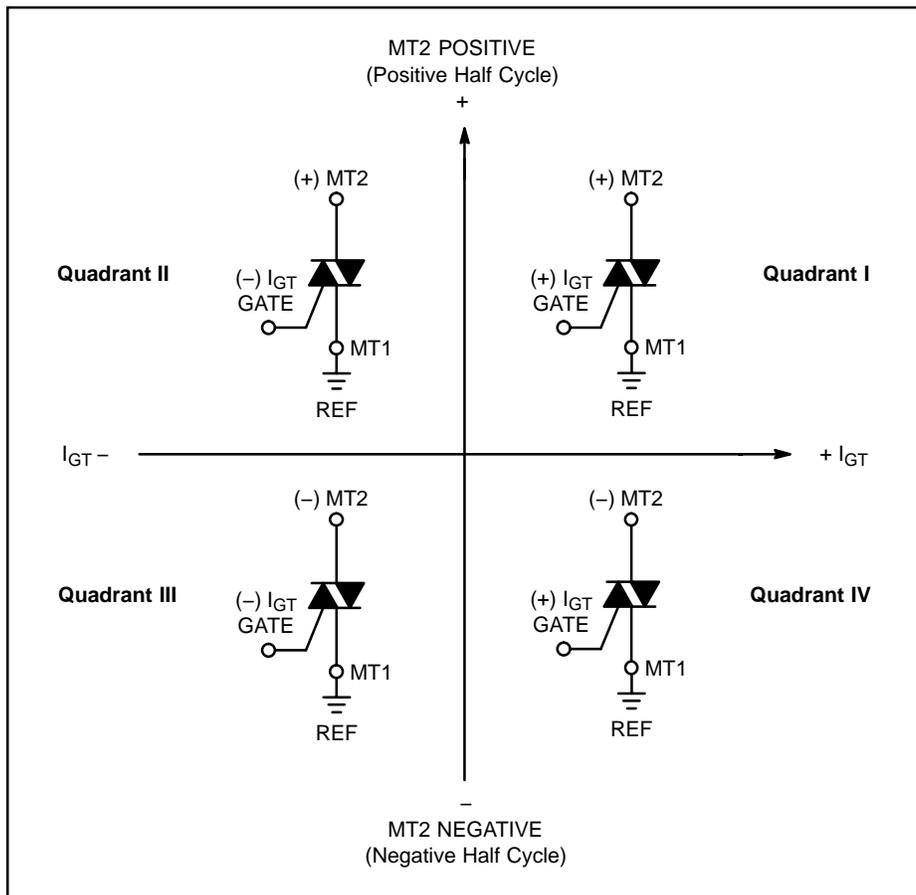
MAC15M, MAC15N

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants I and III are used.

MAC15M, MAC15N

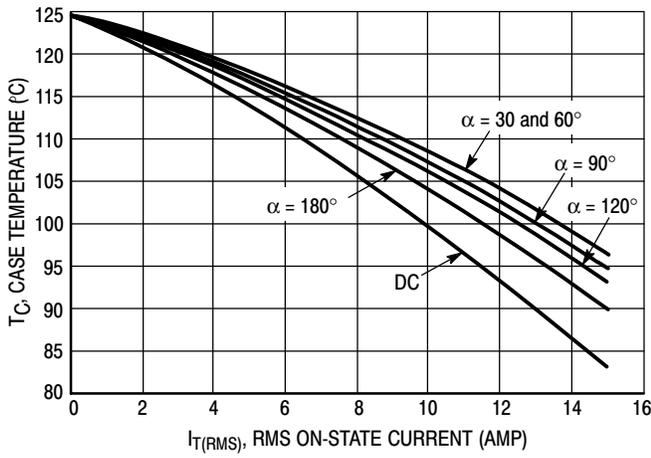


Figure 1. RMS Current Derating

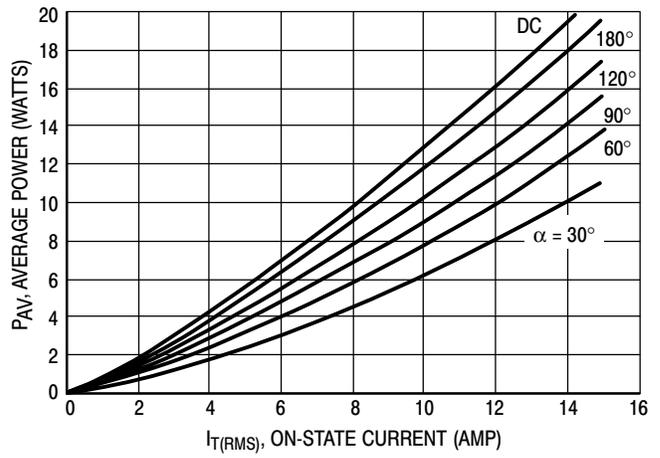


Figure 2. On-State Power Dissipation

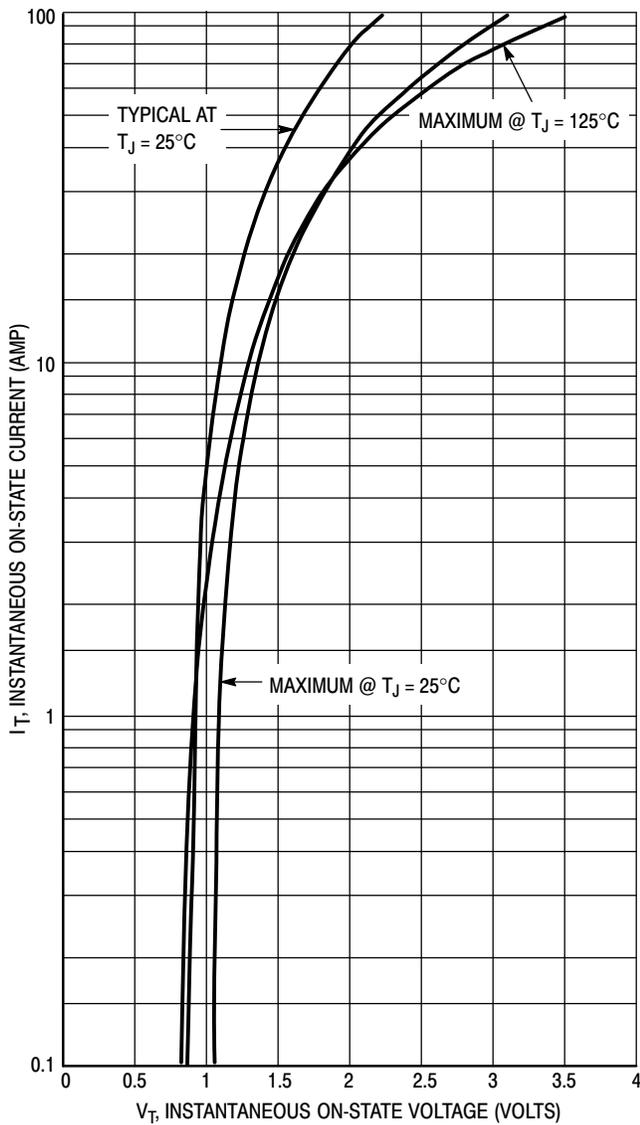


Figure 3. On-State Characteristics

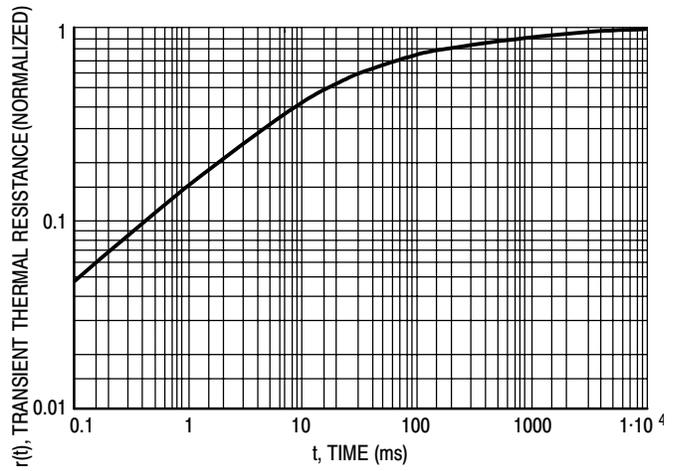


Figure 4. Transient Thermal Response

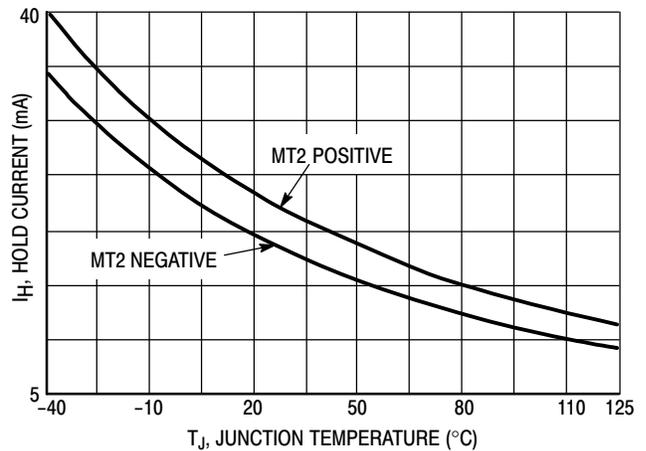


Figure 5. Hold Current Variation

MAC15M, MAC15N

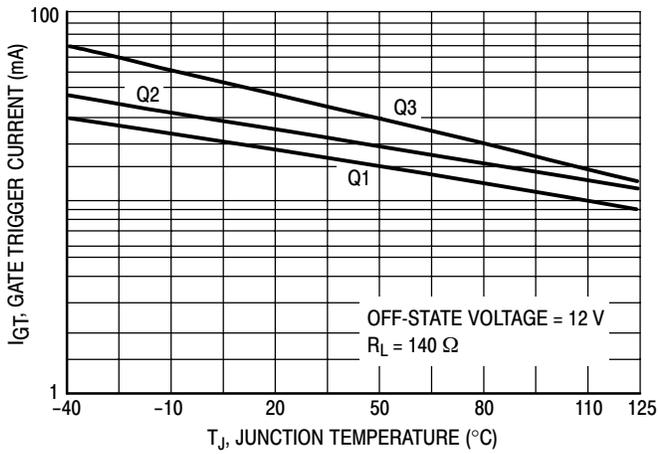


Figure 6. Typical Holding Current versus Junction Temperature

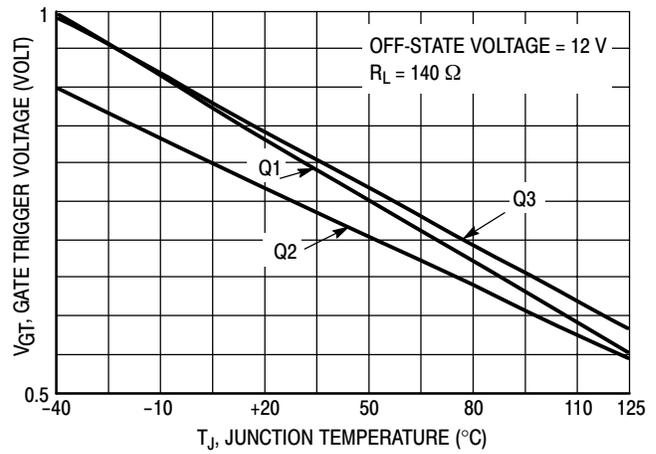


Figure 7. Gate Trigger Voltage versus Junction Temperature

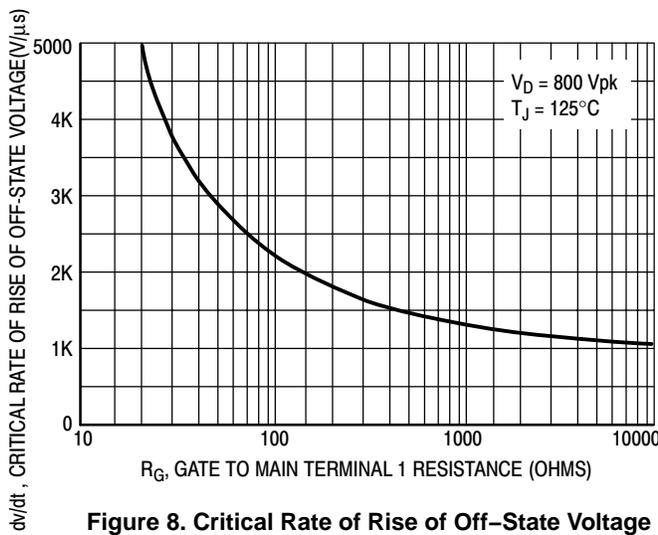


Figure 8. Critical Rate of Rise of Off-State Voltage (Exponential)

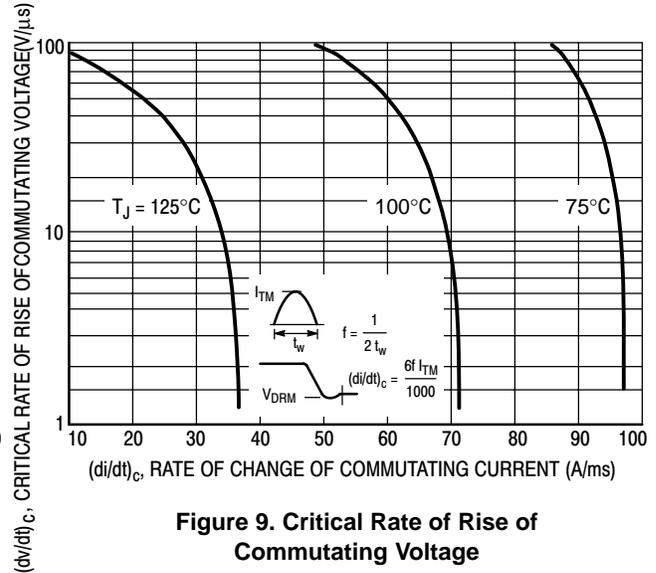
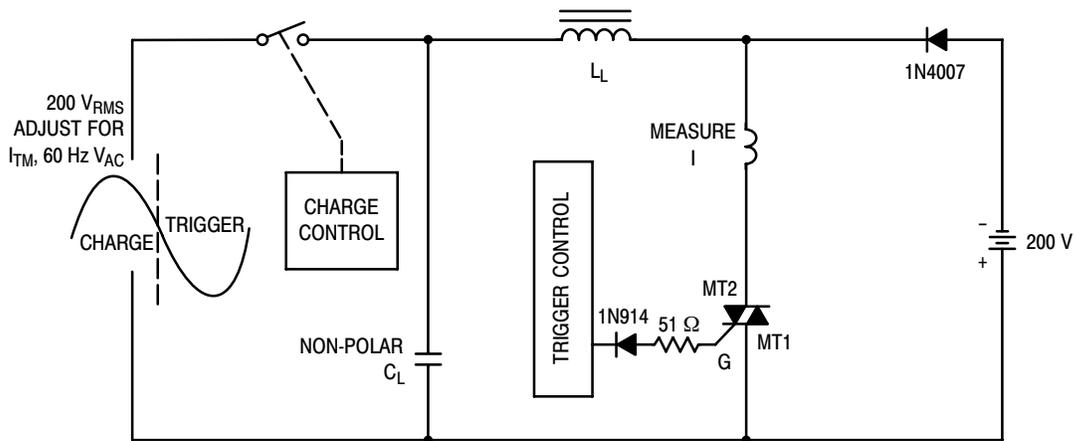


Figure 9. Critical Rate of Rise of Commutating Voltage



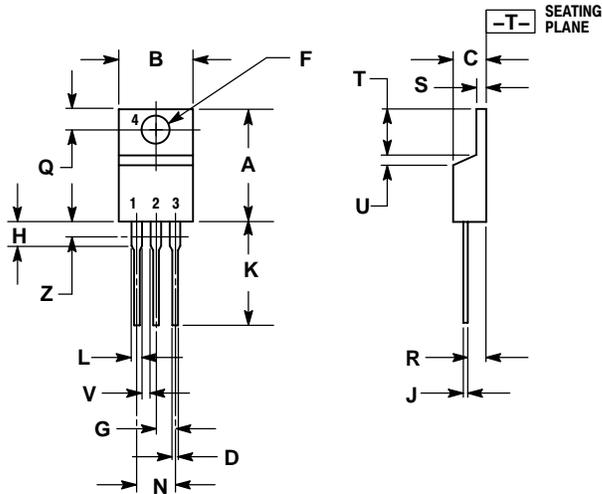
Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

Figure 10. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_c$

MAC15M, MAC15N

PACKAGE DIMENSIONS

TO-220AB
CASE 221A-09
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 4:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.