

## Product Summary

$BV_{DSS}$	$R_{DS(ON)}$	$I_D$ $T_A = +25^\circ C$
20V	0.6Ω @ $V_{GS} = 4.5V$	0.9A
	0.8Ω @ $V_{GS} = 2.5V$	0.7A
	1.0Ω @ $V_{GS} = 1.8V$	0.5A
	1.6Ω @ $V_{GS} = 1.5V$	0.3A

## Description and Applications

This MOSFET is designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

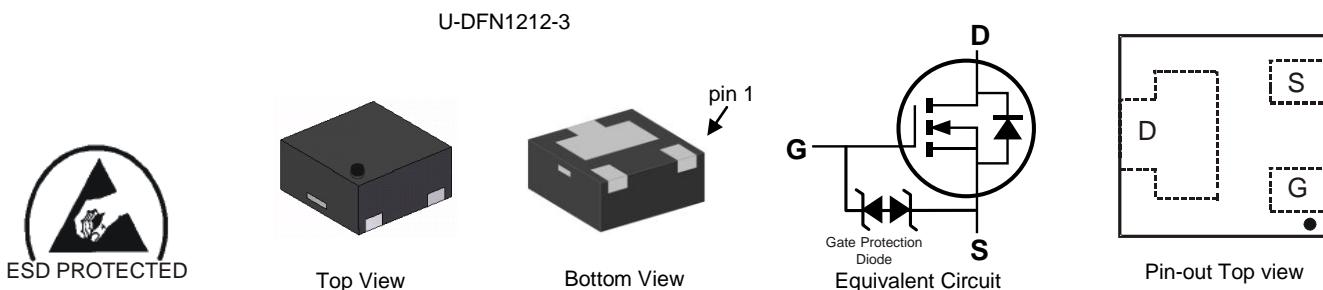
- Power Management Functions
- Battery Operated Systems and Solid-State Relays
- Load Switch

## Features and Benefits

- Low On-Resistance
- Very low Gate Threshold Voltage, 1.0V Max.
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**
- **PPAP Capable (Note 4)**

## Mechanical Data

- Case: U-DFN1212-3
- Case Material: Molded Plastic; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 
- Terminal Connections: See Diagram
- Weight: 0.005 grams (Approximate)



## Ordering Information (Note 5)

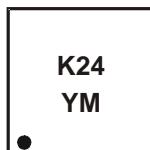
Part Number	Case	Packaging
DMN2400UFDQ-7	U-DFN1212-3	3,000/Tape & Reel
DMN2400UFDQ-13	U-DFN1212-3	10,000/Tape & Reel

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q101 qualified and are PPAP capable. Automotive, AEC-Q101 and standard products are electrically and thermally the same, except where specified. For more information, please refer to [http://www.diodes.com/quality/product\\_compliance\\_definitions/](http://www.diodes.com/quality/product_compliance_definitions/).
5. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information

U-DFN1212-3



K24 = Product Type Marking Code

YM = Date Code Marking

Y = Year (ex: C = 2015)

M = Month (ex: 9 = September)

### Date Code Key

Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
Code	C	D	E	F	G	H	I	J	K	L	M

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$  unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			$V_{DSS}$	20	V
Gate-Source Voltage			$V_{GSS}$	$\pm 12$	V
Continuous Drain Current (Note 7) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$	0.9 0.7	A
Continuous Drain Current (Note 7) $V_{GS} = 2.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	$I_D$	0.7 0.5	A
Pulsed Drain Current (10 $\mu\text{s}$ pulse, duty cycle = 1%)			$I_{DM}$	3.0	A
Maximum Body Diode Forward Current (Note 7)			$I_S$	0.8	A

**Thermal Characteristics** (@ $T_A = +25^\circ\text{C}$  unless otherwise specified.)

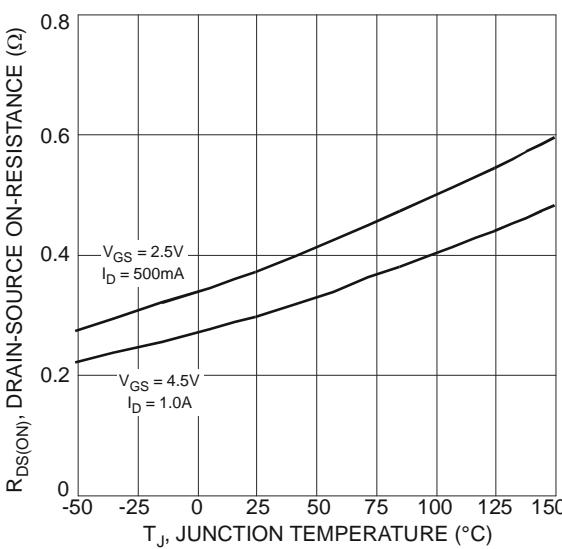
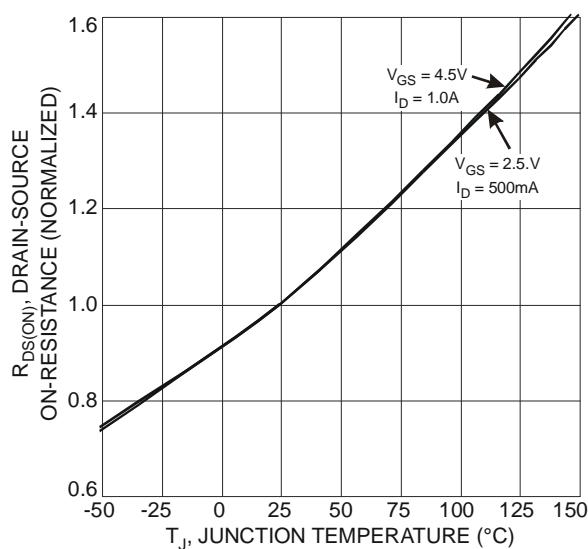
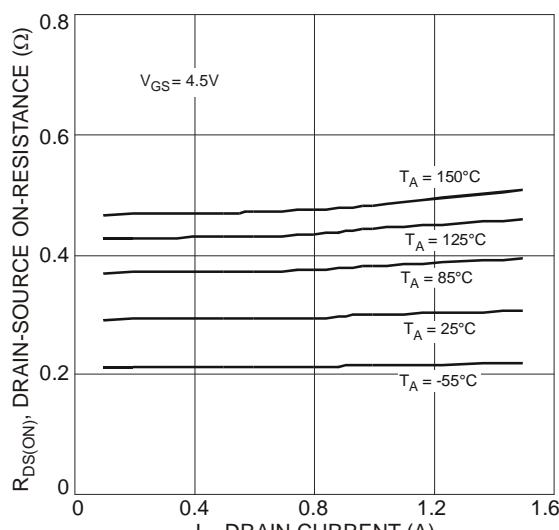
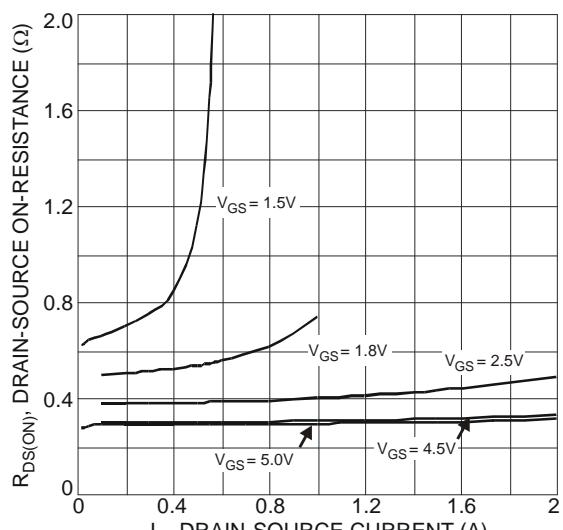
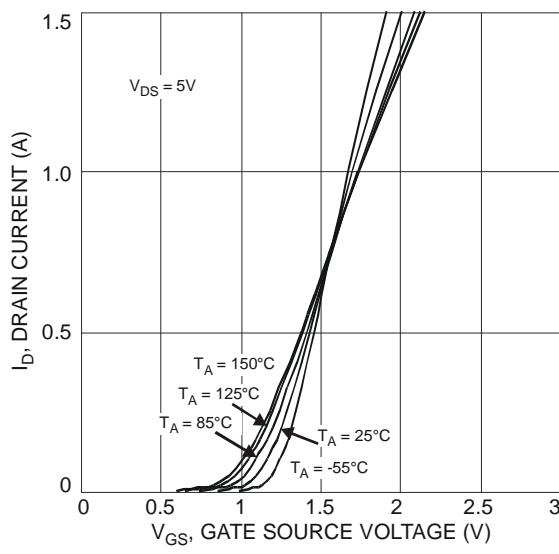
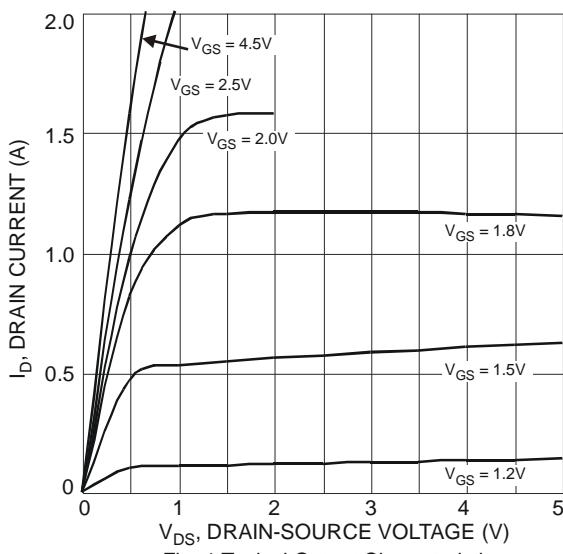
Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 6)		$P_D$	0.4	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	283	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 7)		$P_D$	0.8	W
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	$R_{\theta JA}$	147	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	112	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$  unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	20	-	-	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	$I_{DSS}$	-	-	80 100	nA	$V_{DS} = 4.5\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	-	-	$\pm 1.0$	$\mu\text{A}$	$V_{GS} = \pm 4.5\text{V}, V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	0.45	-	1.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	-	0.35	0.6	$\Omega$	$V_{GS} = 4.5\text{V}, I_D = 200\text{mA}$
		-	0.45	0.8		$V_{GS} = 2.5\text{V}, I_D = 200\text{mA}$
		-	0.6	1.0		$V_{GS} = 1.8\text{V}, I_D = 100\text{mA}$
		-	0.7	1.6		$V_{GS} = 1.5\text{V}, I_D = 50\text{mA}$
		-	-	-		-
Forward Transfer Admittance	$ Y_{IS} $	-	1.4	-	S	$V_{DS} = 3\text{V}, I_D = 200\text{mA}$
Diode Forward Voltage	$V_{SD}$	-	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 500\text{mA}$
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	$C_{iss}$	-	37.0	-	pF	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	$C_{oss}$	-	5.7	-	pF	
Reverse Transfer Capacitance	$C_{rss}$	-	4.2	-	pF	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Gate Resistance	$R_g$	-	68	-	$\Omega$	
Total Gate Charge	$Q_g$	-	0.5	-	nC	$V_{GS} = 4.5\text{V}, V_{DS} = 10\text{V}, I_D = 250\text{mA}$
Gate-Source Charge	$Q_{gs}$	-	0.07	-	nC	
Gate-Drain Charge	$Q_{gd}$	-	0.1	-	nC	$V_{DD} = 10\text{V}, V_{GS} = 4.5\text{V}, R_L = 47\Omega, R_G = 10\Omega, I_D = 200\text{mA}$
Turn-On Delay Time	$t_{D(on)}$	-	4.06	-	ns	
Turn-On Rise Time	$t_r$	-	7.28	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	13.74	-	ns	
Turn-Off Fall Time	$t_f$	-	10.54	-	ns	

Notes:

6. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1-inch square copper plate.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.



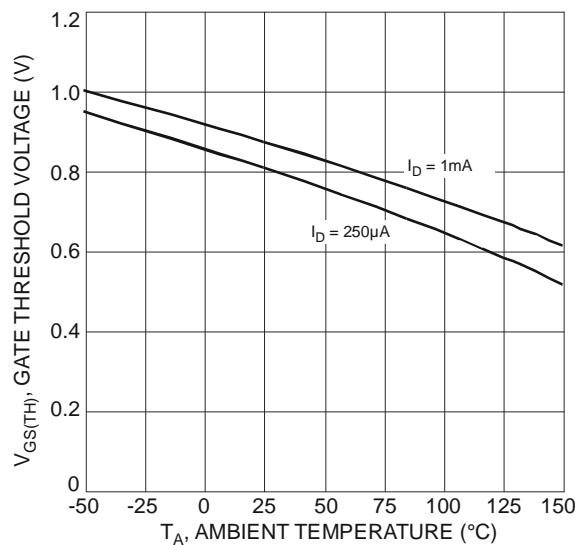


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

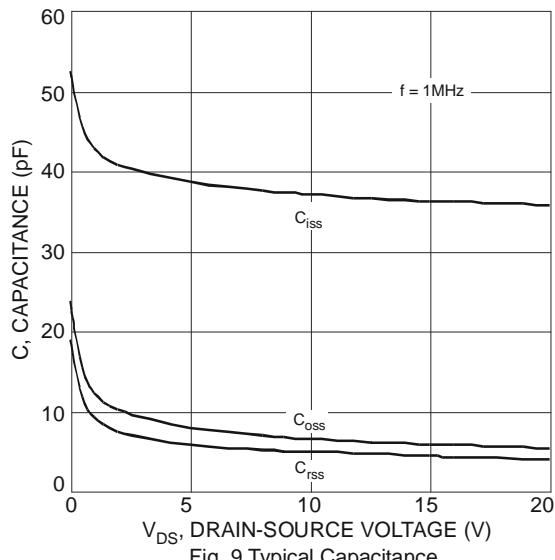


Fig. 9 Typical Capacitance

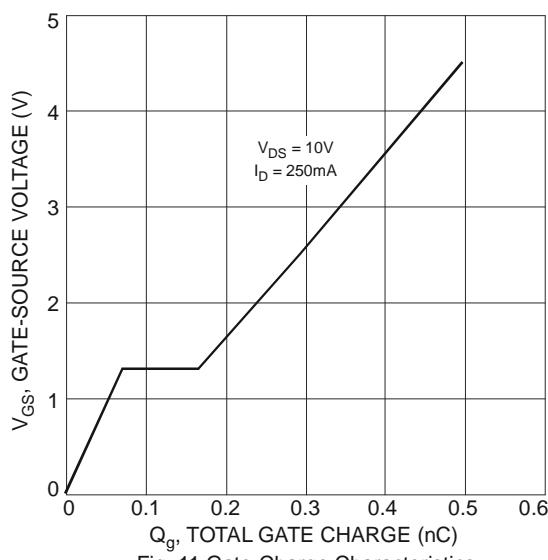


Fig. 11 Gate-Charge Characteristics

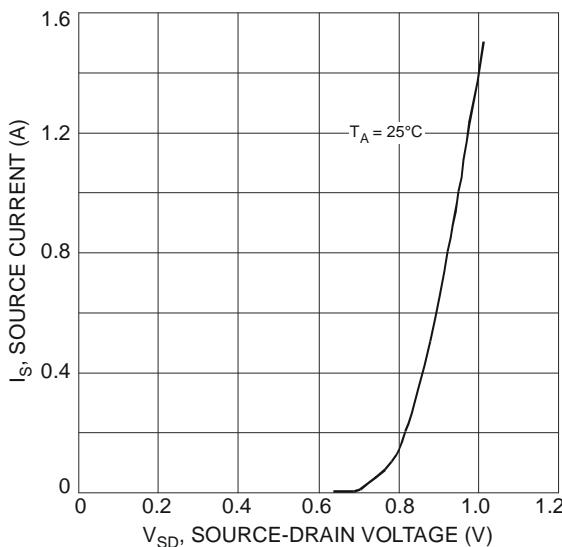


Fig. 8 Diode Forward Voltage vs. Current

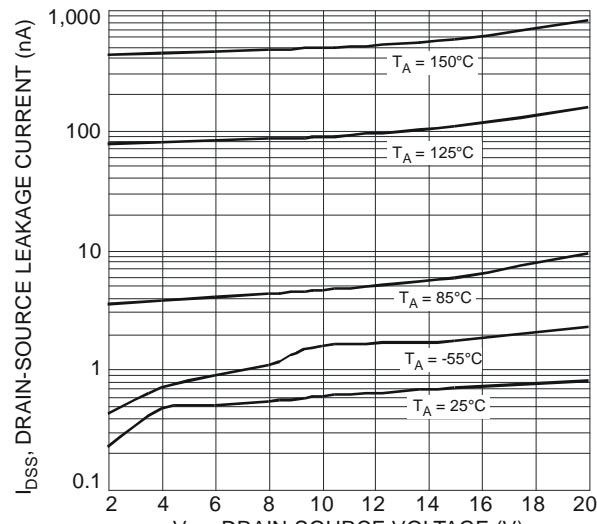


Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

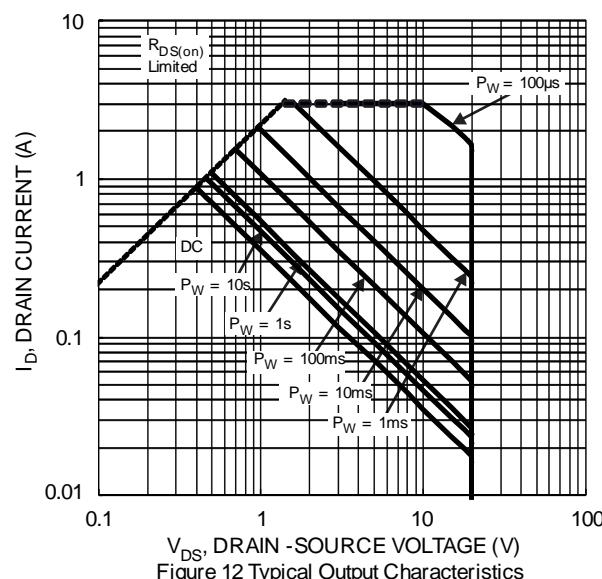


Figure 12 Typical Output Characteristics

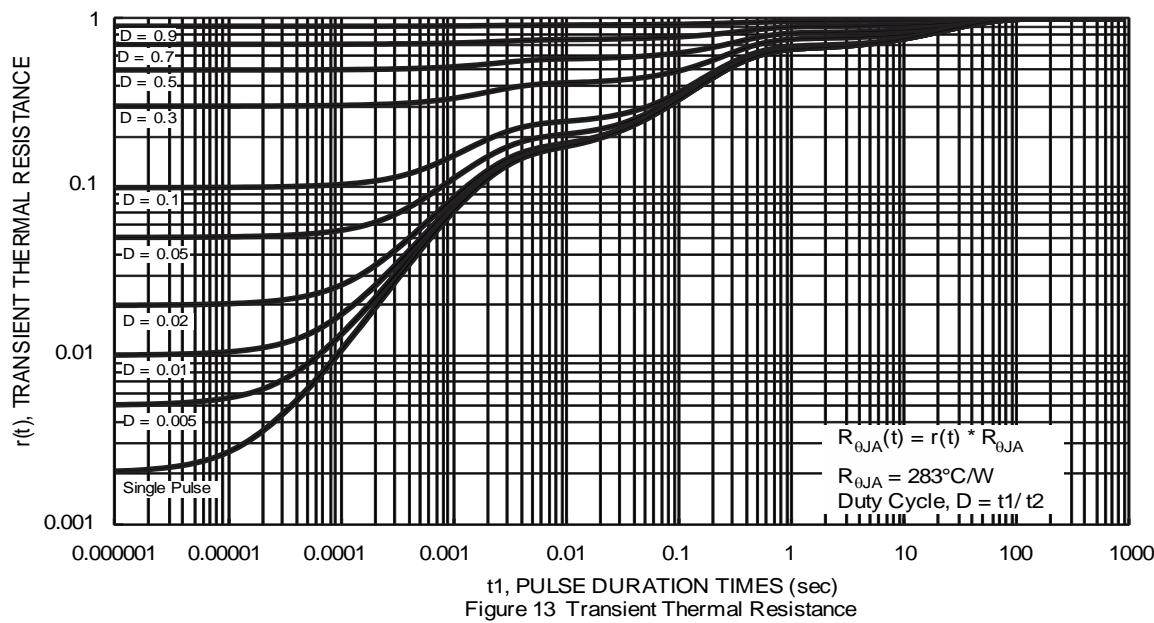
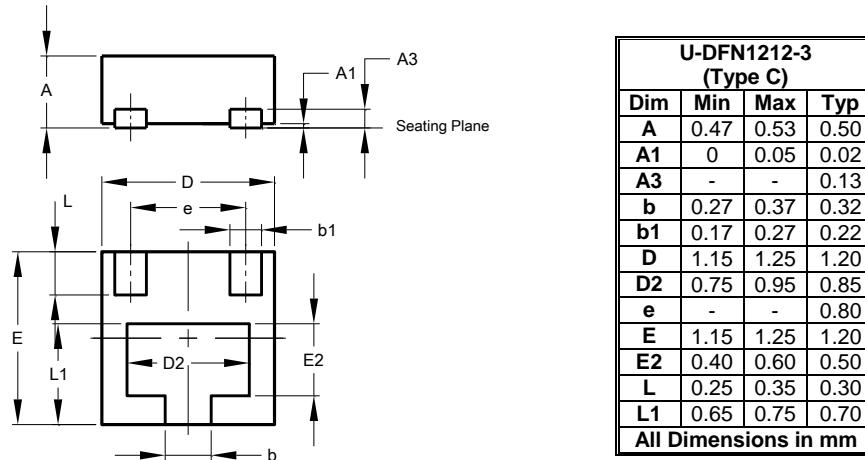


Figure 13 Transient Thermal Resistance

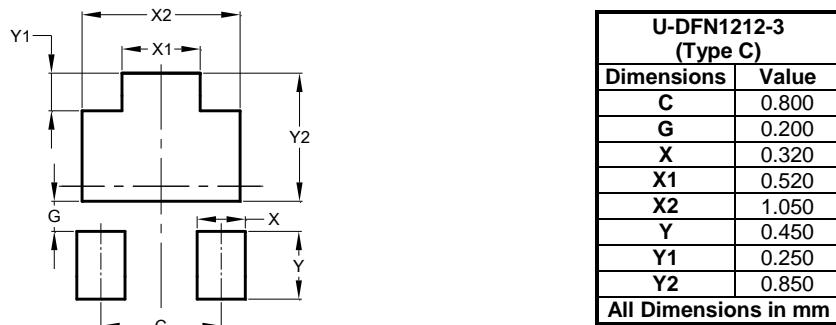
#### Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



#### Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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