

HAF1004(L), HAF1004(S)

Silicon P Channel MOS FET Series Power Switching

REJ03G0028-0500Z
(Previous ADE-208-629B (Z))
Rev.5.00
2003.04.29

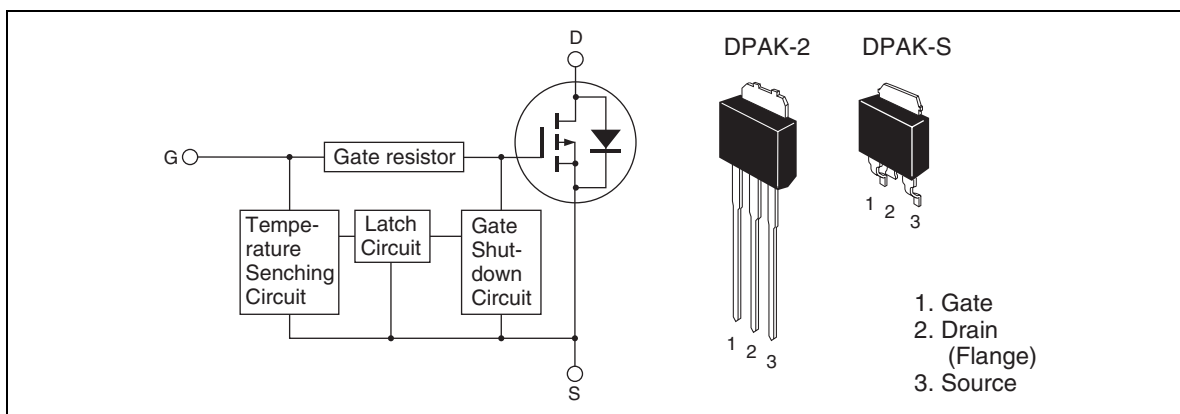
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation to (–4 to –6 V Gate drive)
- High endurance capability against to the shut-down circuit
- Built-in the over temperature shut-down circuit
- Latch type shut down operation (need 0 voltage recovery)

Outline



HAF1004(L), HAF1004(S)

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	−60	V
Gate to source voltage	V _{GSS}	−16	V
Gate to source voltage	V _{GSS}	2.5	V
Drain current	I _D	−5	A
Drain peak current	I _{D (pulse)} ^{Note1}	−10	A
Body-drain diode reverse drain current	I _{DR}	−5	A
Cannel dissipation	Pch ^{Note2}	20	W
Cannel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Notes: 1. PW ≤ 0μs, duty cycle ≤ 1%
2. Value at Ta = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	−3.5	—	—	V	
	V _{IL}	—	—	−1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	−100	μA	Vi = −8 V, V _{DS} = 0
	I _{IH2}	—	—	−50	μA	Vi = −3.5 V, V _{DS} = 0
	I _{IL}	—	—	−1	μA	Vi = −1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	−0.8	—	mA	Vi = −8 V, V _{DS} = 0
	I _{IH(sd)2}	—	−0.35	—	mA	Vi = −3.5 V, V _{DS} = 0
Shut down temperature	Tsd	—	175	—	°C	Cannel temperature
Gate operation voltage	Vop	−3.5	—	−12	V	

Electrical Characteristics

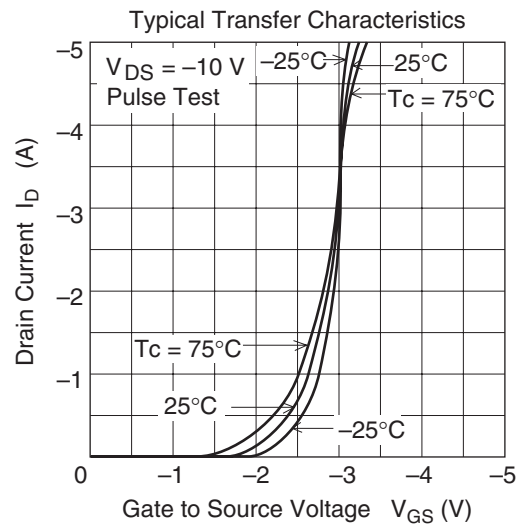
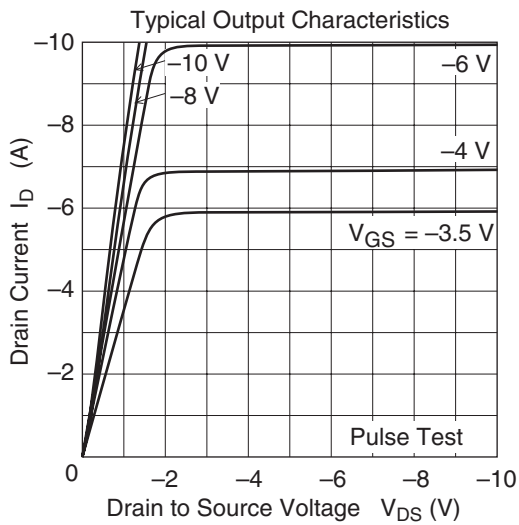
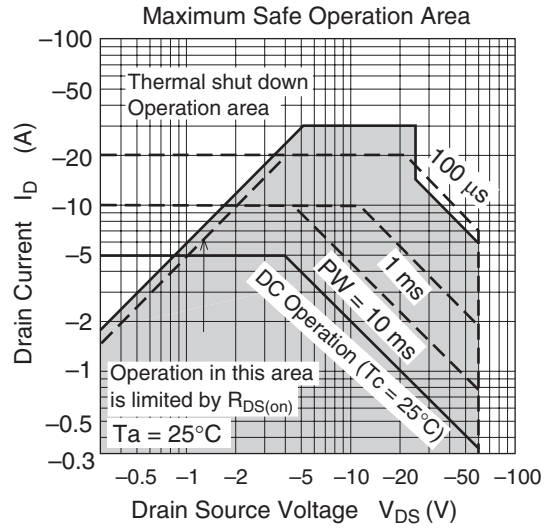
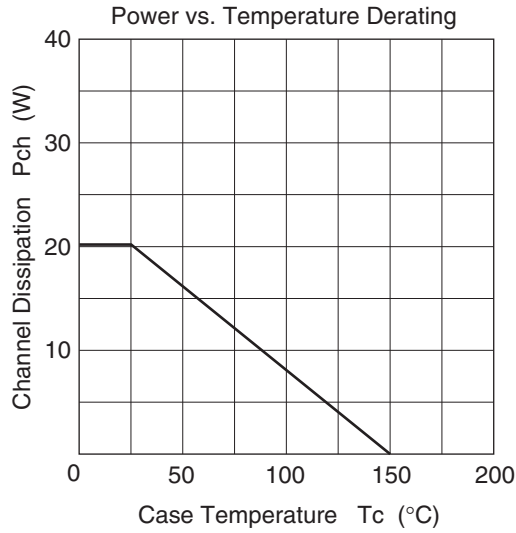
(Ta = 25°C)

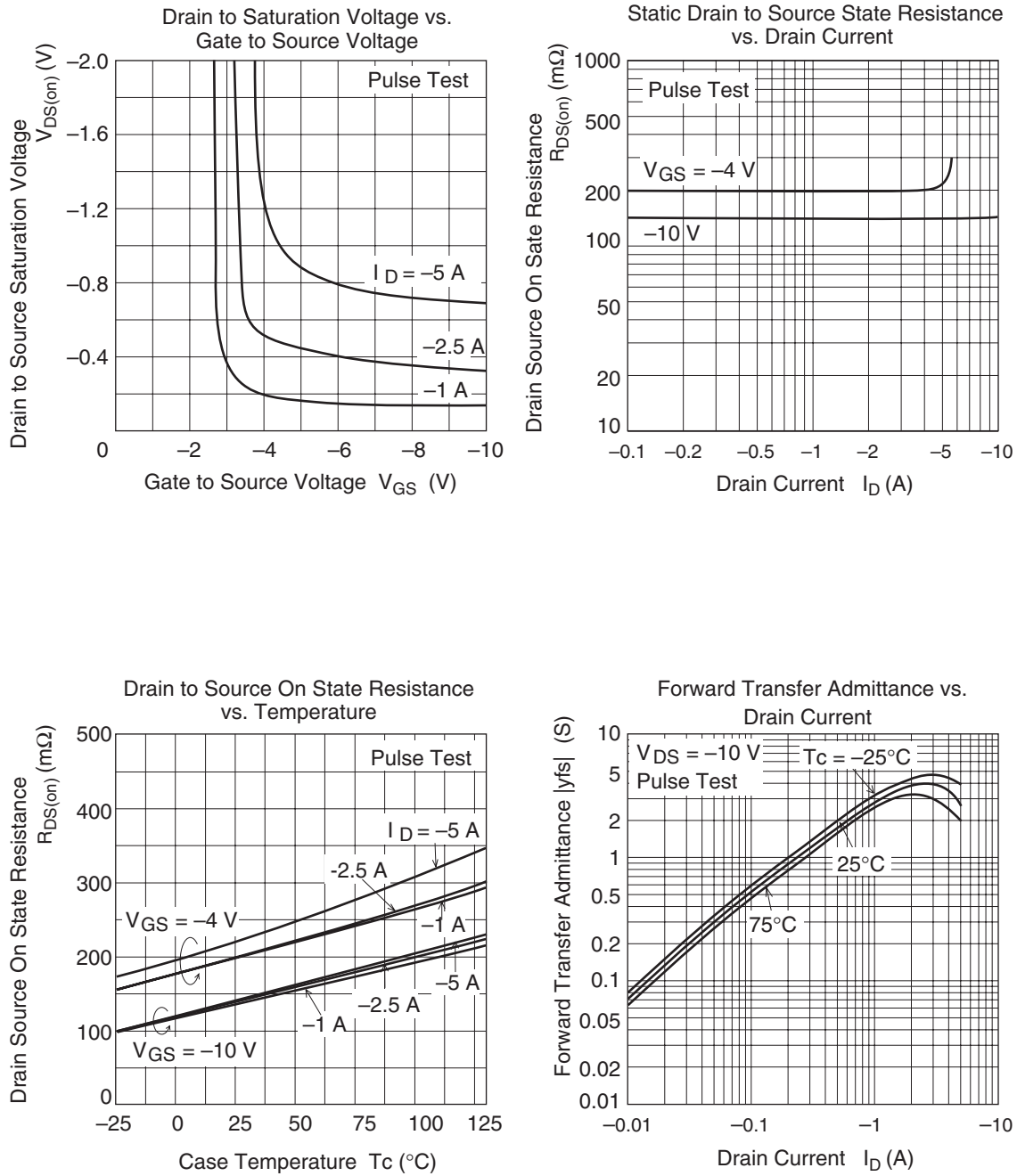
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	4	—	—	A	V _{GS} = -3.5 V, V _{DS} = -2 V
Drain current	I _{D2}	—	—	-10	mA	V _{GS} = -1.2 V, V _{DS} = -2 V
Drain to source breakdown voltage	V _{(BR)DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	-16	—	—	V	I _G = -800 µA, V _{DS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	2.5	—	—	V	I _G = 100 µA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	-100	µA	V _{GS} = -8 V, V _{DS} = 0
	I _{GSS2}	—	—	-50	µA	V _{GS} = -3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	-1	µA	V _{GS} = -1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	100	µA	V _{GS} = 2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	-0.8	—	mA	V _{GS} = -8 V, V _{DS} = 0
	I _{GS(OP)2}	—	-0.35	—	mA	V _{GS} = -3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	µA	V _{DS} = -60 V, V _{GS} = 0
Gate to source cut off voltage	V _{GS(off)}	-1.1	—	-2.25	V	V _{DS} = -10 V, I _D = -1 mA
Forward transfer admittance	y _{fs}	2	4	—	S	I _D = -2.5 A, V _{DS} = -10 V ^{Note3}
Static drain to source on state resistance	R _{DS(on)}	—	140	200	mΩ	I _D = -2.5 A, V _{GS} = -10 V ^{Note3}
Static drain to source on state resistance	R _{DS(on)}	—	200	340	mΩ	I _D = -2.5 A, V _{GS} = -4 V ^{Note3}
Output capacitance	C _{oss}	—	326	—	pF	V _{DS} = -10 V, V _{GS} = 0, f = 1 MHz
Turn-on delay time	t _{d(on)}	—	2	—	µs	V _{GS} = -5 V, I _D = -2.5 A, R _L = 12 Ω
Rise time	t _r	—	7.6	—	µs	
Turn off delay time	t _{d(off)}	—	3.2	—	µs	
Fall time	t _f	—	3.2	—	µs	
Body-drain diode forward voltage	V _{DF}	—	-0.9	—	V	I _F = -5A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	77	—	ns	I _F = -5 A, V _{GS} = 0 diF/dt = 50 A/µs
Over load shut down operation time ^{note4}	t _{os1}	—	8.4	—	ms	V _{GS} = -5 V, V _{DD} = -16 V
	t _{os2}	—	2.4	—	ms	V _{GS} = -5 V, V _{DD} = -24 V

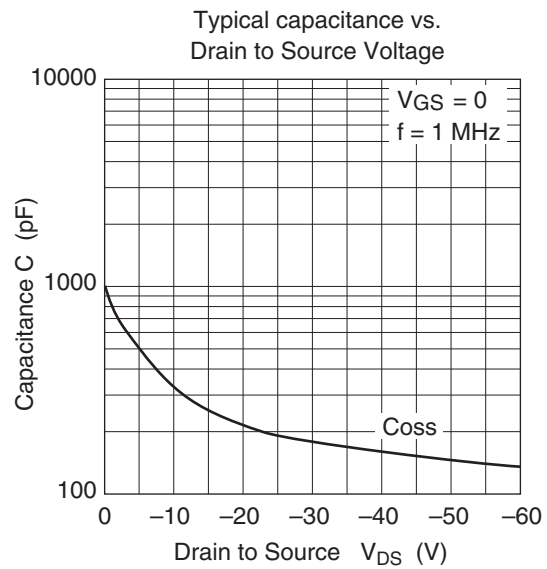
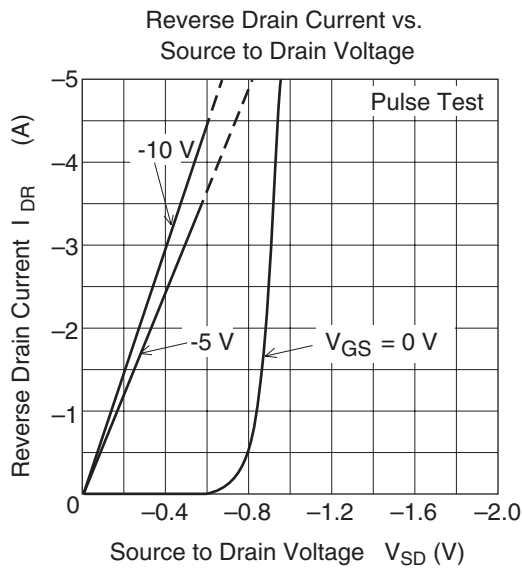
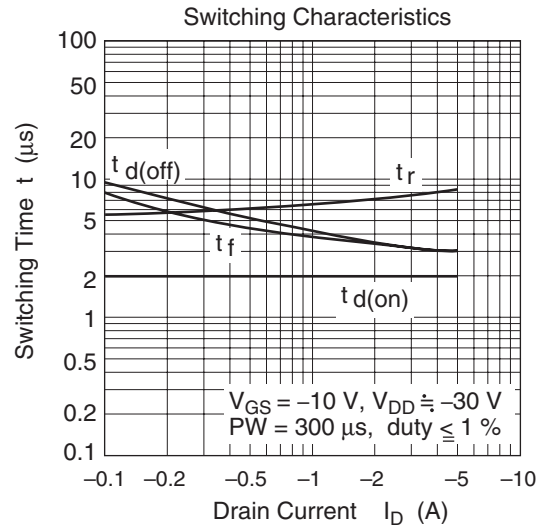
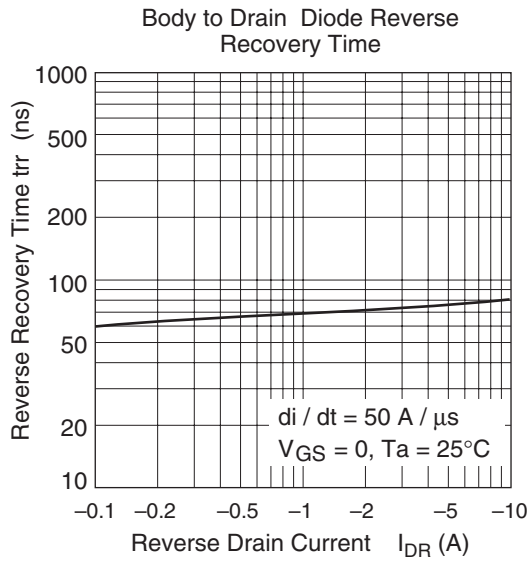
Notes: 3. Pulse test

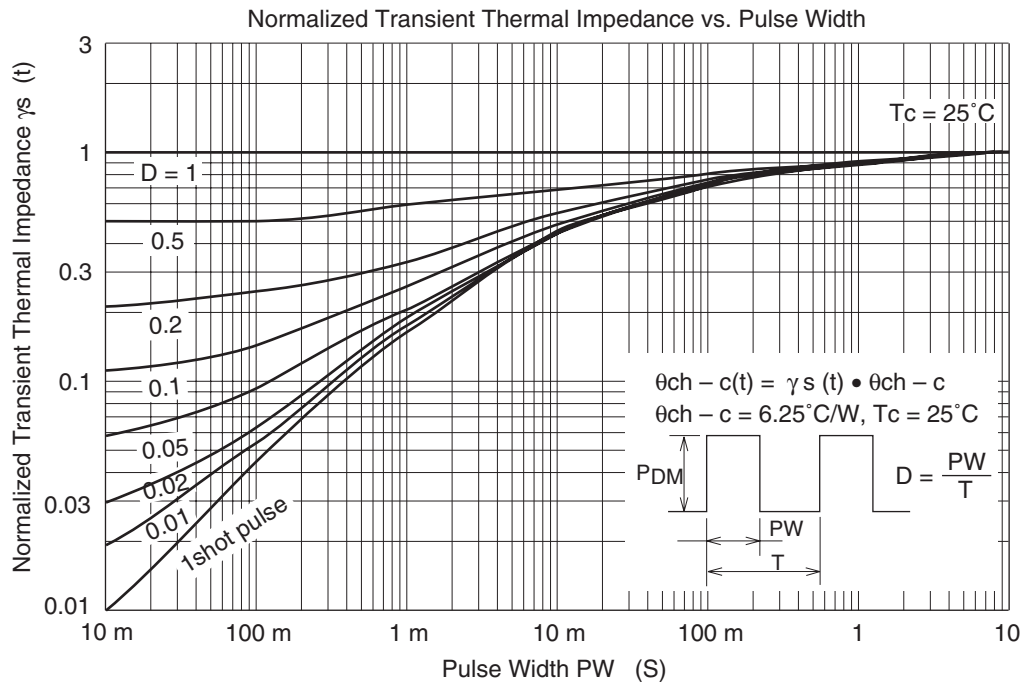
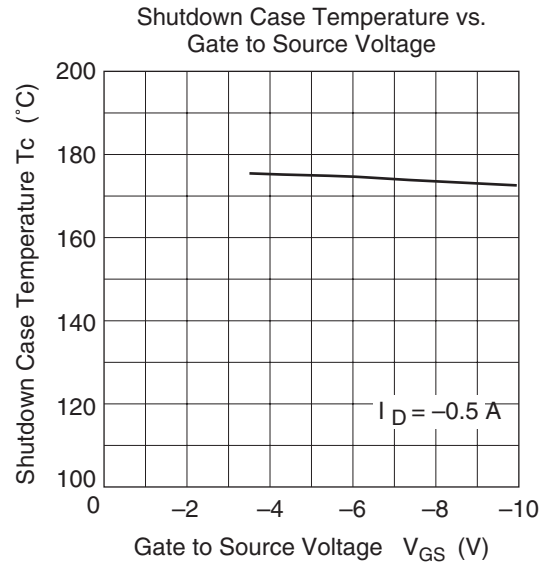
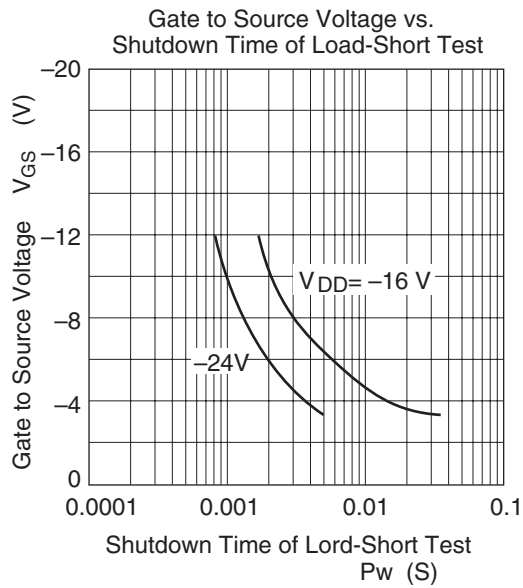
4. Including the junction temperature rise of the loded condition

Main Characteristics

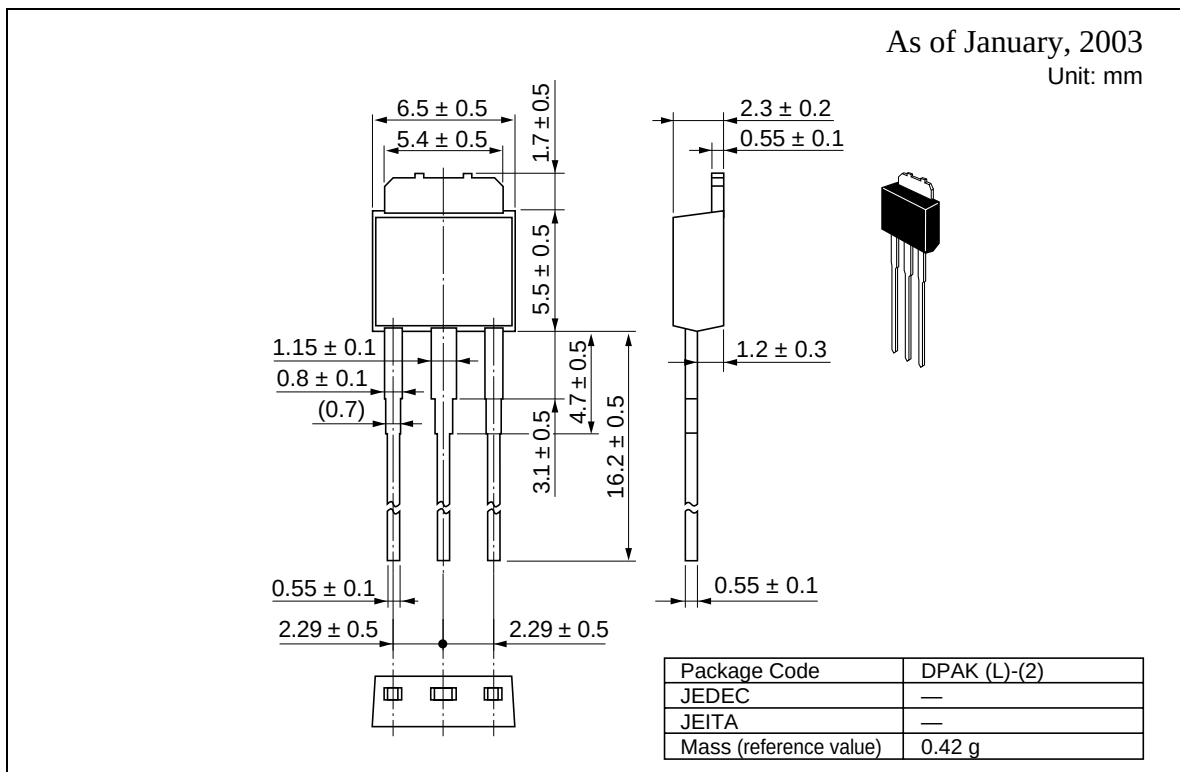






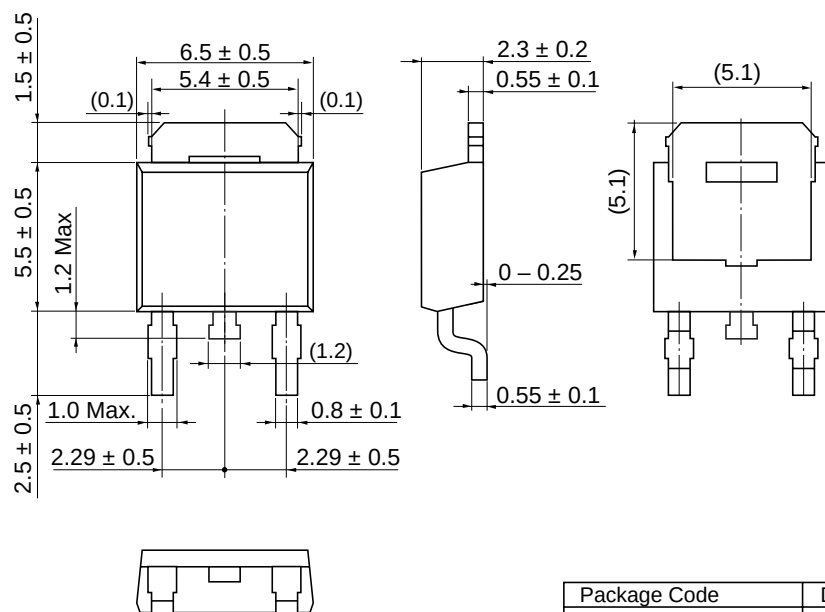


Package Dimensions



As of January, 2003

Unit: mm



Package Code	DPAK (S)
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.28 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
 2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.
-



<http://www.renesas.com>



Copyright © 2003, Renesas Technology Corporation, All rights reserved. Printed in Japan.
Colophon 0.0