DATA SHEET

PCF8570
256 × 8-bit static low-voltage RAM with I²C-bus interface

Preliminary specification
File under Integrated Circuits, IC12

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Philips Semiconductors

PHILIPS

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256 × 8-bit static low-voltage RAM with I²C-bus interface

PCF8570

FEATURES

- Operating supply voltage 2.5 to 6.0 V
- Low data retention voltage; minimum 1.0 V
- Low standby current; maximum 15 μA
- Power saving mode; typical 50 nA
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Available in DIP8 and SO8L packages.

APPLICATIONS

- Telephony:
  - RAM expansion for stored numbers in repertory dialling (e.g. PCD33XX applications)
- General purpose RAM for applications requiring extremely low current and low-voltage RAM retention (i.e. battery or capacitor backed)
- Radio, television and video cassette recorder:
  - channel presets
- General purpose:
  - RAM expansion for the microcontroller families PCD33XX, PCF84CXX, P80CLXXX and most other microcontrollers.

GENERAL DESCRIPTION

The PCF8570 is a low power static CMOS RAM.

The PCF8570 is organized as 256 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.5	6.0	
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	15	μA
I_{DDR}	supply current (power-saving mode)	T_{amb} = 25 °C	–	400	nA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8570P	8	DIP8	plastic	SOT97-1
PCF8570T	8	SO8L	plastic	SOT176-1

BLOCK DIAGRAM

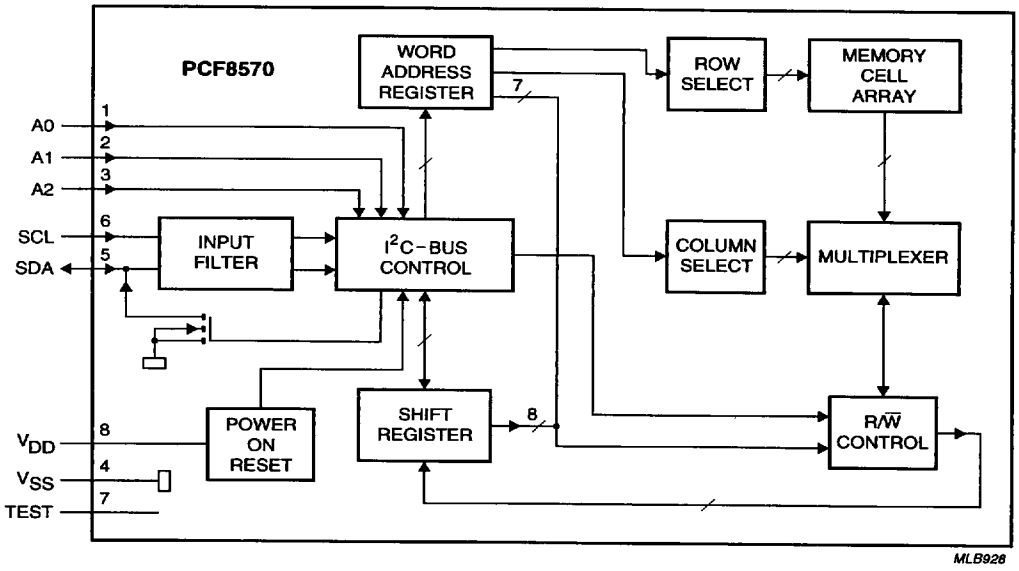


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 13 and 14)
V_{DD}	8	positive supply

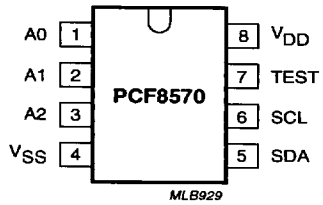


Fig.2 Pin configuration.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

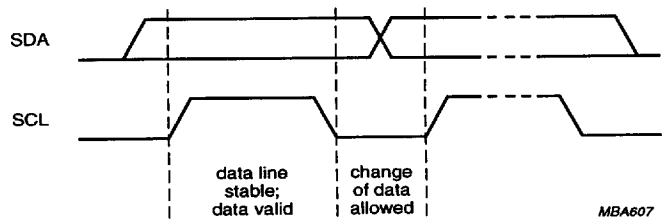


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

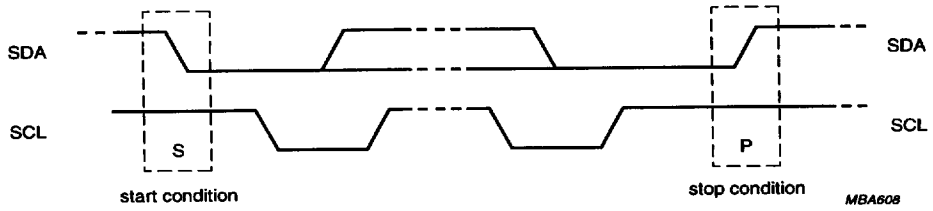


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

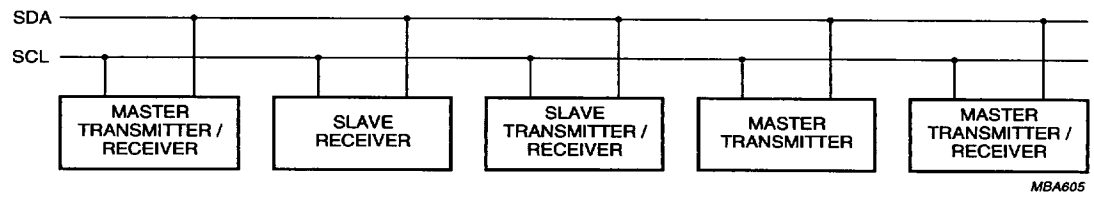


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

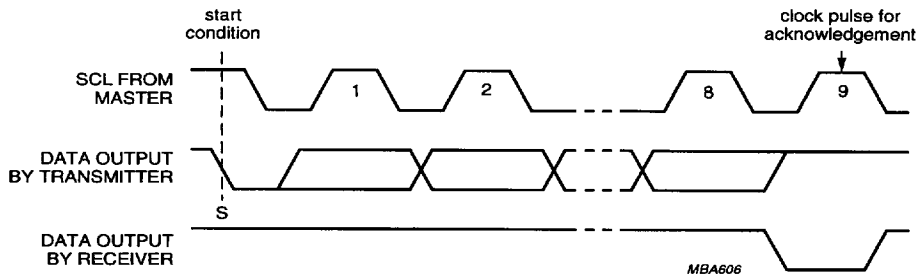


Fig.6 Acknowledgement on the I²C-bus.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8570 WRITE and READ cycles is shown in Figs 7, 8 and 9.

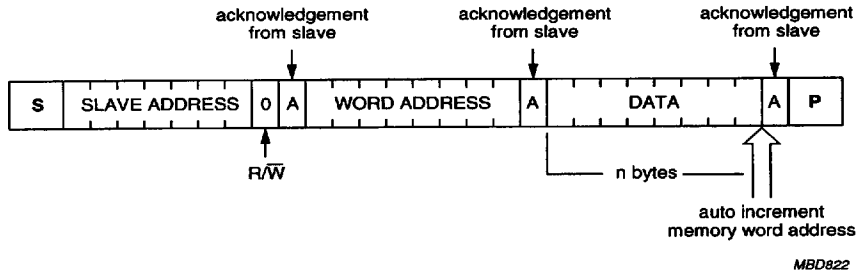


Fig.7 Master transmits to slave receiver (WRITE) mode.

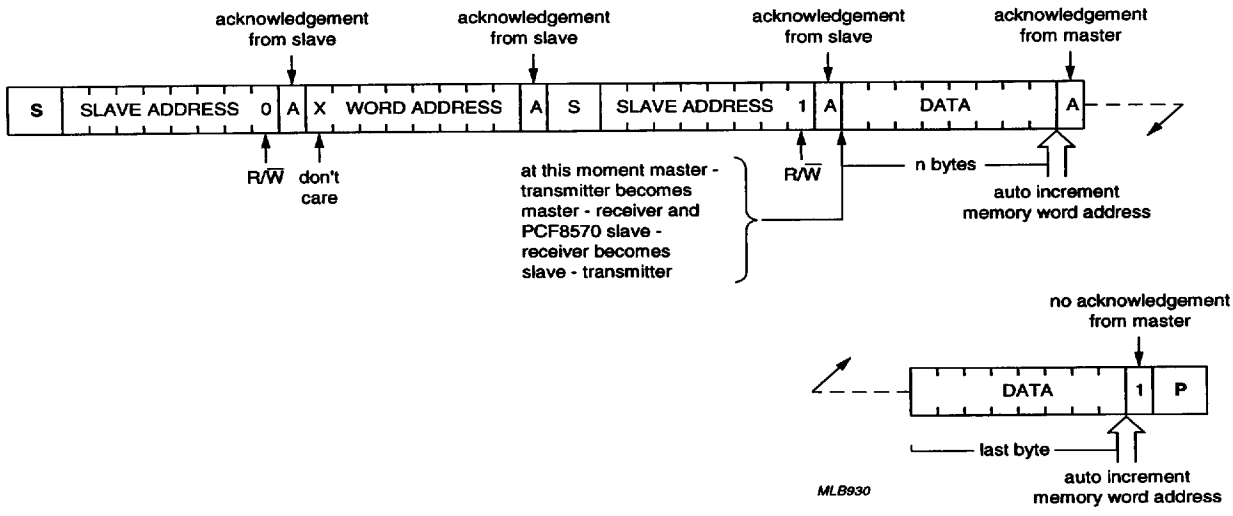


Fig.8 Master reads after setting word address (WRITE word address; READ data).

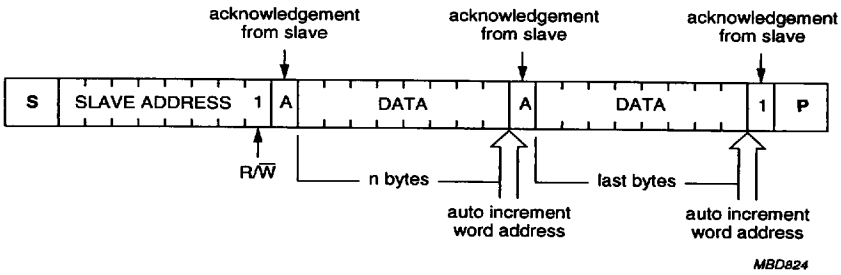


Fig.9 Master reads slave immediately after first byte (READ mode).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+8.0	V
V_I	input voltage (any input)	−0.8	V_{DD} + 0.8	V
I_I	DC input current	–	±10	mA
I_O	DC output current	–	±10	mA
I_{DD}	positive supply current	–	±50	mA
I_{SS}	negative supply current	–	±50	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
I_{DD}	supply current					
	standby mode	$V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 Hz; T_{amb} = −25 to +70 °C	–	–	5	µA
	operating mode	$V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 Hz	–	–	200	µA
V_{POR}	power-on reset voltage	note 1	1.5	1.9	2.3	V
Inputs, input/output SDA						
V_{IL}	LOW level input voltage	note 2	−0.8	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 2	$0.7V_{DD}$	–	V_{DD} + 0.8	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
$\|I_{LI}\|$	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	1	µA
Inputs A0, A1, A2 and TEST						
$\|I_{LI}\|$	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	±250	nA
Inputs SCL and SDA						
C_I	input capacitance	$V_I = V_{SS}$	–	–	7	pF
Low V_{DD} data retention						
V_{DDR}	supply voltage for data retention		1	–	6	V
I_{DDR}	supply current	V_{DDR} = 1 V	–	–	5	µA
		V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	–	–	2	µA
Power saving mode (see Figs 13 and 14)						
I_{DDR}	supply current	TEST = V_{DD}; T_{amb} = 25 °C	–	50	400	nA
t_{HD2}	recovery time		–	50	–	µs

Notes

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ±0.5 mA.

AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.10; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW-to-data out valid	–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

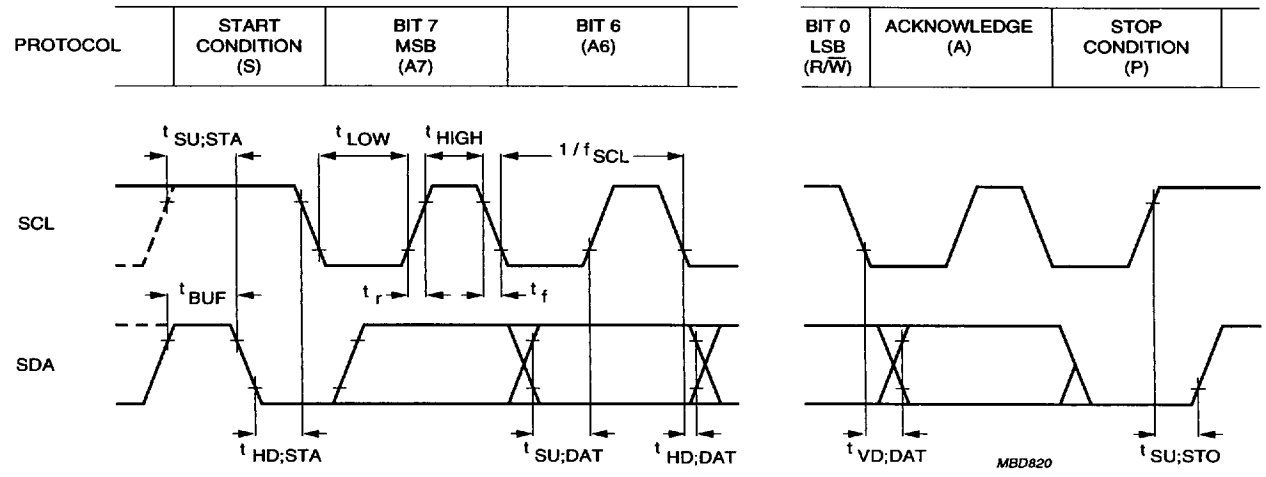


Fig.10 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Slave address

The PCF8570 has a fixed combination 1 0 1 0 as group 1, while group 2 is fully programmable (see Fig.11).

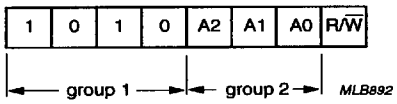
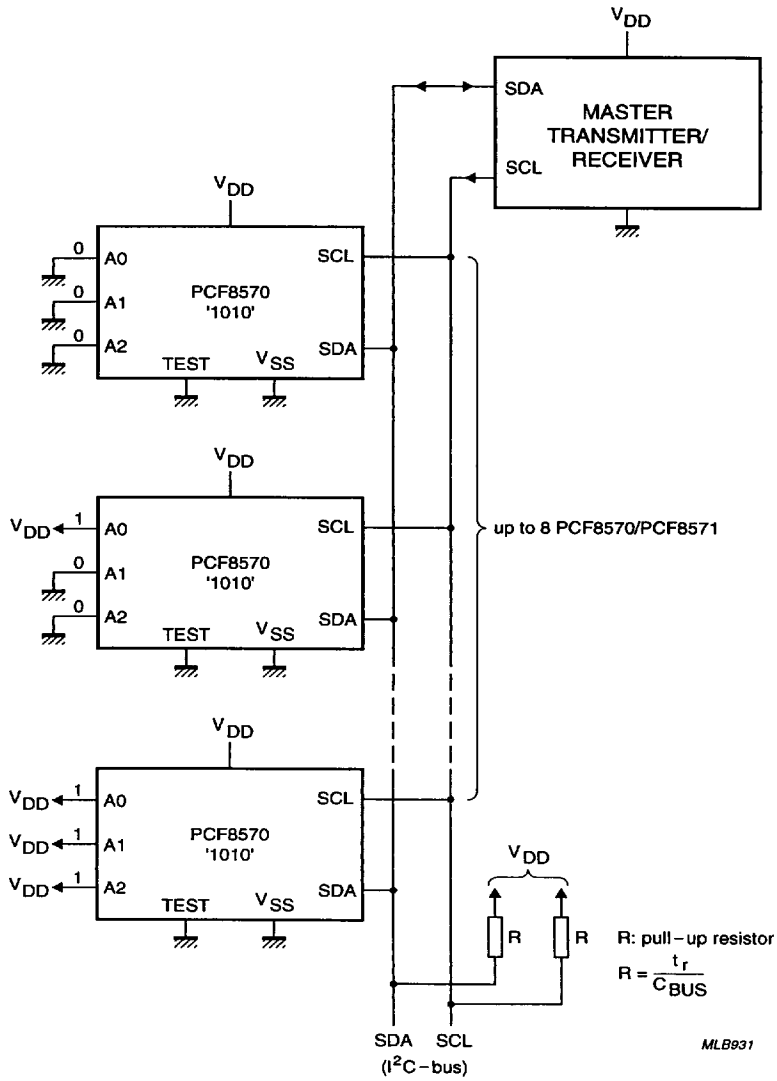


Fig.11 Slave address.

Application example

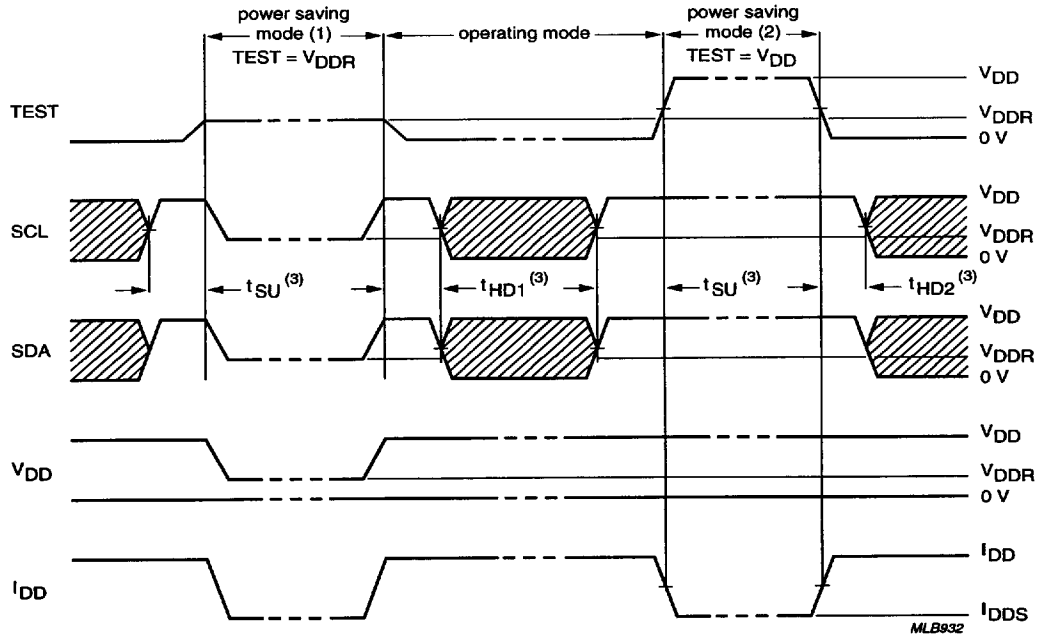


It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.12 Application diagram.

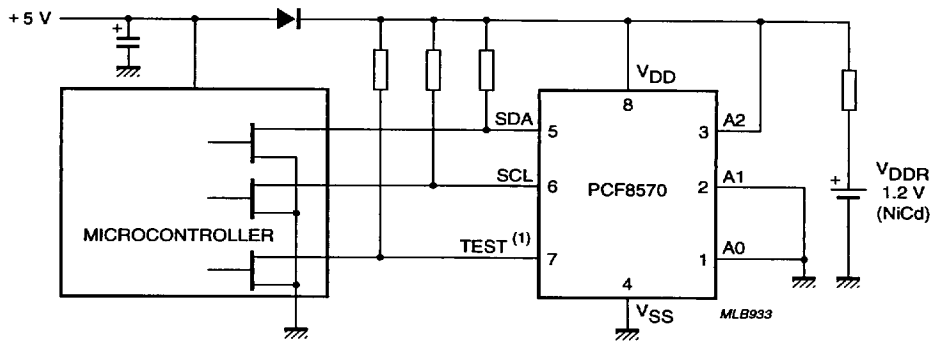
Power saving mode

With the condition TEST = V_{DD} or V_{DDR} the PCF8570 goes into the power saving mode and I²C-bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and t_{HD1} ≥4 µs and t_{HD2} ≥50 µs.

Fig.13 Timing for power saving mode.

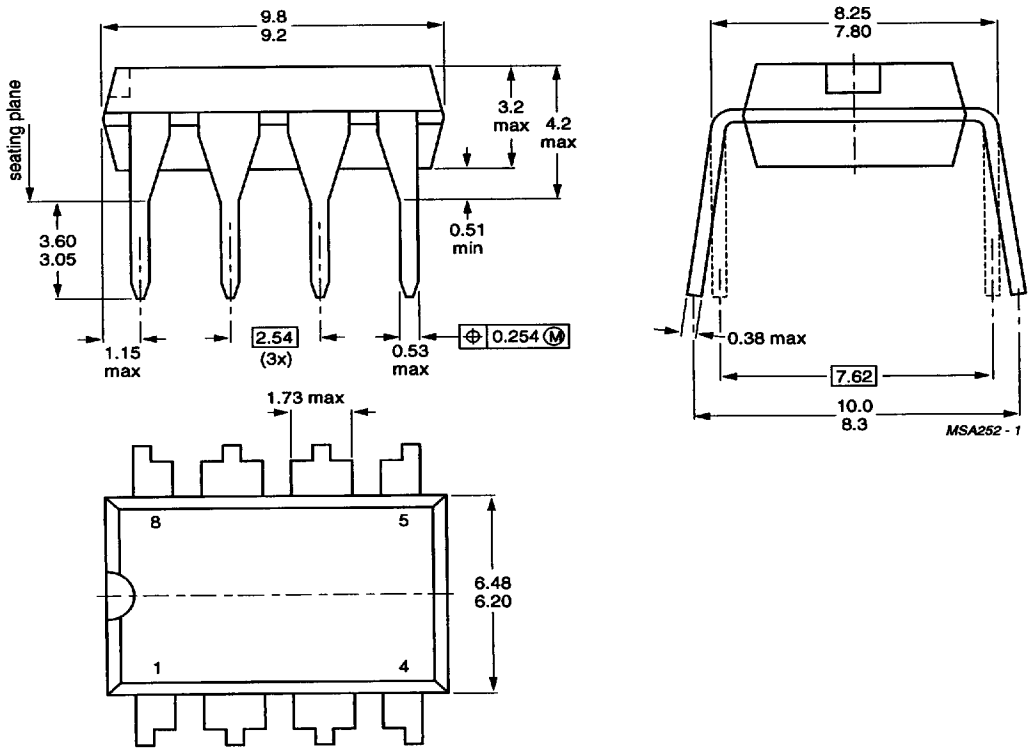


It is recommended that a 4.7 µF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

(1) In the operating mode TEST = 0 V; in the power saving mode TEST = V_{DDR}.

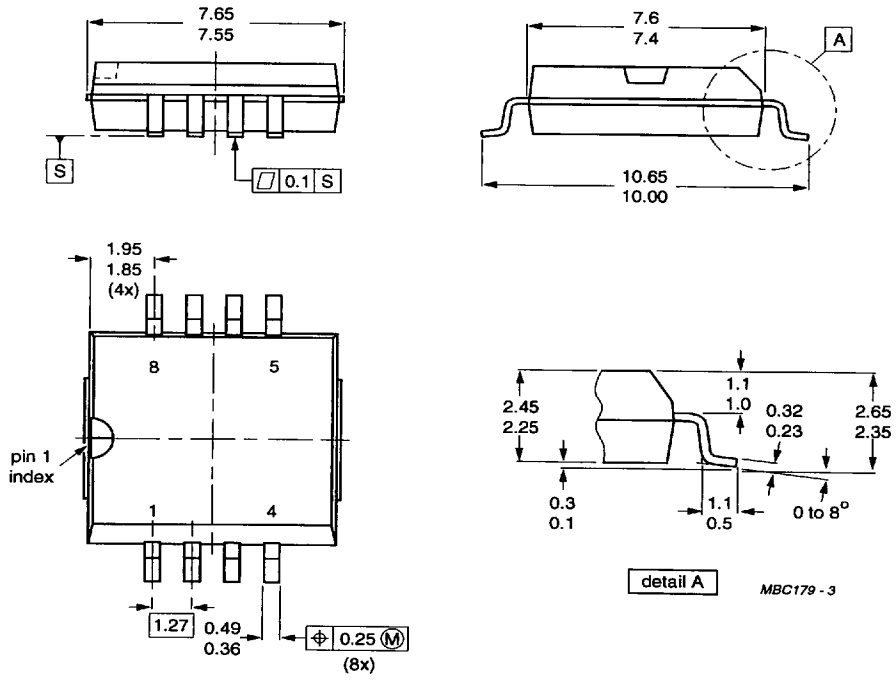
Fig.14 Application example for power saving mode.

PACKAGE OUTLINES



Dimensions in mm.

Fig.15 Plastic dual in-line package; 8 leads (300 mil); DIP8, SOT97-1.



Dimensions in mm.

Fig.16 Plastic small outline package; 8 leads; large body (SO8L, SOT176-1).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low-voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.