

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π -MOS)

2SK3758

Switching Regulator Applications

- Low drain-source ON resistance: $R_{DS(ON)} = 1.35 \Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 3.5S$ (typ.)
- Low leakage current: $I_{DSS} = 100 \mu A$ ($V_{DS} = 500 V$)
- Enhancement-mode: $V_{th} = 2.0 \sim 4.0 V$ ($V_{DS} = 10 V, I_D = 1 mA$)

/Circuit

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	500	V
Drain-gate voltage ($R_{GS} = 20 k\Omega$)		V_{DGR}	500	V
Gate-source voltage		V_{GSS}	± 30	V
	DC (Note 1)	I_D	5	
	Pulse ($t = 1 ms$) (Note 1)	I_{DP}	20	
Drain power dissipation ($T_c = 25^\circ C$)		P_D	58	W
Single pulse avalanche energy (Note 2)		E_{AS}	12	mJ
Avalanche current		I_{AR}	5	A
Repetitive avalanche energy (Note 3)		E_{AR}	5.8	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	-55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	2.16	°C/W
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	°C/W

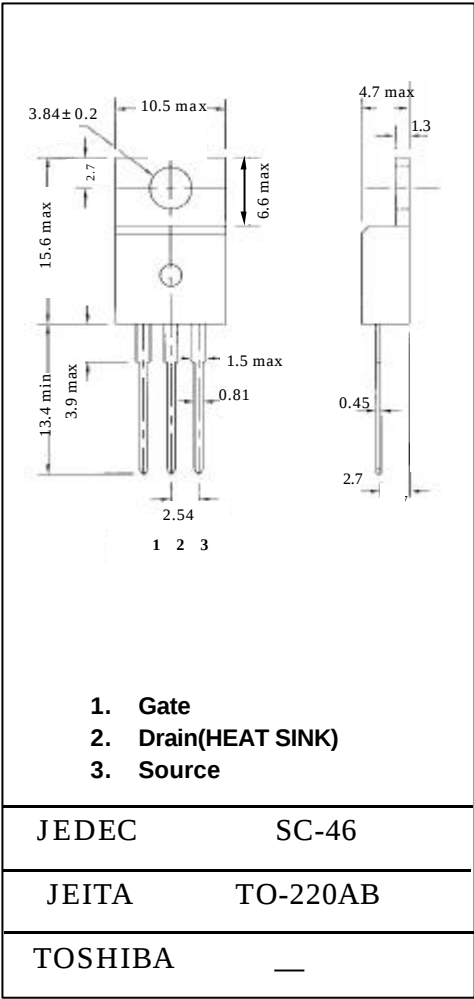
Note 1: Please use devices on conditions that the channel temperature is below 150°C.

Note 2: $V_{DD} = 90 V, T_{ch} = 25^\circ C$ (initial), $L = 0.82 mH, I_{AR} = 5 A, R_G = 25 \Omega$

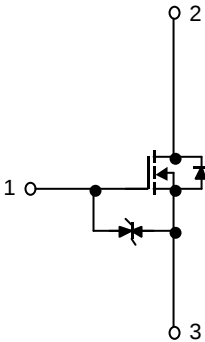
Note 3: Repetitive rating: Pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.

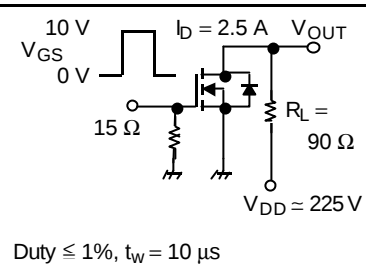
unit : mm



Weight : 2.0g(typ.)



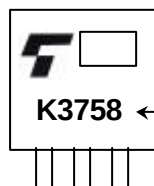
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Gate-source breakdown voltage		$V_{(BR) GSS}$	$I_D = \pm 10 \mu\text{A}, V_{GS} = 0 \text{ V}$	± 30	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR) DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	500	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$	—	1.35	1.50	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 2.5 \text{ A}$	1.5	3.5	—	S
Input capacitance		C_{iss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	550	—	pF
Reverse transfer capacitance		C_{rss}		—	7	—	
Output capacitance		C_{oss}		—	70	—	
Switching time	Rise time	t_r		—	10	—	ns
	Turn-on time	t_{on}		—	20	—	
	Fall time	t_f		—	10	—	
	Turn-off time	t_{off}		—	50	—	
Total gate charge		Q_g	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	—	16	—	nC
Gate-source charge		Q_{gs}		—	10	—	
Gate-drain charge		Q_{gd}		—	6	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	20	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 5 \text{ A}, V_{GS} = 0 \text{ V},$	—	1400	—	ns
Reverse recovery charge	Q_{rr}	$dI_{DR}/dt = 100 \text{ A}/\mu\text{s}$	—	9	—	μC

Marking



TYPE

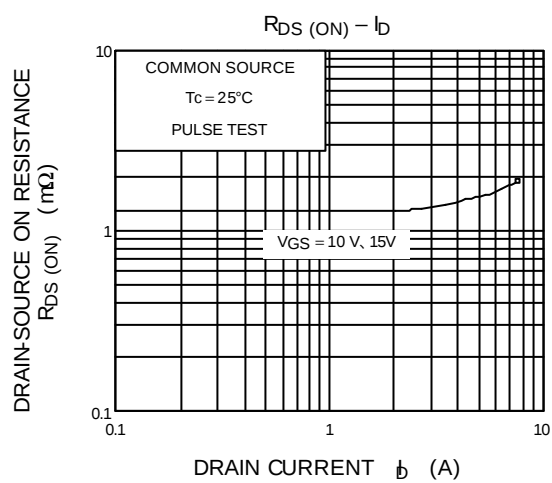
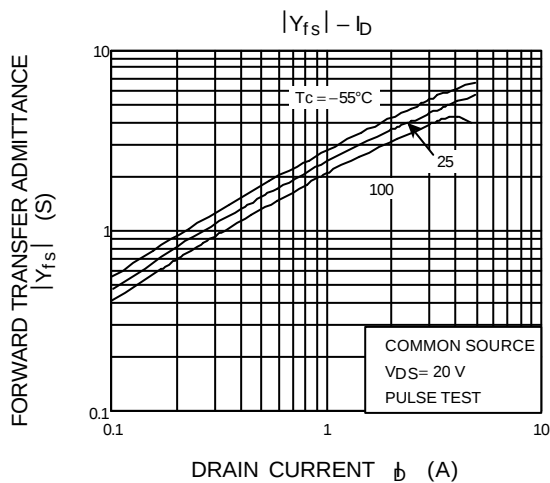
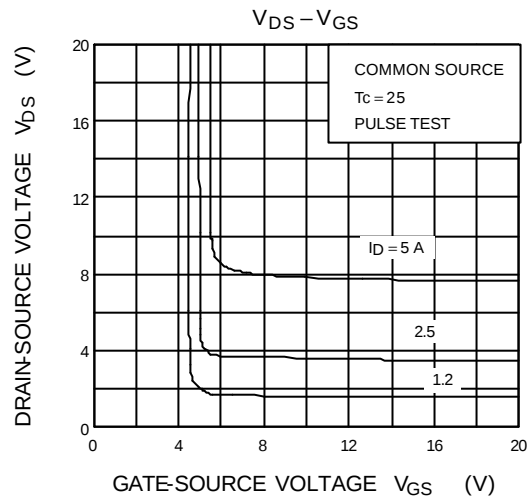
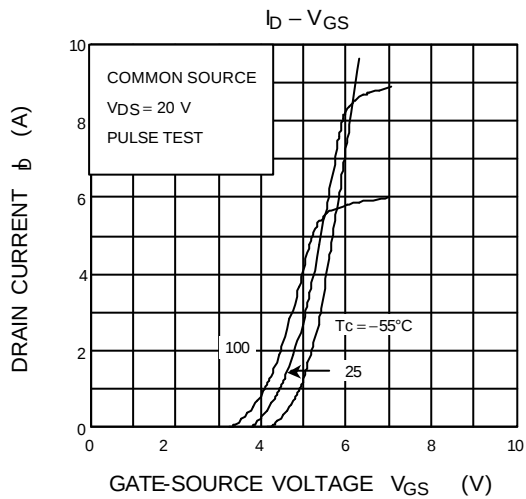
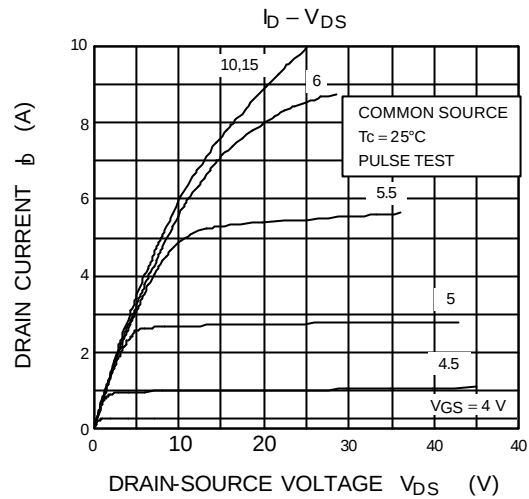
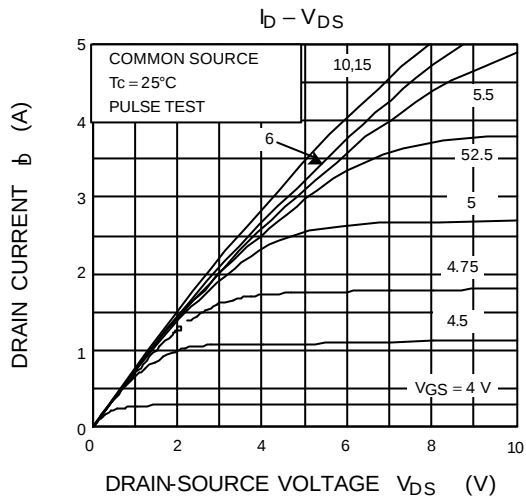
Lot Number

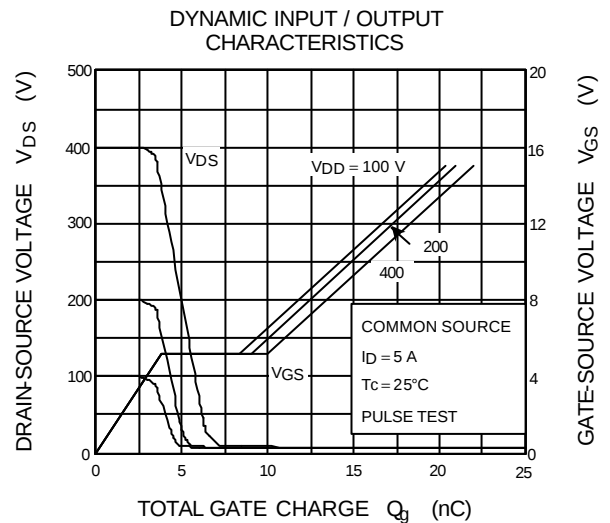
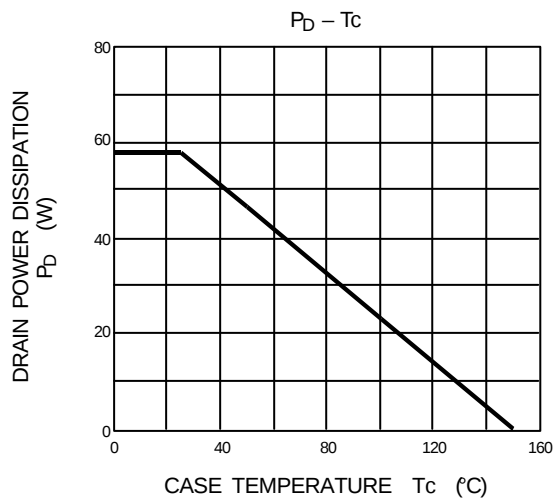
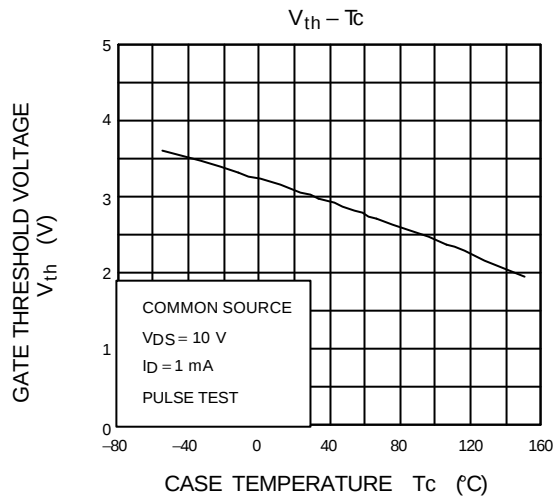
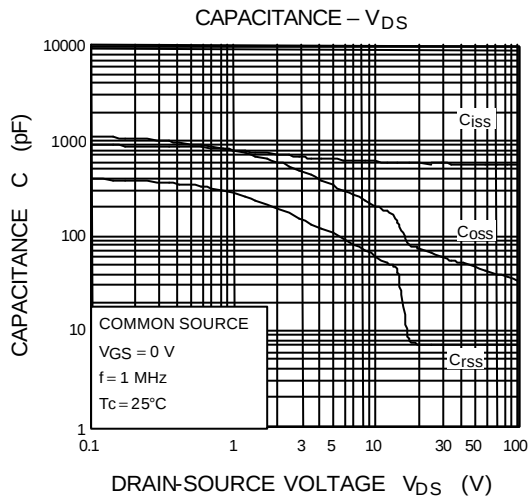
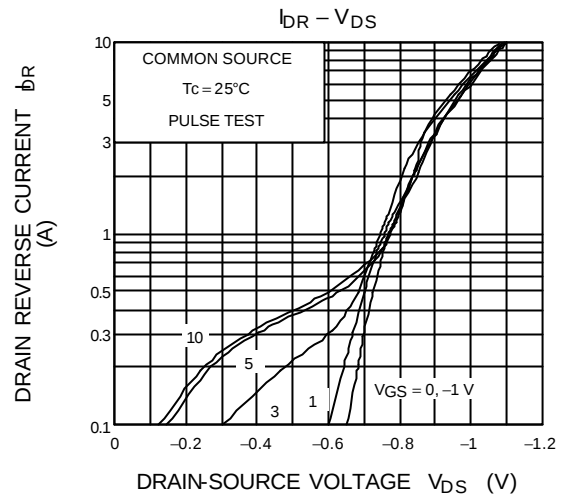
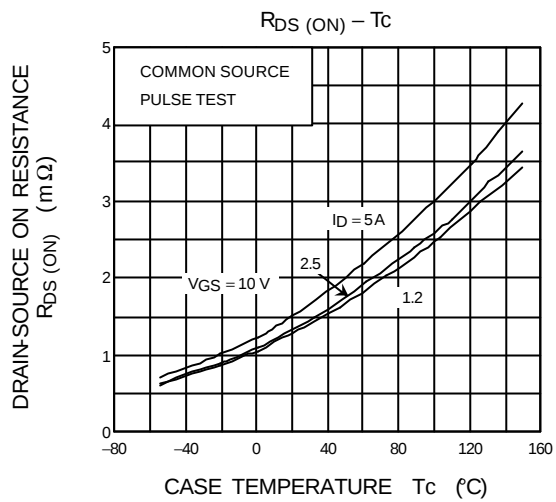


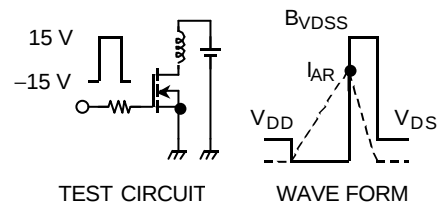
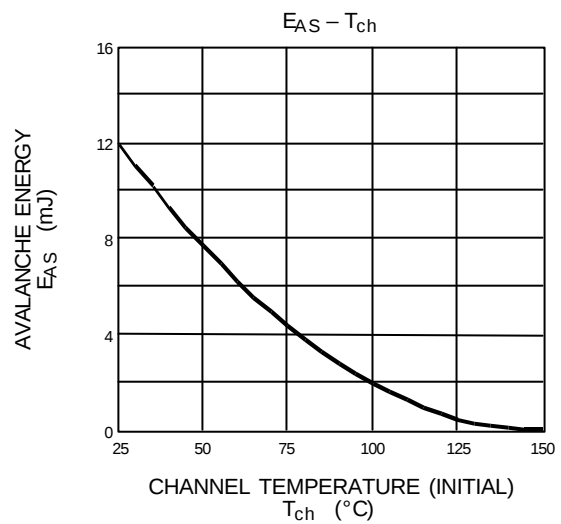
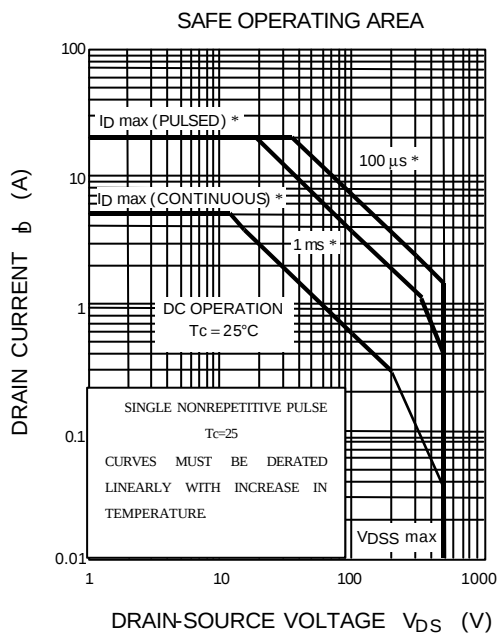
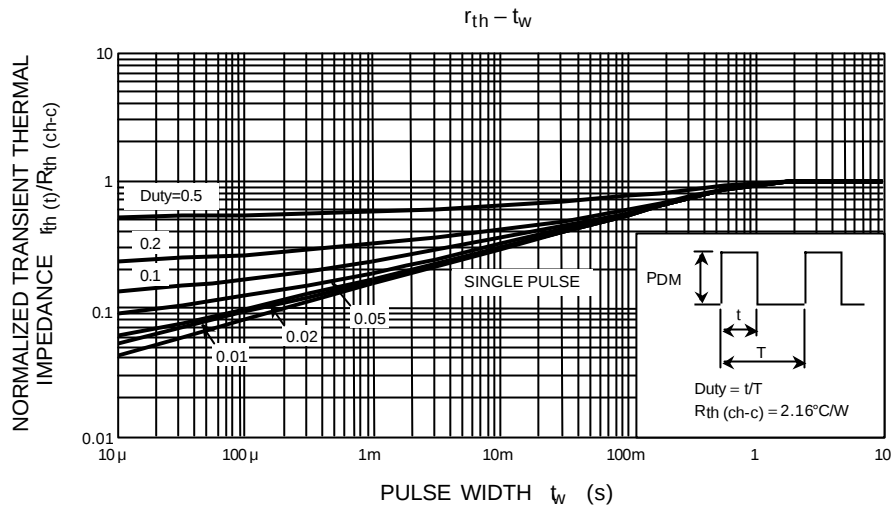
Date

Month (Starting from Alphabet A)

Year (Last Number of the Christian Era)







$$R_G = 25 \, \Omega$$

$$V_{DD} = 90 \, V, L = 0.82 \, mH$$

$$\dot{A}_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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