

# Secondary Side Average Current Mode Controller

## FEATURES

- Practical Secondary Side Control of Isolated Power Supplies
- Provides a Self Regulating Bias Supply From a High Input Voltage Using an External N-Channel Depletion Mode FET
- Onboard Precision, Fixed Gain, Differential Current Sense Amplifier
- Wide Bandwidth Current Error Amplifier
- 5V Reference
- High Current, Programmable Gm Amplifier Optimized to Drive Opto-couplers

## DESCRIPTION

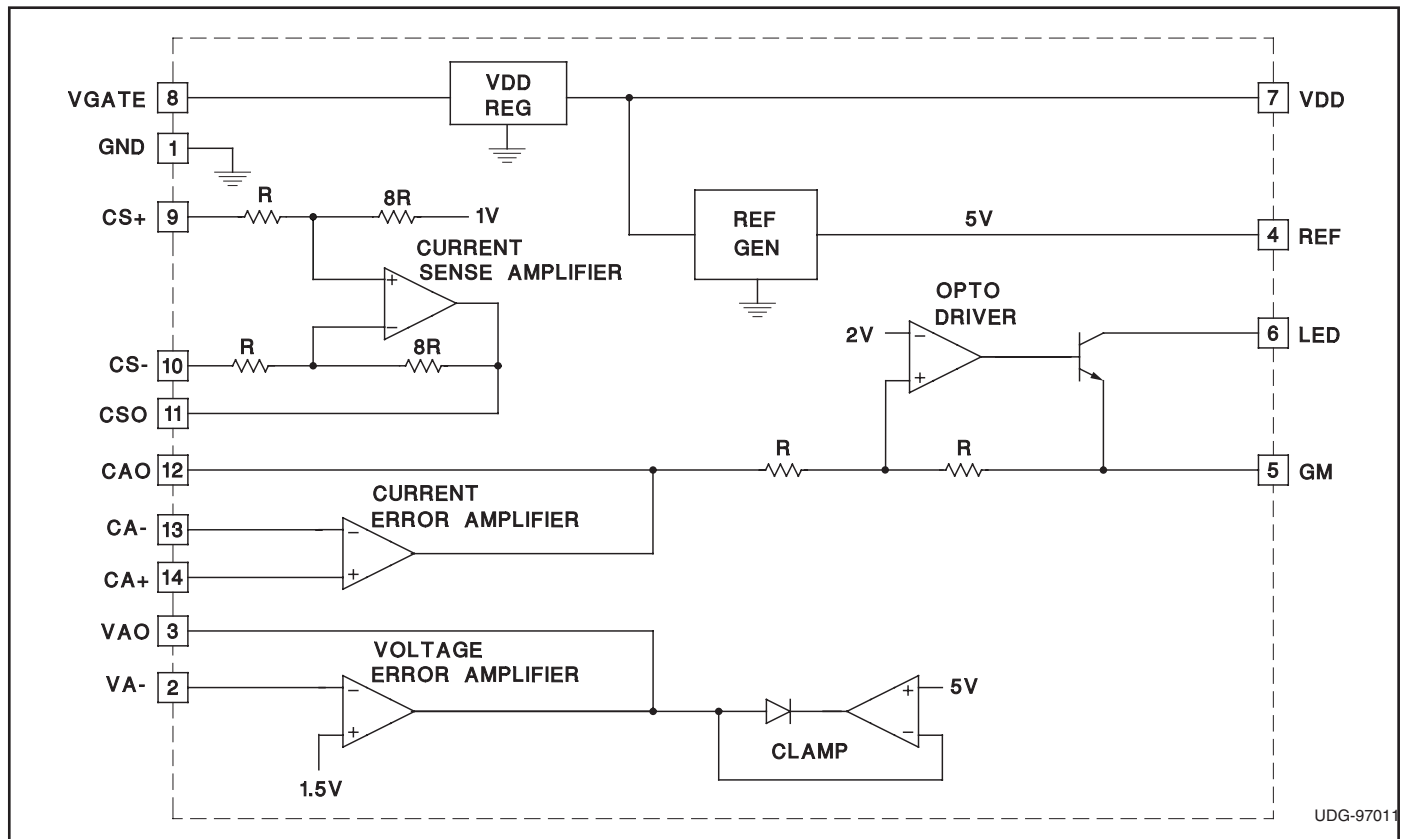
The UCC3839 provides the control functions for secondary side average current mode control in isolated power supplies. Start up, pulse width modulation and MOSFET drive must be accomplished independently on the primary side. Communication from secondary to primary side is anticipated through an opto-isolator.

Accordingly, the UCC3839 contains a fixed gain current sense amplifier, voltage and current error amplifiers, and a Gm type buffer/driver amplifier for the opto-isolator. Additional housekeeping functions include a precision 5V reference and a bias supply regulator.

Power for the UCC3839 can be generated by peak rectifying the voltage of the secondary winding of the isolation transformer. From this unregulated voltage, the UCC3839's bias supply regulator will generate its own 7.5V bias supply using an external, N-channel, depletion mode FET.

The UCC3839 can be configured for traditional average current mode control where the output of the voltage error amplifier commands the current error amplifier. It can also be configured for output voltage regulation with average current mode short circuit current limiting, employing two parallel control loops regulating the output voltage and output current independently.

## BLOCK DIAGRAM



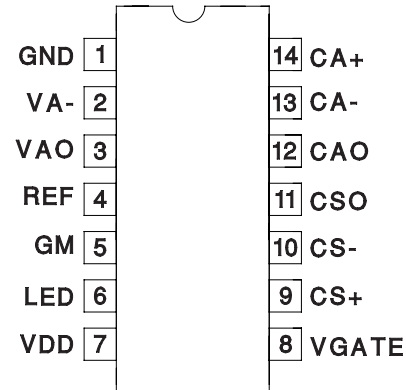
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15V
Supply Current	
(LED not connected)	2mA
(LED connected)	14mA
Analog Inputs	–0.3V to 15V
Power Dissipation at T <sub>A</sub> = 60°C	
(LED not connected)	20mW
(LED connected)	55mW
Storage Temperature	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10sec.)	+300°C

Currents are positive into, negative out of the specified terminal.  
Consult Packaging Section of Databook for thermal limitations and considerations of package.

## CONNECTION DIAGRAMS

DIL-14, SOIC-14 (Top View)  
D or N Package



**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, 0°C to 70°C for the UCC3839, –40°C to 85° for the UCC2839. V<sub>LINE</sub> = 10V, R<sub>G</sub> = 400Ω. T<sub>A</sub> = T<sub>J</sub>.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Current Error Amplifier</b>					
V <sub>IO</sub>				10	mV
AVOL		60			dB
CMRR	V <sub>CM</sub> = 0.5V to 5.5V	60			dB
PSRR	V <sub>LINE</sub> = 10V to 20V	60			dB
CAO High	CA– = 1V, CA+ = 1.1V, I <sub>CAO</sub> = –100μA	4.8		7	V
I <sub>CAO</sub>	CA– = 1V, CA+ = 1.1V, CAO = 0.5V	–500		–250	μA
CAO Low	CA– = 1V, CA+ = 0.9V, I <sub>CAO</sub> = 500μA		0.2	0.4	V
GBW	F = 100kHz, T <sub>A</sub> = 25°C	3	5		MHz
<b>Voltage Error Amplifier</b>					
VA–		1.46	1.5	1.525	V
AVOL		60			dB
PSRR	V <sub>LINE</sub> = 10V to 20V	60			dB
VAO High	I <sub>VAO</sub> = –100μA to 100μA	4.8	5	5.2	V
I <sub>VAO</sub>	VA– = 1.45V, VAO = 0.5V	–500		–250	μA
VAO Low	VA– = 1.55V, VAO = 0.5V, I <sub>VAO</sub> = 500μA		0.2	0.4	V
GBW	(Note 1)	3	5		MHz
<b>Current Sense Amplifier</b>					
CSO Zero	CS+ = CS– = –0.3V to 5.5V, I <sub>CSO</sub> = –100μA to 100μA	0.85	1	1.15	V
AV	CS+ = 0, CS– = 0mV to –200mV	7.75	8	8.2	V/V
<b>Current Sense Amplifier (cont.)</b>					
Slew Rate	CS+ = 0, CS– = 0mV to –0.5V	2	4		V/μs
CSO	CS+ = –200mV, CS– = –700mV	4.75	5	5.2	V
<b>LED Driver</b>					
I <sub>LED</sub>	LED = 5.5V, CA– = 1V, CA+ = 1.1V, R <sub>G</sub> = 400		0	10	μA
	LED = 5.5V, CA– = 1V, CA+ = 0.9V, R <sub>G</sub> = 400	9	10	11	mA
G <sub>m</sub>	LED = 5.5V, CAO = 1V to 3V, R <sub>G</sub> = 400	2.25	2.5	2.75	mS
Slew Rate	CAO = 2V to 2.5V, LED = 400Ω to 5.5V, R <sub>G</sub> = 400	1	4		V/μs

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, 0°C to 70°C for the UCC3839, –40°C to 85° for the UCC2839.  $V_{LINE} = 10V$ ,  $R_G = 400\Omega$ .  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Precision Reference</b>					
REF	$T_J = 25^\circ C$	4.94	5	5.06	V
	$I_{REF} = 0mA$ to 1mA, $V_{LINE} = 10V$ to 20V	4.9		5.1	V
VA+/REF		0.298	0.3	0.302	V/V
<b>VDD Regulator</b>					
VDD	$I_{DD} = 0mA$ to –15mA, $V_{LINE} = 10V$ to 40V	7	7.5	8	V
IVDD	$V_{LINE} = 10V$ to 40V, $CA- = 0V$ , $CA+ = 1V$ , $VA- = 2.9V$ , $CS+ = CS- = 0$ , $I_{REF} = 0$		1.3	2	mA

Note 1: Ensured by design. Not 100% tested in production.

## PIN DESCRIPTIONS

**CA–:** Current Error Amplifier Negative Input.

**CAO:** Current Error Amplifier Output. Output source current is limited, and output sink current is guaranteed to be greater than the VAO output source current. Current loop compensation components are generally connected to CAO and CA–.

**CA+:** Current Error Amplifier Positive Input.

**CS–:** Current Sense Amplifier Negative Input.

**CSO:** Current Sense Amplifier Output. Internally set gain  $V_{OUT}/V_{IN} = 8$   $V_{IN} = 0V$  results in  $CSO = 1V$ .

**CS+:** Current Sense Amplifier Positive Input.

**GM:** Gm (transconductance) Programming Pin. Resistor  $R_{GM} = 400\Omega$  to GND.

**GND:** Chip Ground.

**LED:** Output of LED Driver. Connect LED from VDD pin to LED.

**REF:** 5V Precision Reference Buffer Output. Minimum Decoupling Capacitance = 0.01 $\mu$ F

**VA–:** Voltage Error Amplifier Negative Input. Voltage Error Amplifier is internally referenced to 1.5V

**VAO:** Voltage Error Amplifier Output. In a two loop average current mode control configuration, VAO is connected to CA+ and is the current command signal. VAO is internally clamped not to exceed 5V for short circuit control. In a single loop voltage mode control configuration with a parallel average short circuit current control loop, VAO is connected directly to CAO. Output source current is limited, and output sink current is guaranteed to be greater than the CAO output source current.

**VDD:** 7.5V Regulator output. Supply for most of the chip. Minimum Decoupling Capacitance = 0.01 $\mu$ F

**VGATE:** External FET Gate Control Voltage.

## APPLICATION INFORMATION

Fig. 1 shows a typical secondary side average current mode controller configuration using the UCC3839. In this configuration, output voltage is sensed and regulated by the voltage error amplifier. Its output, VAO provides the reference for the current error amplifier at the CA+ pin. VAO can be connected to CA+ directly or through a resistive divider depending on the particular application requirements.

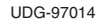
Average current mode control needs accurate output current information which is provided by a low value current sense resistor. The voltage proportional to the converter's output current is sensed and amplified by the

precision current sense amplifier of the chip. The onboard current sense amplifier has a gain of 8 and is intended for differential sensing of the shunt voltage with a common mode voltage range from 0V up to 5V. The output of the current sense amplifier, CSO is 1V for zero input which guarantees that the circuit can control currents down to 0A.

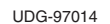
The CSO signal is fed to the CA– input of the current error amplifier through a resistor. The current error amplifier takes the VAO and CSO signals and generates the error signal for the pulse width modulator.



## APPLICATION INFORMATION (cont.)



**Figure 2. Voltage mode with average current short circuit limit.**



**Figure 3. Typical primary side circuit for use with secondary side average current mode controller.**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC2839D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	UCC2839D	
UCC2839DG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85		
UCC3839D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
UCC3839DG4	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		

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**TBD:** The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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