



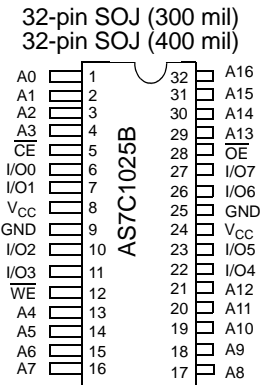
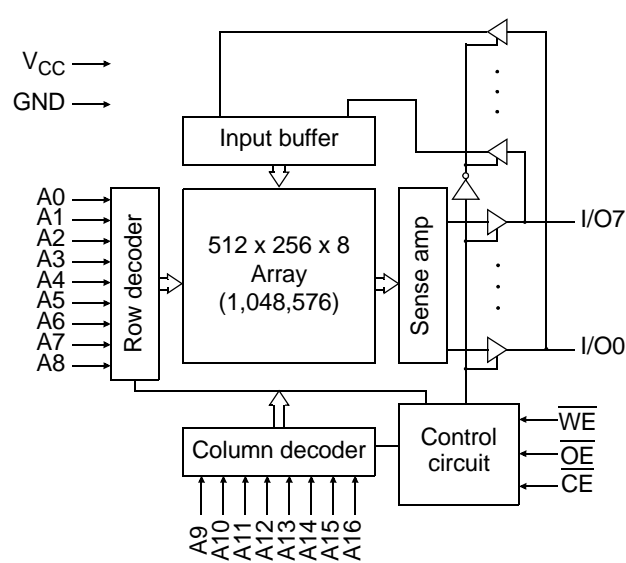
5V 128K X 8 CMOS SRAM (Center power and ground)

Features

- Industrial and commercial temperatures
- Organization: 131,072 x 8 bits
- High speed
  - 10/12/15/20 ns address access time
  - 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
  - 605mW / max @ 10 ns
- Low power consumption: STANDBY
  - 55 mW / max CMOS
- 6 T 0.18 u CMOS technology
- Easy memory expansion with  $\overline{CE}$ ,  $\overline{OE}$  inputs
- Center power and ground
- TTL/LVTTL-compatible, three-state I/O
- JEDEC-standard packages
  - 32-pin, 300 mil SOJ
  - 32-pin, 400 mil SOJ
- ESD protection  $\geq 2000$  volts
- Latch-up current  $\geq 200$  mA

Pin arrangement

Logic block diagram



Selection guide

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	110	100	90	80	mA
Maximum CMOS standby current	10	10	10	10	mA



## Functional description

The AS7C1025B is a high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 131,072 x 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 10/12/15/20 ns with output enable access times ( $t_{OE}$ ) of 5/6/7/8 ns are ideal for high-performance applications. The chip enable input  $\overline{CE}$  permits easy memory and expansion with multiple-bank memory systems.

When  $\overline{CE}$  is high, the device enters standby mode. If inputs are still toggling, the device will consume  $I_{SB}$  power. If the bus is static, then full standby power is reached ( $I_{SB1}$ ). For example, the AS7C1026B is guaranteed not to exceed 55 mW under nominal full standby conditions.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and chip enable ( $\overline{CE}$ ). Data on the input pins I/O0 through I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and chip enable ( $\overline{CE}$ ), with write enable ( $\overline{WE}$ ) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5 V supply. The AS7C1025B is packaged in common industry standard packages.

## Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on $V_{CC}$ relative to GND	$V_{t1}$	-0.50	+7.0	V
Voltage on any pin relative to GND	$V_{t2}$	-0.50	$V_{CC} + 0.5$	V
Power dissipation	$P_D$	—	1.0	W
Storage temperature (plastic)	$T_{stg}$	-65	+150	°C
Ambient temperature with $V_{CC}$ applied	$T_{bias}$	-55	+125	°C
DC current into outputs (low)	$I_{OUT}$	—	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	High Z	Output disable ( $I_{CC}$ )
L	H	L	$D_{OUT}$	Read ( $I_{CC}$ )
L	L	X	$D_{IN}$	Write ( $I_{CC}$ )

Key: X = don't care, L = low, H = high.



### Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		$V_{CC}$	4.5	5.0	5.5	V
Input voltage		$V_{IH}$	2.2	–	$V_{CC} + 0.5$	V
		$V_{IL}$	–0.5	–	0.8	V
Ambient operating temperature	commercial	$T_A$	0	–	70	°C
	industrial	$T_A$	–40	–	85	°C

$V_{IL}$  min = –1.0V for pulse width less than 5ns

$V_{IH}$  max =  $V_{CC} + 2.0$ V for pulse width less than 5ns.

### DC operating characteristics (over the operating range)<sup>1</sup>

Parameter	Symbol	Test conditions	–10		–12		–15		–20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{IN} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	μA
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, \overline{CE} = V_{IH}, V_{out} = \text{GND to } V_{CC}$	–	1	–	1	–	1	–	1	μA
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max}$ $\overline{CE} \leq V_{IL}, f = f_{Max}, I_{OUT} = 0 \text{ mA}$	–	110	–	100	–	90	–	80	mA
Standby power supply current <sup>1</sup>	$I_{SB}$	$V_{CC} = \text{Max}$ $\overline{CE} \geq V_{IH}, f = f_{Max}$	–	50	–	45	–	45	–	40	mA
	$I_{SB1}$	$V_{CC} = \text{Max}$ $\overline{CE} \geq V_{CC} - 0.2 \text{ V},$ $V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC} - 0.2 \text{ V},$ $f = 0$	–	10		10		10		10	mA
Output voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	–	0.4	–	0.4	–	0.4	–	0.4	V
	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4		2.4	–	2.4	–	2.4	–	V

### Capacitance ( $f = 1 \text{ MHz}, T_a = 25^\circ \text{ C}, V_{CC} = \text{NOMINAL}$ )<sup>2</sup>

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{CE}$ , $\overline{WE}$ , $\overline{OE}$	$V_{IN} = 0 \text{ V}$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{IN} = V_{OUT} = 0 \text{ V}$	7	pF



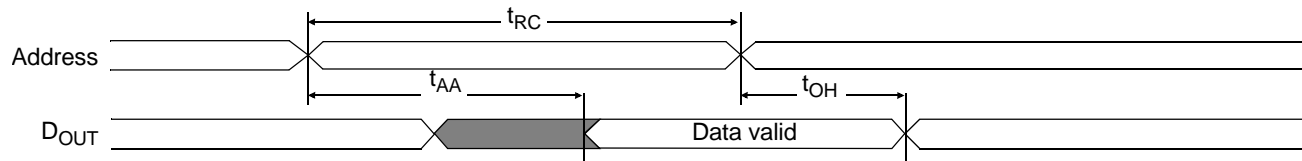
### Read cycle (over the operating range)<sup>3,9</sup>

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	10	-	12	-	15	-	20	-	ns	
Address access time	$t_{AA}$	-	10	-	12	-	15	-	20	ns	3
Chip enable ( $\overline{CE}$ ) access time	$t_{ACE}$	-	10	-	12	-	15	-	20	ns	3
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	-	5	-	6	-	7	-	8	ns	
Output hold from address change	$t_{OH}$	3	-	3	-	3	-	3	-	ns	5
$\overline{CE}$ low to output in low Z	$t_{CLZ}$	3	-	3	-	3	-	3	-	ns	4, 5
$\overline{CE}$ low to output in high Z	$t_{CHZ}$	-	4	-	5	-	6	-	7	ns	4, 5
$\overline{OE}$ low to output in low Z	$t_{OLZ}$	0	-	0	-	0	-	0	-	ns	4, 5
$\overline{OE}$ high to output in high Z	$t_{OHZ}$	-	4	-	5	-	6	-	7	ns	4, 5
Power up time	$t_{PU}$	0	-	0	-	0	-	0	-	ns	4, 5
Power down time	$t_{PD}$	-	10	-	12	-	15	-	20	ns	4, 5

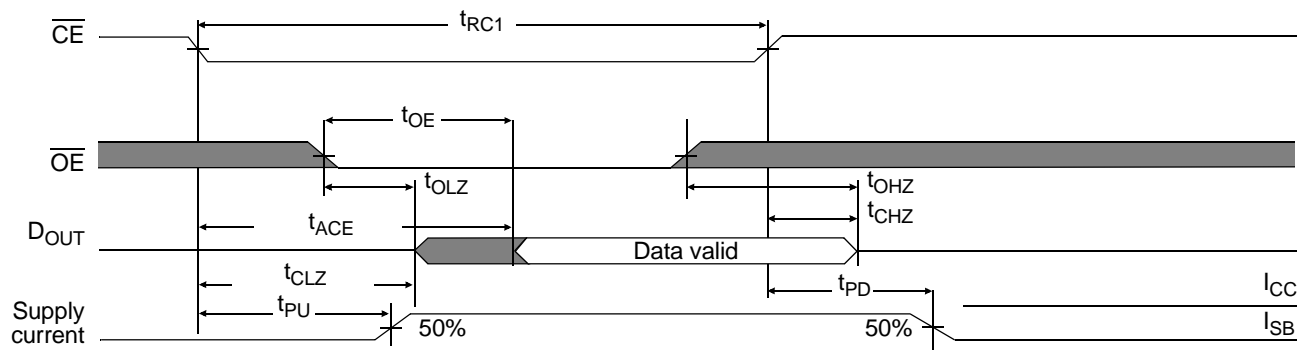
### Key to switching waveforms

Rising input     
 Falling input     
 Undefined/don't care

### Read waveform 1 (address controlled)<sup>3,6,7,9</sup>



### Read waveform 2 ( $\overline{CE}$ and $\overline{OE}$ controlled)<sup>3,6,8,9</sup>

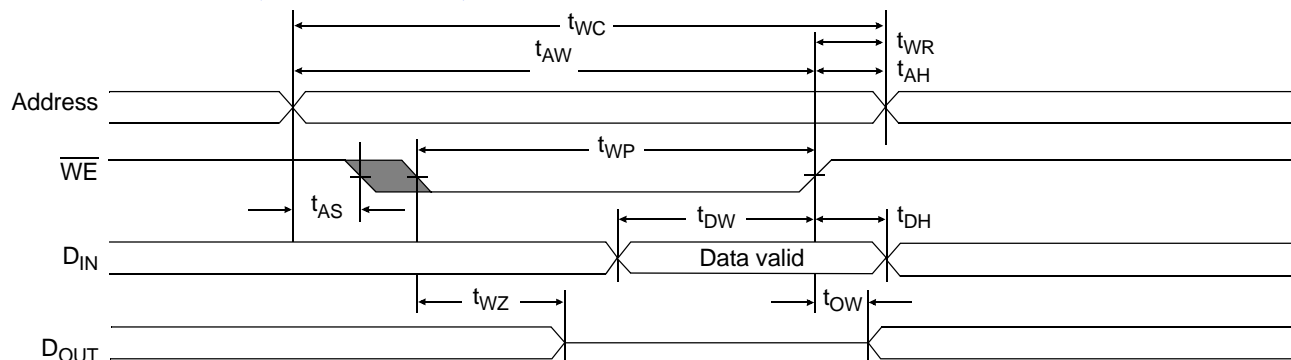




### Write cycle (over the operating range)<sup>11</sup>

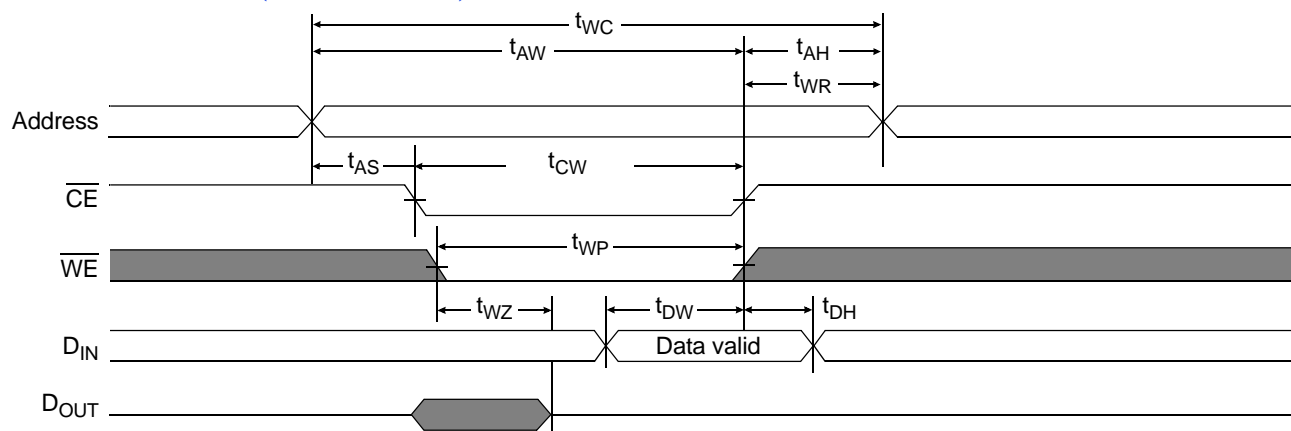
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	10	-	12	-	15	-	20	-	ns	
Chip enable ( $\overline{CE}$ ) to write end	$t_{CW}$	8	-	9	-	10	-	12	-	ns	
Address setup to write end	$t_{AW}$	8	-	9	-	10	-	10	-	ns	
Address setup time	$t_{AS}$	0	-	0	-	0	-	0	-	ns	
Write pulse width	$t_{WP}$	7	-	8	-	9	-	12	-	ns	
Write recovery time	$t_{WR}$	0	-	0	-	0	-	0	-	ns	
Address hold from end of write	$t_{AH}$	0	-	0	-	0	-	0	-	ns	
Data valid to write end	$t_{DW}$	5	-	6	-	8	-	10	-	ns	
Data hold time	$t_{DH}$	0	-	0	-	0	-	0	-	ns	4, 5
Write enable to output in high Z	$t_{WZ}$	-	5	-	6	-	7	-	8	ns	4, 5
Output active from write end	$t_{OW}$	1	-	1	-	1	-	2	-	ns	4, 5

### Write waveform 1 ( $\overline{WE}$ controlled)<sup>10,11</sup>





## Write waveform 2 ( $\overline{\text{CE}}$ controlled)<sup>10,11</sup>



## AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.5 V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5 V.

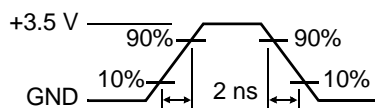


Figure A: Input pulse

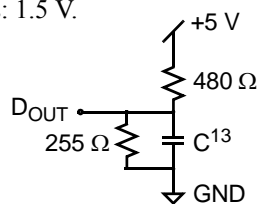
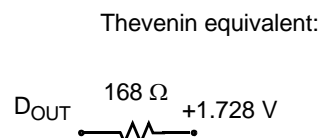


Figure B: 5 V Output load



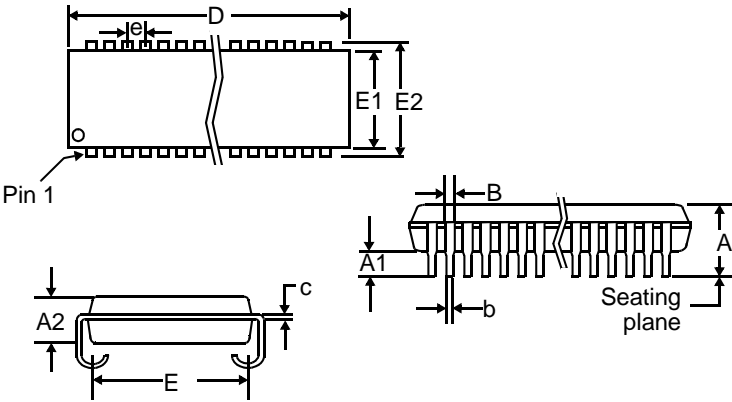
## Notes

- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{\text{CE}}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4  $t_{CLZ}$  and  $t_{CHZ}$  are specified with  $CL = 5$  pF, as in Figure B. Transition is measured  $\pm 500$  mV from steady-state voltage.
- 5 This parameter is guaranteed, but not 100% tested.
- 6  $\overline{\text{WE}}$  is high for read cycle.
- 7  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are low for read cycle.
- 8 Address is valid prior to or coincident with  $\overline{\text{CE}}$  transition low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 N/A.
- 13  $C = 30$  pF, except all high Z and low Z parameters where  $C = 5$  pF.



Package dimensions

32-pin SOJ  
300 mil/400 mil



Symbol	32-pin SOJ 300 mil		32-pin SOJ 400 mil	
	Min	Max	Min	Max
A	0.128	0.145	0.132	0.146
A1	0.025	-	0.025	-
A2	0.095	0.105	0.105	0.115
B	0.026	0.032	0.026	0.032
b	0.016	0.020	0.015	0.020
c	0.007	0.010	0.007	0.013
D	0.820	0.830	0.820	0.830
E	0.255	0.275	0.354	0.378
E1	0.295	0.305	0.395	0.405
E2	0.330	0.340	0.435	0.445
e	0.050 BSC		0.050 BSC	



## Ordering Codes

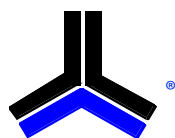
Package \ Access time	Temperature	10 ns	12 ns	15 ns	20 ns
300-mil SOJ	Commercial	AS7C1025B-10TJC	AS7C1025B-12TJC	AS7C1025B-15TJC	AS7C1025B-20TJC
	Industrial	AS7C1025B-10TJI	AS7C1025B-12TJI	AS7C1025B-15TJI	AS7C1025B-20TJI
400-mil SOJ	Commercial	AS7C1025B-10JC	AS7C1025B-12JC	AS7C1025B-15JC	AS7C1025B-20JC
	Industrial	AS7C1025B-10JI	AS7C1025B-12JI	AS7C1025B-15JI	AS7C1025B-20JI

**Note:** Add suffix 'N' to the above part number for LEAD FREE parts. (Ex AS7C1025B-10TJCN)

## Part numbering system

AS7C	1025B	-XX	X	X	X
SRAM prefix	Device number	Access time	Package: TJ = SOJ 300 mil J = SOJ 400 mil	Temperature range C = commercial, 0° C to 70° C I = industrial, -40° C to 85° C	N = LEAD FREE PART





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Part Number: AS7C1025B  
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[AS7C1025B-12TJCNTR](#)