

SN74LS259

8-Bit Addressable Latch

The SN74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- Serial-to-Parallel Conversion
- Eight Bits of Storage With Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

GUARANTEED OPERATING RANGES

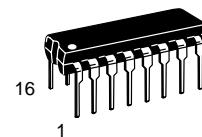
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			-0.4	mA
I_{OL}	Output Current – Low			8.0	mA



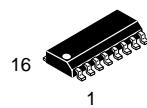
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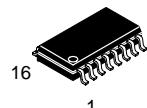
LOW
POWER
SCHOTTKY



PLASTIC
N SUFFIX
CASE 648



SOIC
D SUFFIX
CASE 751B



SOEIAJ
M SUFFIX
CASE 966

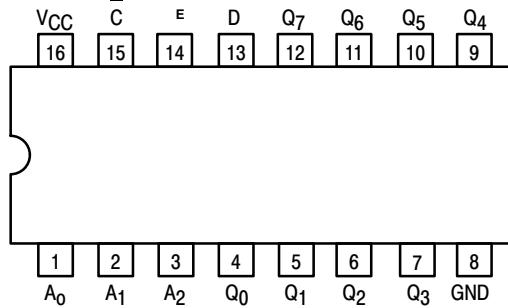
ORDERING INFORMATION

Device	Package	Shipping
SN74LS259N	16 Pin DIP	2000 Units/Box
SN74LS259D	SOIC-16	38 Units/Rail
SN74LS259DR2	SOIC-16	2500/Tape & Reel
SN74LS259M	SOEIAJ-16	See Note 1
SN74LS259MEL	SOEIAJ-16	See Note 1

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

SN74LS259

CONNECTION DIAGRAM DIP (TOP VIEW)



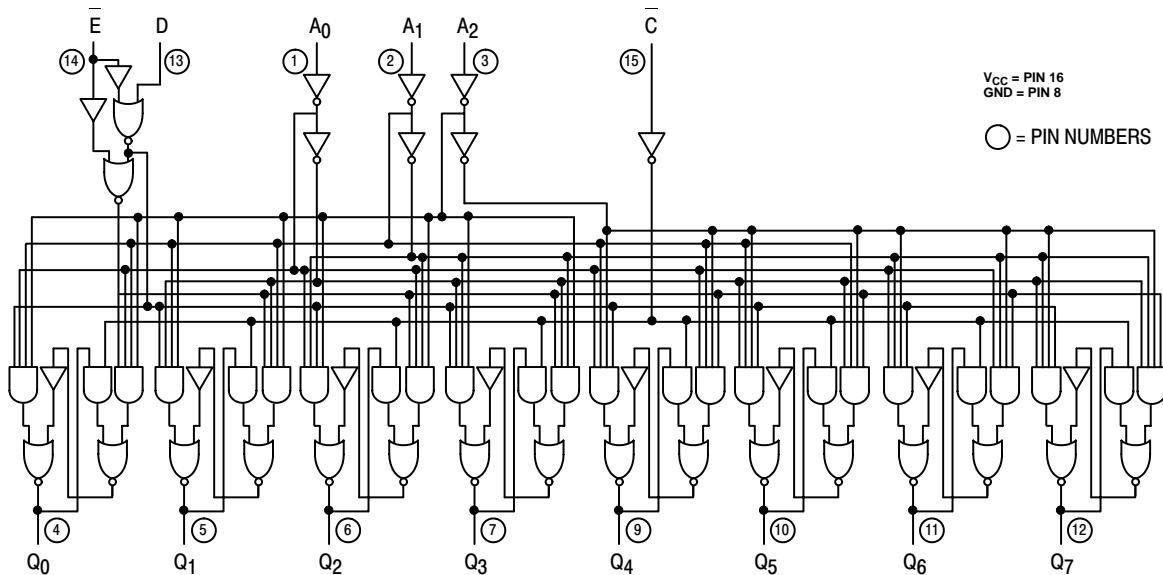
LOADING (Note a)

PIN NAMES	HIGH	LOW
A ₀ , A ₁ , A ₂	0.5 U.L.	0.25 U.L.
D	0.5 U.L.	0.25 U.L.
E	1.0 U.L.	0.5 U.L.
C	0.5 U.L.	0.25 U.L.
Q ₀ - Q ₇	10 U.L.	5 U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all

other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the SN74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations.

MODE SELECTION

		MODE				
E	C					
L	H	Addressable Latch				
H	H	Memory				
L	L	Active HIGH Eight-Channel Demultiplexer				
H	L	Clear				

TRUTH TABLE
PRESENT OUTPUT STATES

C	E	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	MODE		
L	H	X	X	X	X	L	L	L	L	L	L	L	L	L	Clear	
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	L		
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L		
L	L	H	H	L	L	L	H	L	L	L	L	L	L	L		
• • •					•											
• • •					•											
• • •					•											
• • •					•											
L L H H H H H					L L L L L L L L	L	L	L	L	L	L	L	L	H		
H H X X X X X					Q _{N-1}											Memory
H I I L L L L					Q _{N-1}	Addressable Latch										
H L H L L L L					Q _{N-1}	H	Q _{N-1}	Addressable Latch								
H L L H L L L					Q _{N-1}	Q _{N-1}	L	Q _{N-1}	Addressable Latch							
H L H H L L L					Q _{N-1}	Q _{N-1}	Q _{N-1}	H	Q _{N-1}	Addressable Latch						
• • •					•											
• • •					•											
• • •					•											
• • •					•											
H L L H H H H					Q _{N-1}											Q _{N-1} L
H L H H H H H					Q _{N-1}											Q _{N-1} H

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

SN74LS259

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 2)	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			36	mA	$V_{CC} = \text{MAX}$

2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Enable to Output		22	35	ns	
t_{PHL}	Turn-On Delay, Enable to Output		15	24	ns	
t_{PLH}	Turn-Off Delay, Data to Output		20	32	ns	
t_{PHL}	Turn-On Delay, Data to Output		13	21	ns	
t_{PLH}	Turn-Off Delay, Address to Output		24	38	ns	
t_{PHL}	Turn-On Delay, Address to Output		18	29	ns	
t_{PHL}	Turn-On Delay, Clear to Output		17	27	ns	$C_L = 15 \text{ pF}$

AC SET-UP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_s	Input Setup Time	20			ns
t_W	Pulse Width, Clear or Enable	15			ns
t_h	Hold Time, Data	5.0			ns
t_h	Hold Time, Address	20			ns

AC WAVEFORMS

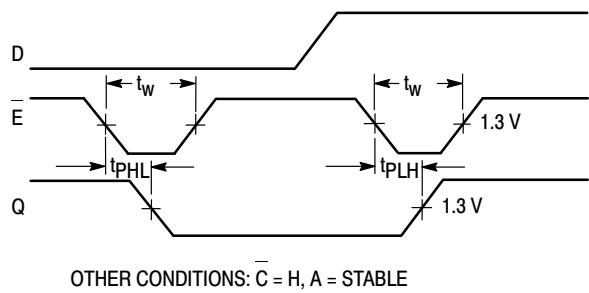


Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width

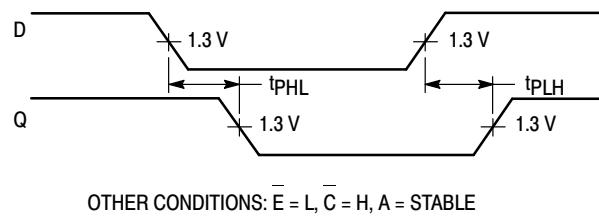


Figure 2. Turn-on and Turn-off Delays, Data to Output

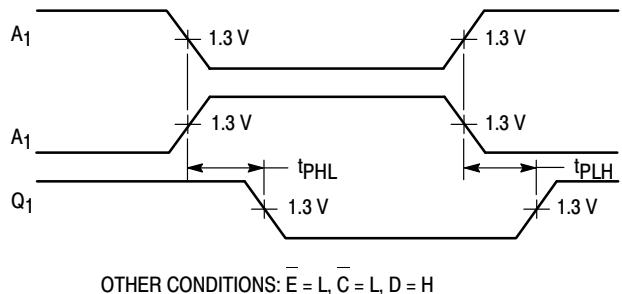


Figure 3. Turn-on and Turn-off Delays, Address to Output

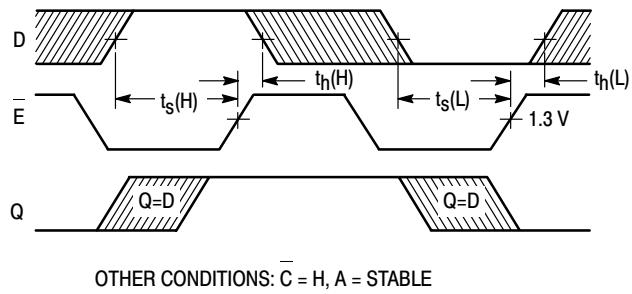


Figure 4. Setup and Hold Time, Data to Enable

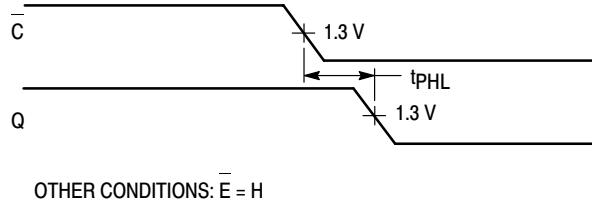


Figure 5. Turn-on Delay, Clear to Output

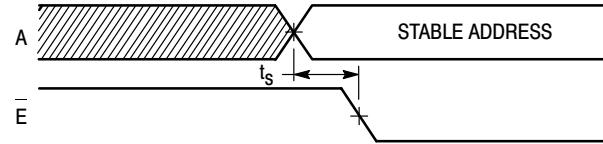


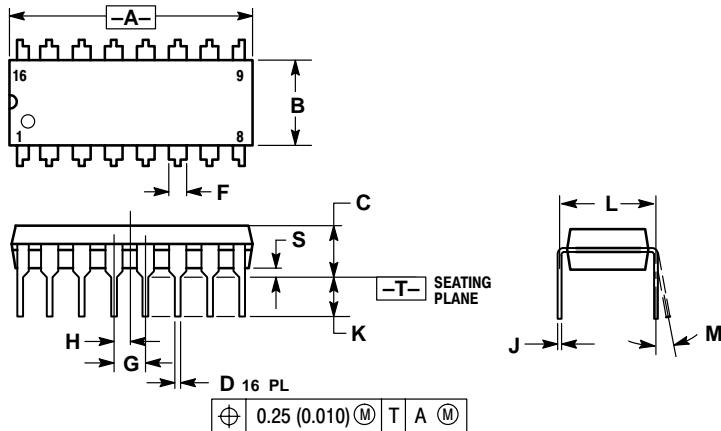
Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)

NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



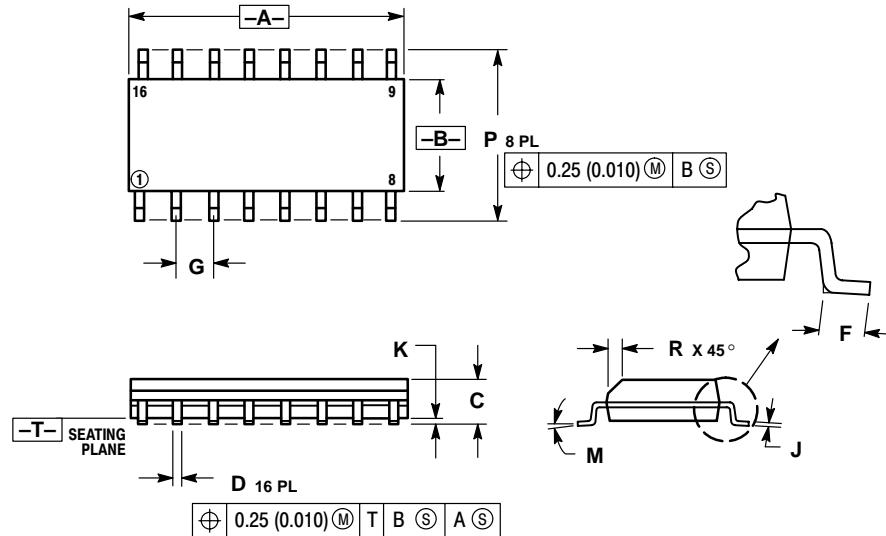
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
H	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



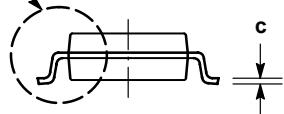
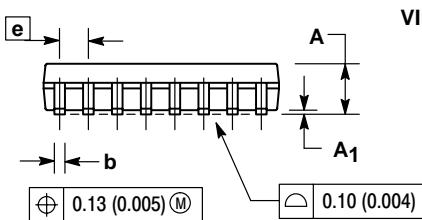
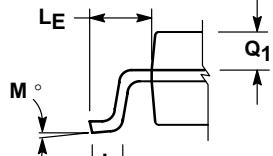
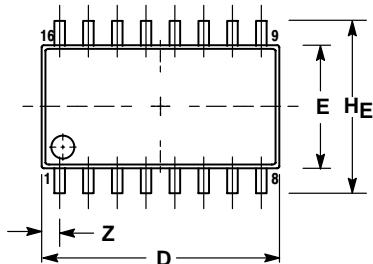
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

M SUFFIX
SOEIAJ PACKAGE
CASE 966-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (D) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27	BSC	0.050	BSC
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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