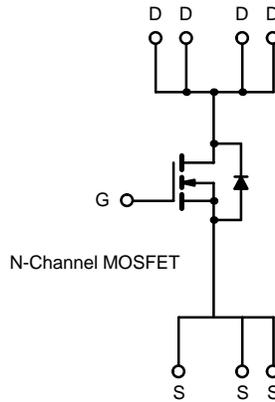
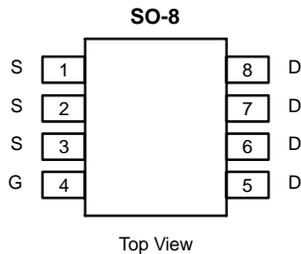




N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0185 @ $V_{GS} = 10$ V	9
	0.033 @ $V_{GS} = 4.5$ V	7

TrenchFET[®]
Power MOSFETs
High-Efficiency
PWM Optimized



Ordering Information: Si4800DY
Si4800DY-T1 (with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 25	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^{a, b}	$T_A = 25^\circ\text{C}$	I_D	9	A
	$T_A = 70^\circ\text{C}$		7	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	40	
Continuous Source Current (Diode Conduction) ^{a, b}		I_S	2.3	
Maximum Power Dissipation ^{a, b}	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^a	$t \leq 10$ sec	R_{thJA}		50	$^\circ\text{C/W}$
	Steady State		70		

Notes
a. Surface Mounted on FR4 Board.
b. $t \leq 10$ sec.

MOSFET SPECIFICATIONS (T_J = 25° C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.8			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55° C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 9 A		0.0155	0.0185	Ω
		V _{GS} = 4.5 V, I _D = 7 A		0.0275	0.033	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 9 A		16		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.3 A, V _{GS} = 0 V		0.71	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 5.0 V, I _D = 9 A		8.7	13	nC
Gate-Source Charge	Q _{gs}			2.25		
Gate-Drain Charge	Q _{gd}			4.2		
Gate Resistance	R _g		0.5	1.5	2.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D = 1 A, V _{GEN} = 10 V, R _G = 6 Ω		11	16	ns
Rise Time	t _r			8	15	
Turn-Off Delay Time	t _{d(off)}			22	30	
Fall Time	t _f			9	15	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.3 A, di/dt = 100 A/μs		50	80	

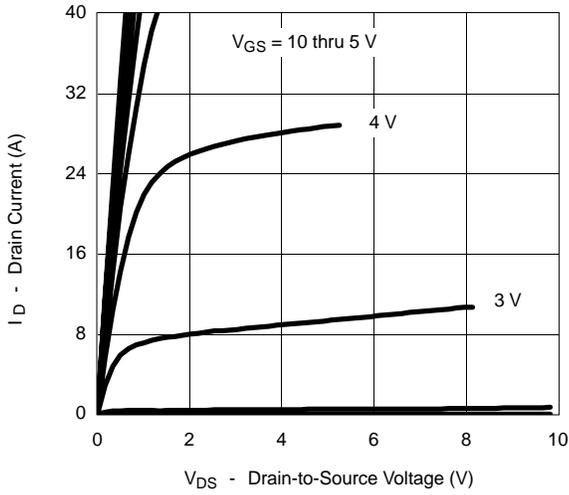
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

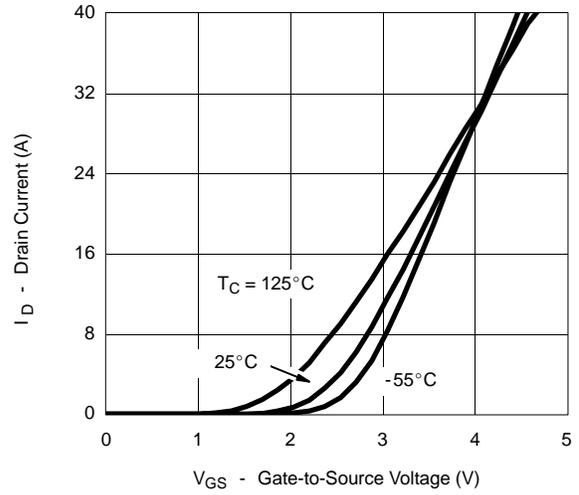


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

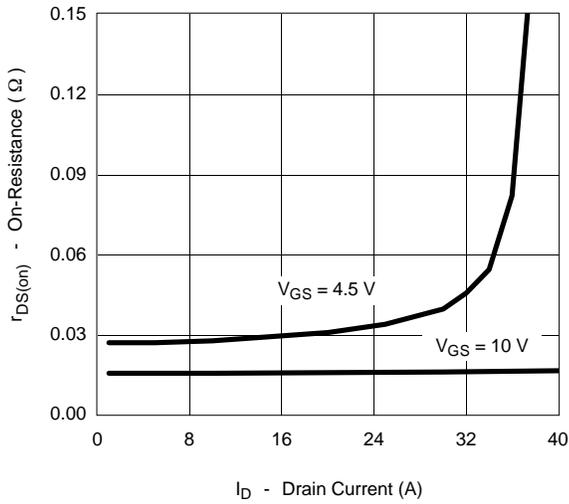
Output Characteristics



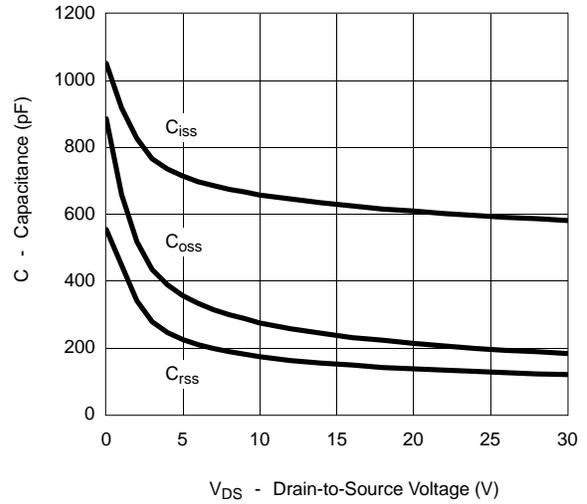
Transfer Characteristics



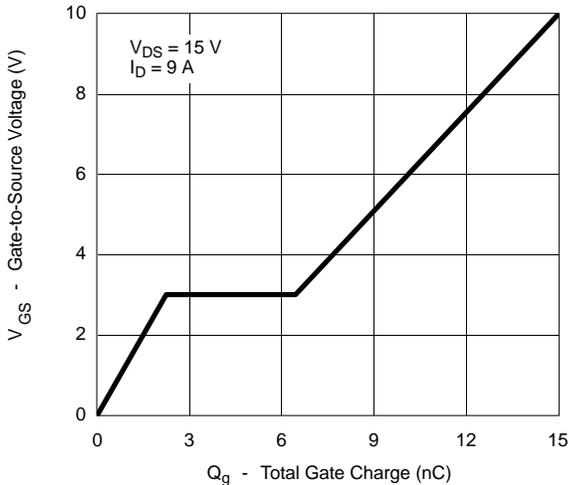
On-Resistance vs. Drain Current



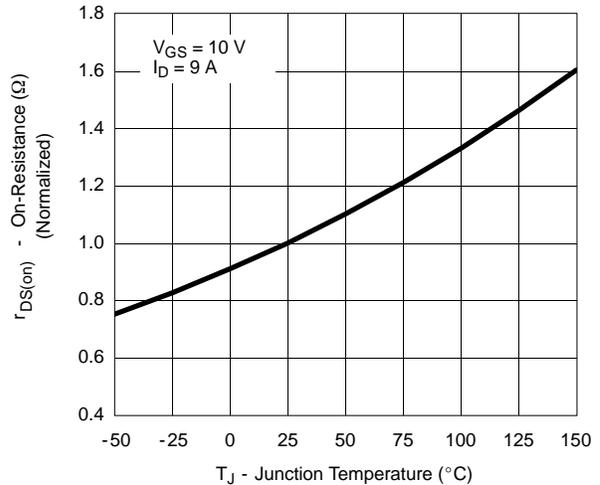
Capacitance



Gate Charge

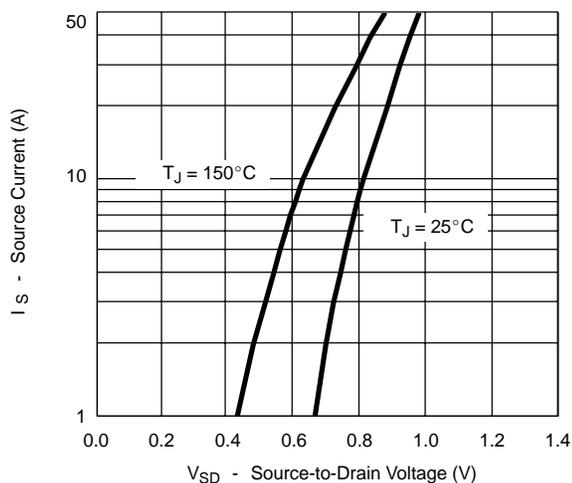


On-Resistance vs. Junction Temperature

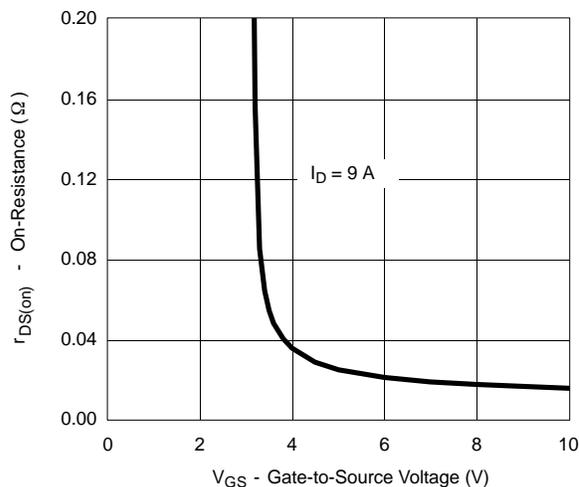


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

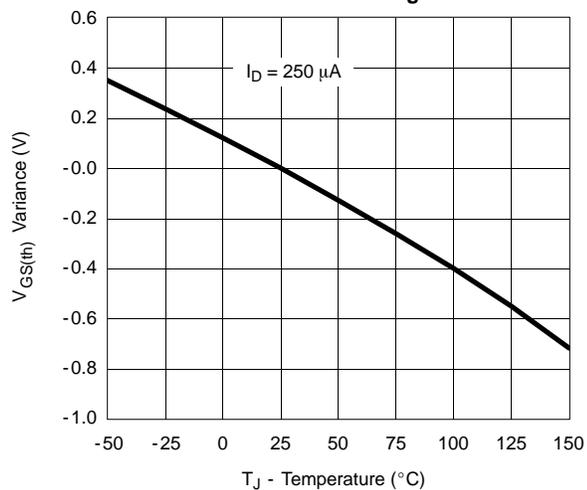
Source-Drain Diode Forward Voltage



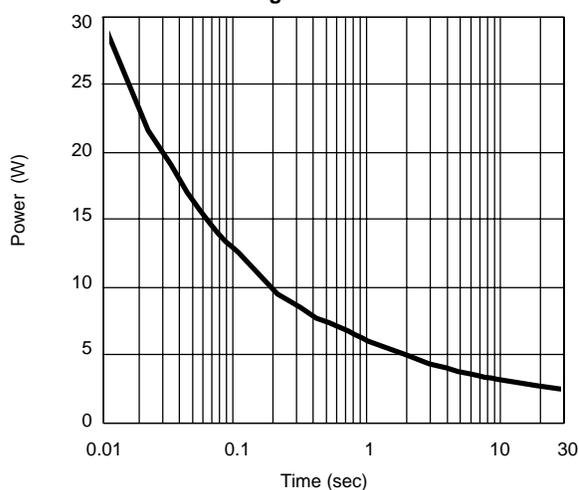
On-Resistance vs. Gate-to-Source Voltage



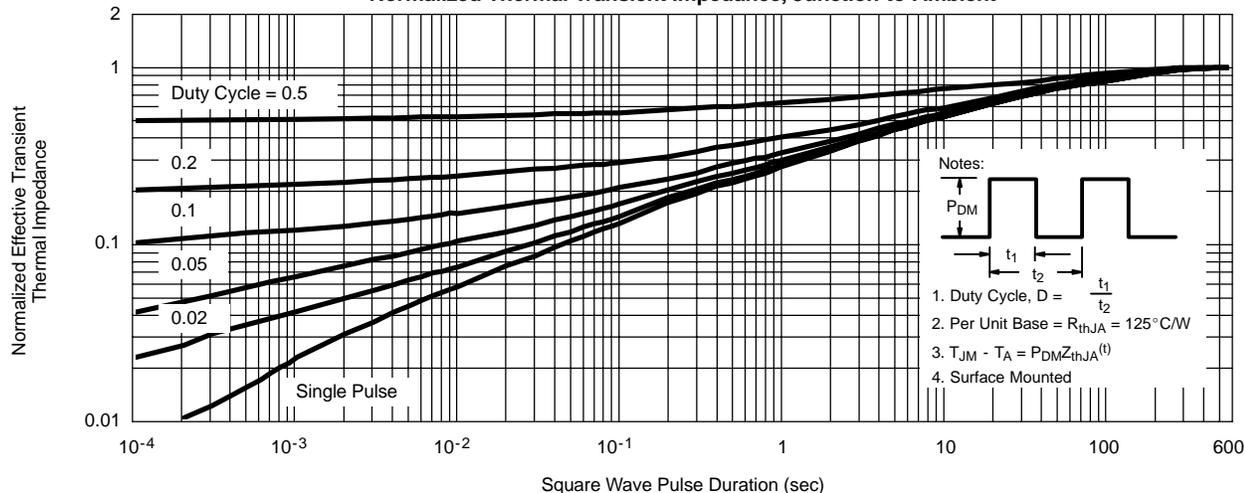
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient





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