

Octal buffer/line driver; 3-state; inverting

74LVC240

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines @ 85 °C

DESCRIPTION

The 74LVC240 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC240 is an octal inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The '240' is identical to the '244' but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA _n	nY _n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	C _L = 50 pF V _{CC} = 3.3 V	4.6	ns
C _I	input capacitance		5.0	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC240D	20	SO	plastic	SO20/SOT163A
74LVC240DB	20	SSOP	plastic	SSOP20/SOT339
74LVC240PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1OE	output enable input (active LOW)
2, 4, 6, 8	1A ₀ to 1A ₃	data inputs
3, 5, 7, 9	2Y ₀ to 2Y ₃	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A ₀ to 2A ₃	data inputs
18, 16, 14, 12	1Y ₀ to 1Y ₃	bus outputs
19	2OE	output enable input (active LOW)
20	V _{CC}	positive power supply

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74LVC240

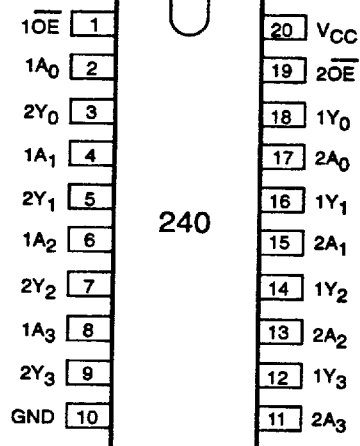


Fig.1 Pin configuration.

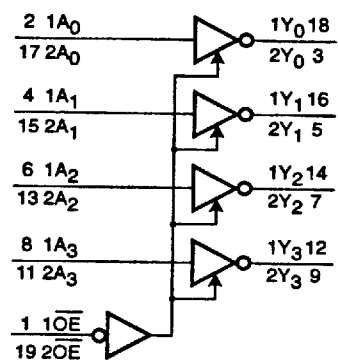


Fig.2 Logic symbol.

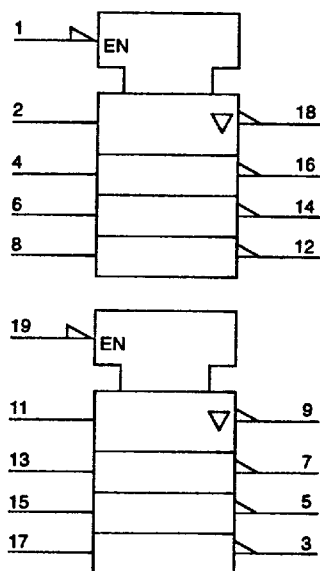


Fig.3 IEC logic symbol.

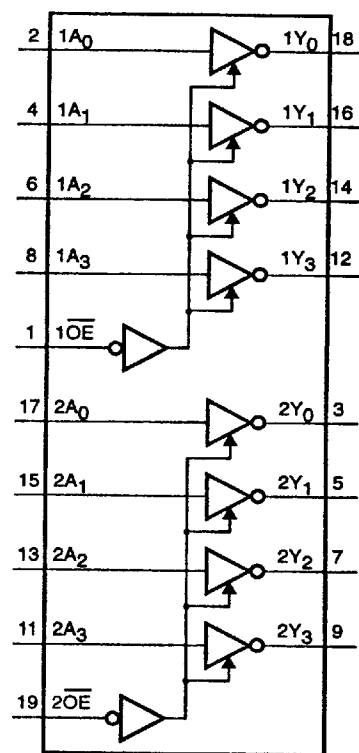


Fig.4 Functional diagram.

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74LVC240

DC CHARACTERISTICS FOR 74LVC240

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

 I_{CC} category: MSI**AC CHARACTERISTICS FOR 74LVC240**GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

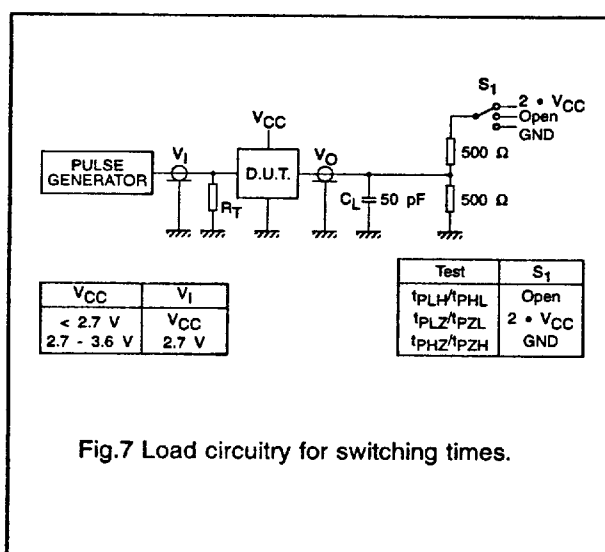
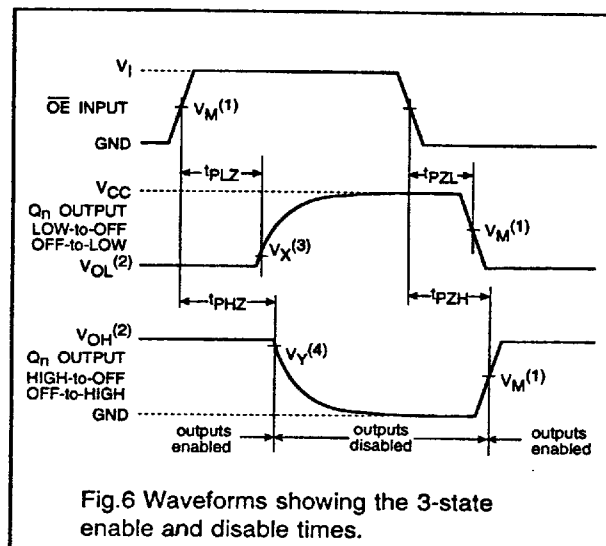
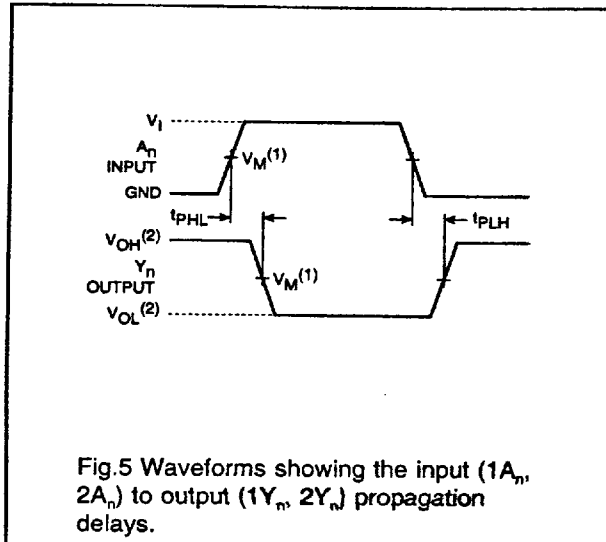
SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	– 1.5 1.5	21 4.8 4.6*	– 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time 1OE to 1Y _n ; 2OE to 2Y _n	– 1.5 1.5	42 6.3 6.0*	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time 1OE to 1Y _n ; 2OE to 2Y _n	– 1.5 1.5	6.5 3.4 3.3*	– 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Figs 6, 7

Notes: All typical values are measured at $T_{amb} = 25$ °C.* Typical values are measured at $V_{CC} = 3.3$ V.

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AC WAVEFORMS



- Notes:
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 - (3) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$