LMV7235/LMV7239/LMV7239Q 75 nsec, Ultra Low Power, Low Voltage, Rail-to-Rail Input Comparator with Open-Drain/Push-Pull Output

Check for Samples: LMV7235, LMV7239

FEATURES

- **(V_S = 5V, T_A = 25°C**
- **Typical values unless otherwise specified)**
- **Propagation delay 75 nsec**
- **Low supply current 65µA**
- **Rail-to-Rail input**
- **Open drain and push-pull output**
- **Ideal for 2.7V and 5V single supply applications**
- **Available in space saving packages**
  - **5-pin SOT-23**
  - **5-pin SC70**
- **LMV7239Q is an automotive grade product that is AECQ grade 1 qualified and is manufactured on an automotive grade flow.**

APPLICATIONS

- **Portable and battery powered systems**
- **Scanners**
- **Set top boxes**
- **High speed differential line receiver**
- **Window comparators**
- **Zero-crossing detectors**
- **High speed sampling circuits**
- **Automotive**

DESCRIPTION

The LMV7235/LMV7239/LMV7239Q are ultra low power, low voltage, 75 nsec comparators. They are guaranteed to operate over the full supply voltage range of 2.7V to 5.5V. These devices achieve a 75 nsec propagation delay while consuming only 65µA of supply current at 5V.

The LMV7235/LMV7239/LMV7239Q have a greater than rail-to-rail common mode voltage range. The input common mode voltage range extends 200mV below ground and 200mV above supply, allowing both ground and supply sensing.

The LMV7235 features an open drain output. By connecting an external resistor, the output of the comparator can be used as a level shifter.

The LMV7239/LMV7239Q features a push-pull output stage. This feature allows operation without the need of an external pull-up resistor.

The LMV7235/LMV7239/LMV7239Q are available in the 5-Pin SC70 and 5-Pin SOT-23 packages, which are ideal for systems where small size and low power is critical.

Typical Application

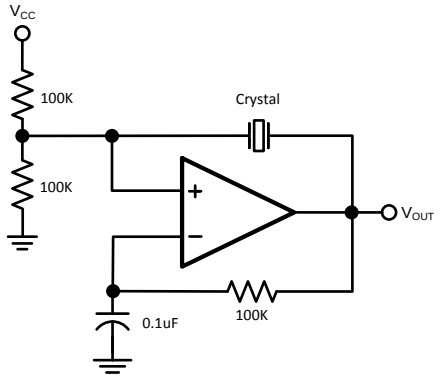


Figure 1. Crystal Oscillator

Connection Diagram

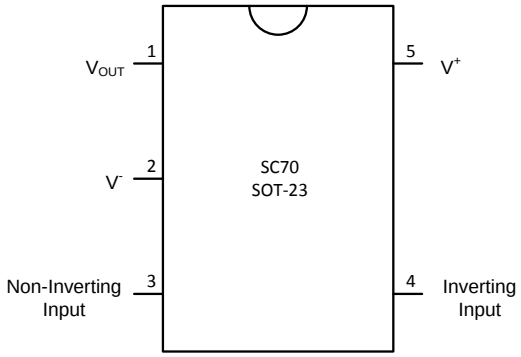
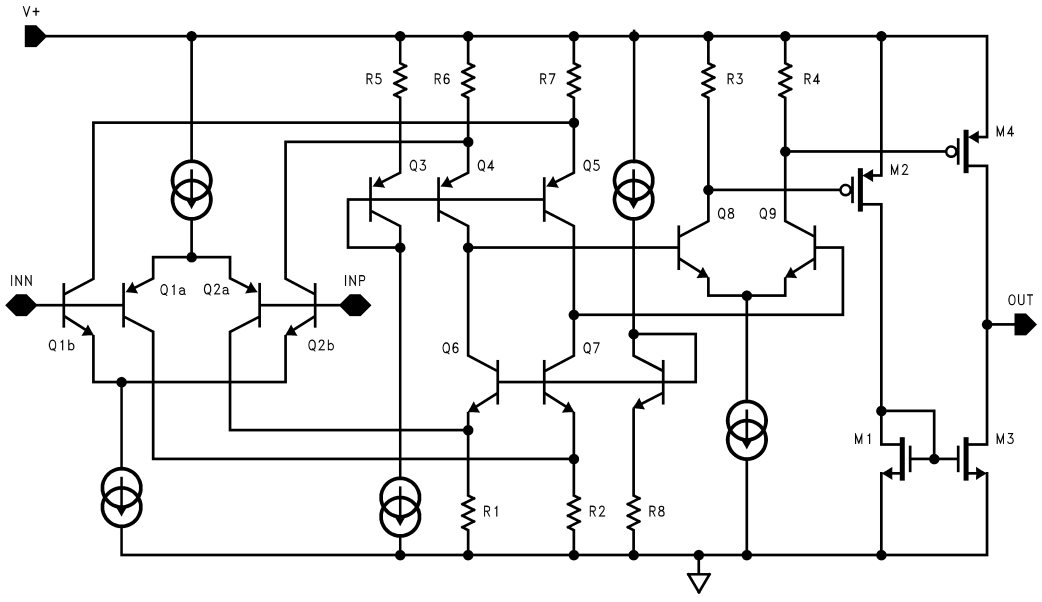


Figure 2. 5-Pin SC70/SOT-23 (Top View)

Simplified Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Model Body	1000V
Machine Body	100V
Differential Input Voltage	± Supply Voltage
Output Short Circuit Duration	(4)
Supply Voltage (V^+ - V^-)	6V
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C (lead temp)
Voltage at Input/Output Pins	(V^+) +0.3V, (V^-) −0.3V
Current at Input Pin (5)	±10mA

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the *Electrical Characteristics.*

(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**

(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.

(5) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Operating Ratings

Supply Voltages (V^+ - V^-)	2.7V to 5.5V
Temperature Range (1)	
LMV7235/LMV7239	−40°C to +85°C
LMV7239Q	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Thermal Resistance	
5-Pin SC70	478°C/W
5-Pin SOT-23	265°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, $V_{CM} = V^+/2$, V^+ = 2.7V, V^- = 0V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			0.8	6 **8**	mV
I_B	Input Bias Current			30	400 **600**	nA
I_{OS}	Input Offset Current			5	200 **400**	nA

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{CM} = V^+/2, V^+ = 2.7V, V^- = 0V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 2.7V (3)	52	62		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB	V^- −0.1**V⁻**	−0.2 to 2.9	V^+ +0.1**V⁺**	V
V_O	Output Swing High (LMV7239 only)	I_L = 4mA, V_{ID} = 500mV	V^+ −0.35	V^+ −0.26		V
		I_L = 0.4mA, V_{ID} = 500mV		V^+ −0.02		V
	Output Swing Low (LMV7235/LMV7239/LMV7239Q)	I_L = −4mA, V_{ID} = −500mV		230	350 **450**	mV
		I_L = −0.4mA, V_{ID} = −500mV		15		mV
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (LMV7239 only) (4)		15		mA
		Sinking, V_O = 2.7V (LMV7235, R_L = 10k) (4)		20		mA
I_S	Supply Current	No load		52	85 **100**	µA
t_{PD}	Propagation Delay	Overdrive = 20mV C_{LOAD} = 15pF (5)		96		ns
		Overdrive = 50mV C_{LOAD} = 15pF (5)		87		ns
		Overdrive = 100mV C_{LOAD} = 15pF (5)		85		ns
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	Overdrive = 20mV (6)		2		ns
t_r	Output Rise Time	LMV7239/LMV7239Q 10% to 90%		1.7		ns
		LMV7235 10% to 90% (5)		112		ns
t_f	Output Fall Time	90% to 10%		1.7		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)			3		nA

(3) CMRR is not linear over the common mode range. Limits are guaranteed over the worst case from 0 to $V_{CC/2}$ or $V_{CC/2}$ to V_{CC}.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(5) A 10k pull-up resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.
(6) Propagation Delay Skew is defined as the absolute value of the difference between t_{PDLH} and t_{PDHL}.

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{CM} = V^+/2, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Limits (1)	Units
V_{OS}	Input Offset Voltage			1	6 **8**	mV
I_B	Input Bias Current			30	400 **600**	nA
I_{OS}	Input Offset Current			5	200 **400**	nA
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 5V	52	67		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	65	85		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB	V^- −0.1**V**$^-$	−0.2 to 5.2	V^+ +0.1**V**$^+$	V
V_O	Output Swing High (LMV7239 only)	I_L = 4mA, V_{ID} = 500mV	V^+ −0.25	V^+ −0.15		V
		I_L = 0.4mA, V_{ID} = 500mV		V^+ −0.01		V
	Output Swing Low (LMV7235/LMV7239/LMV7239Q)	I_L = −4mA, V_{ID} = −500mV		230	350 **450**	mV
		I_L = −0.4mA, V_{ID} = −500mV		10		mV
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (LMV7239 only) (3)	25 **15**	55		mA
		Sinking, V_O = 5V (LMV7235, R_L = 10k) (3)	30 **20**	60		mA
I_S	Supply Current	No load		65	95 **110**	µA
t_{PD}	Propagation Delay	Overdrive = 20mV C_{LOAD} = 15pF (4)		89		ns
		Overdrive = 50mV C_{LOAD} = 15pF (4)		82		ns
		Overdrive = 100mV C_{LOAD} = 15pF (4)		75		ns
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	Overdrive = 20mV (5)		1		ns
t_r	Output Rise Time	LMV7239 10% to 90%		1.2		ns
		LMV7235 10% to 90% (4)		100		ns
t_f	Output Fall Time	90% to 10%		1.2		ns
$I_{LEAKAGE}$	Output Leakeage Current (LMV7235 only)			3		nA

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(4) A 10k pull-up resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.
(5) Propagation Delay Skew is defined as the absolute value of the difference between t_{PDLH} and t_{PDHL}.

TYPICAL PERFORMANCE CHARACTERISTICS

(Unless otherwise specified, V_S = 5V, C_L = 10pF, T_A = 25°C).

Supply Current vs. Supply Voltage

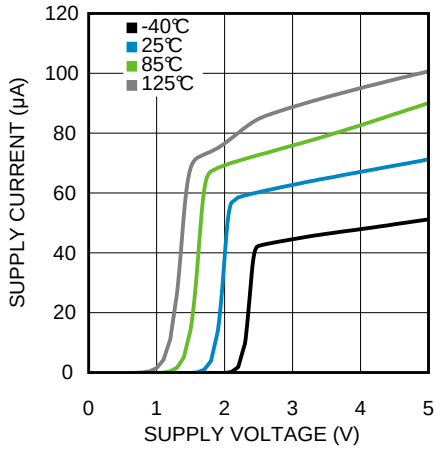


Figure 3.

Sourcing Current vs. Output Voltage

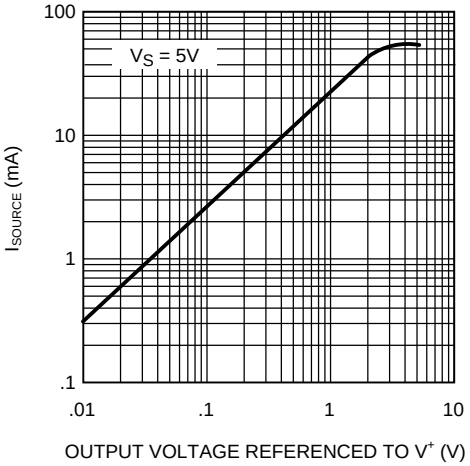


Figure 4.

Sourcing Current vs. Output Voltage

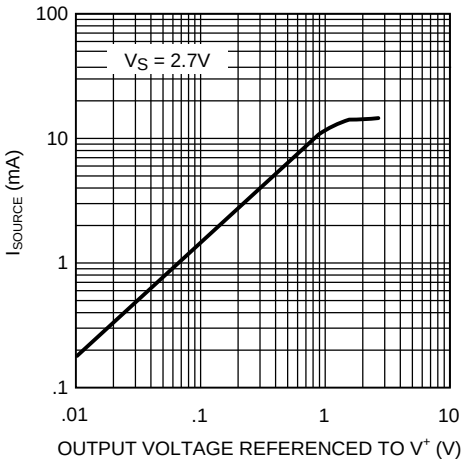


Figure 5.

Sinking Current vs. Output Voltage

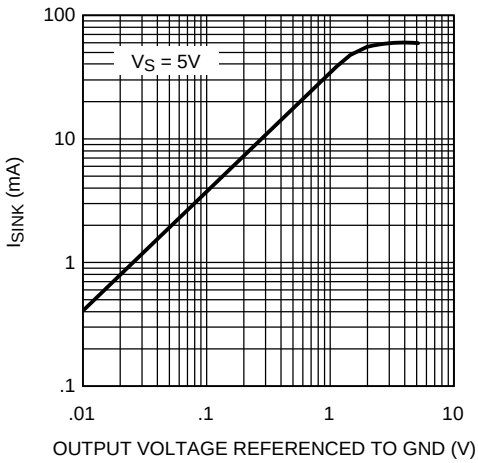


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Unless otherwise specified, V_S = 5V, C_L = 10pF, T_A = 25°C).

Sinking Current vs. Output Voltage

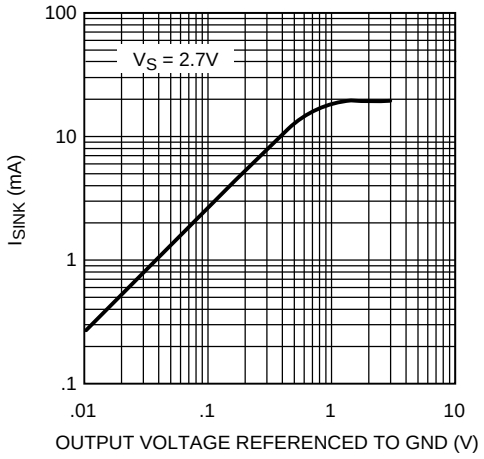


Figure 7.

Input Bias Current vs. Input Voltage

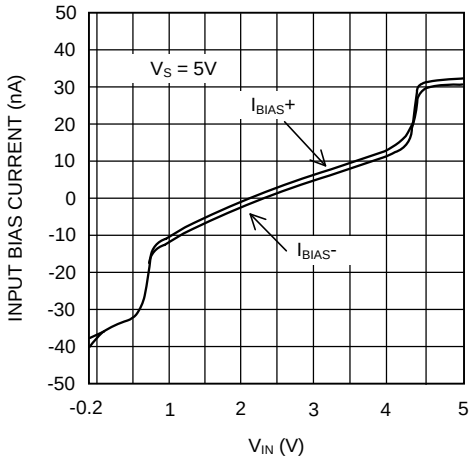


Figure 8.

Input Bias Current vs. Input Voltage

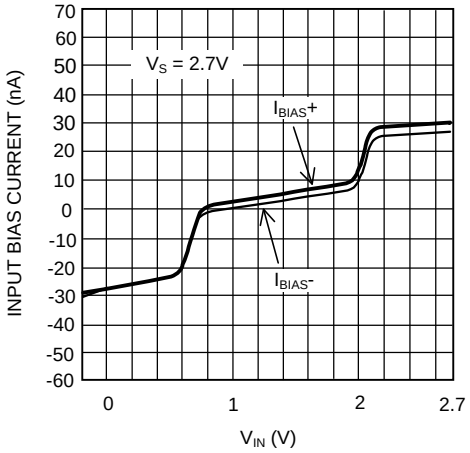


Figure 9.

Propagation Delay vs. Temperature

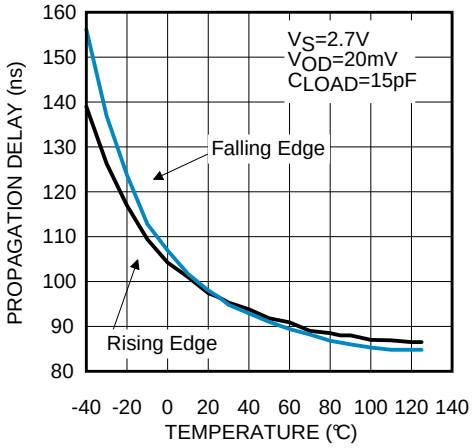


Figure 10.

Propagation Delay vs. Temperature

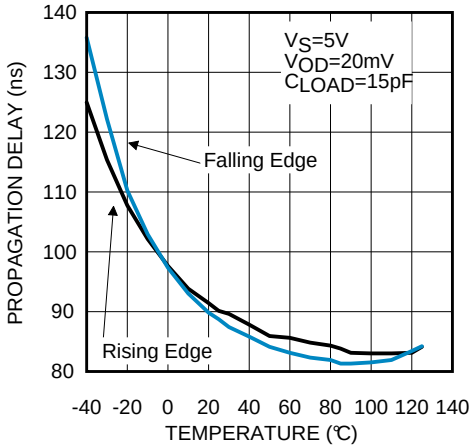


Figure 11.

Propagation Delay vs. Capacitive Load

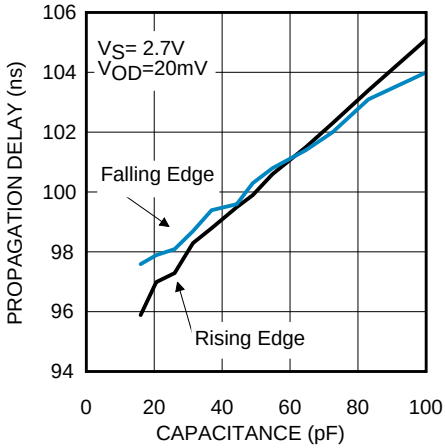


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Unless otherwise specified, V_S = 5V, C_L = 10pF, T_A = 25°C).

Propagation Delay vs. Capacitive Load

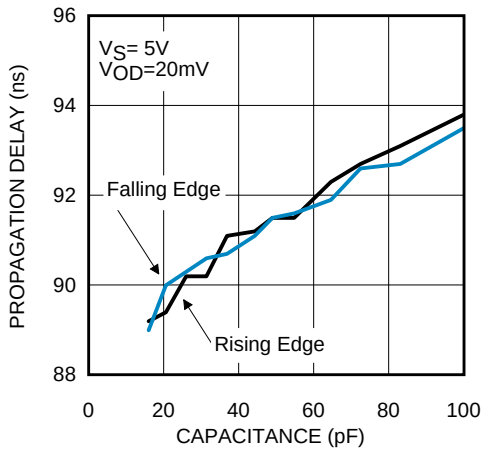


Figure 13.

Propagation Delay vs. Input Overdrive

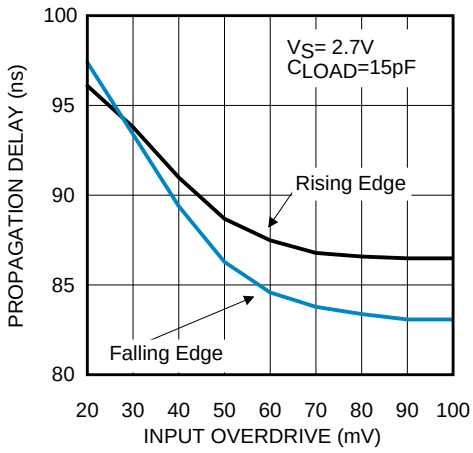


Figure 14.

Propagation Delay vs. Input Overdrive

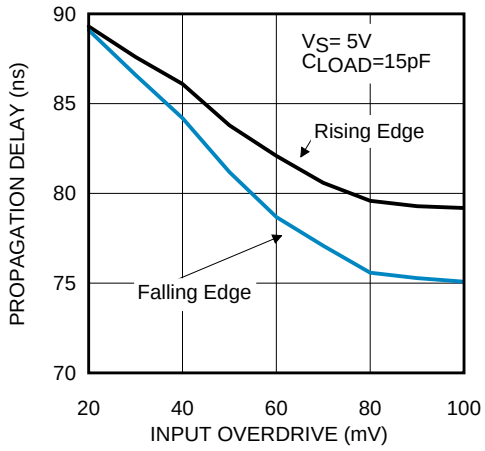


Figure 15.

Propagation Delay vs. Common Mode Voltage

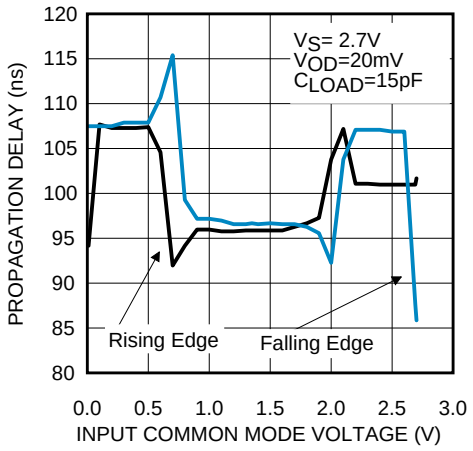


Figure 16.

Propagation Delay vs. Common Mode Voltage

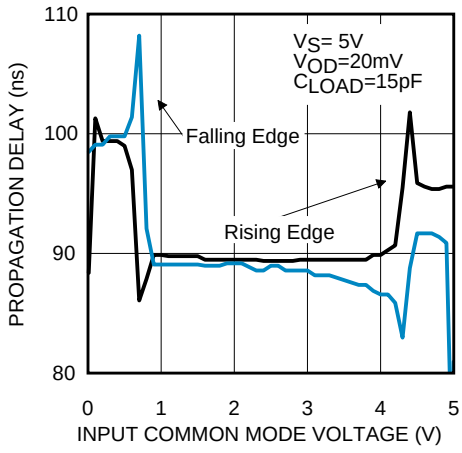


Figure 17.

APPLICATION INFORMATION

The LMV7235/LMV7239/LMV7239Q are single supply comparators with 75ns of propagation delay and only 65µA of supply current.

The LMV7235/LMV7239/LMV7239Q are rail-to-rail input and output. The typical input common mode voltage range of −0.2V below the ground to 0.2V above the supply. The LMV7235/LMV7239/LMV7239Q use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near V^- and the NPN stage senses common mode voltage near V^+. If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on resulting in an increase of input bias current.

If one of the input goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

The LMV7239 has a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing high output sinking or sourcing current during the transition. After the transition, the output current decreases and the supply current settles back to about 65µA at 5V, thus conserving power consumption.

The LMV7235 has an open drain that requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage.

CIRCUIT LAYOUT AND BYPASSING

The LMV7235/LMV7239/LMV7239Q require high speed layout. Follow these layout guidelines:

1. Use printed circuit board with a good, unbroken low-inductance ground plane.

2. Place a decoupling capacitor (0.1µF ceramic surface mount capacitor) as close as possible to V_{CC} pin.

3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from output.

4. Solder the device directly to the printed circuit board rather than using a socket.

5. For slow moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to t_{PD} when the source impedance is low.

6. The topside ground plane runs between the output and inputs.

7. Ground trace from the ground pin runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

COMPARATOR WITH HYSTERESIS

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis or positive feedback.

INVERTING COMPARATOR WITH HYSTERESIS

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V_{CC} of the comparator, as shown in Figure 18. When V_{IN} at the inverting input is less than V_A, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1||R3 in series with R2. The lower input trip voltage V_{A1} is defined as:

$$V_{A1} = V_{CC}R2 / [(R1||R3) + R2] \quad (1)$$

When V_{IN} is greater than V_A ($V_{IN} > V_A$), the output voltage is low, very close to ground. In this case the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage V_{A2} is defined as:

$$V_{A2} = V_{CC} (R2||R3) / [(R1)+ (R2||R3)] \quad (2)$$

The total hysteresis provided by the network is defined as:

$$\text{Delta } V_A = V_{A1} - V_{A2} \quad (3)$$

To assure that the comparator will always switch fully to V_{CC} and not be pulled down by the load the resistors, values should be chosen as follows:

$$R_{PULL\text{-}UP} << R_{LOAD} \quad (4)$$

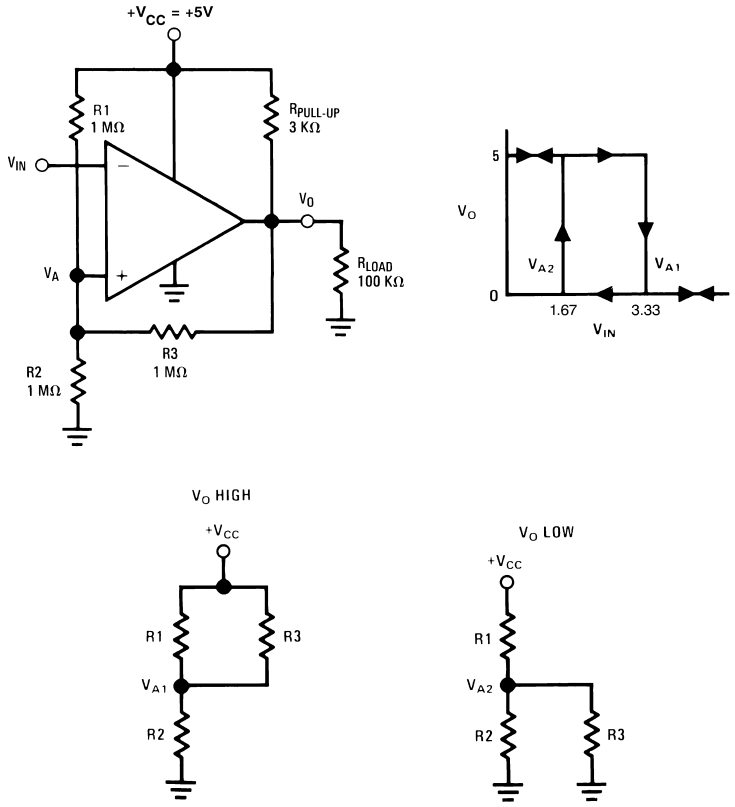


Figure 18. Inverting Comparator with Hysteresis

NON-INVERTING COMPARATOR WITH HYSTERESIS

A non inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by:

$$V_{IN1} = R1*(V_{REF} / R2) + V_{REF} \quad (5)$$

When V_{IN} is high, the output is also high, to make the comparator switch back to it's low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN} can be calculated by:

$$V_{IN2} = [V_{REF} (R1+ R2) - V_{CC} R1] / R2 \quad (6)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\text{Delta } V_{IN} = V_{CC} R1 / R2 \quad (7)$$

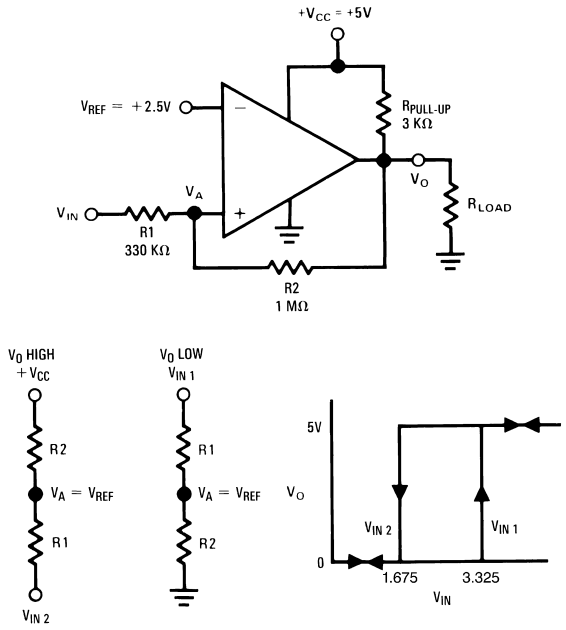


Figure 19. Non-Inverting Comparator with Hysteresis

ZERO-CROSSING DETECTOR

The inverting input is connected to ground and the non-inverting input is connected to 100mVp-p signal. As the signal at the non-inverting input crosses 0V, the comparator's output changes state.

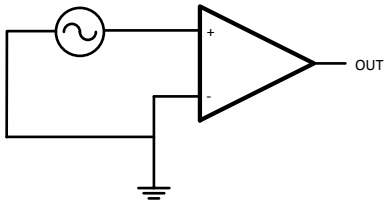


Figure 20. Zero-Crossing Detector

THRESHOLD DETECTOR

Instead of tying the inverting input to 0V, the inverting input can be tied to a reference voltage. The non-inverting input is connected to the input. As the input passes the V_{REF} threshold, the comparator's output changes state.

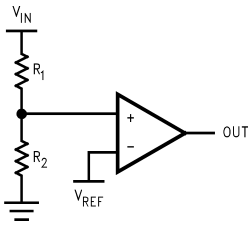


Figure 21. Threshold Detector

CRYSTAL OSCILLATOR

A simple crystal oscillator using the LMV7239 is shown below. Resistors R1 and R2 set the bias point at the comparator's non-inverting input. Resistors R3, R4 and C1 sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator offset.

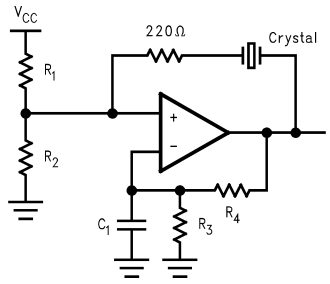


Figure 22. Crystal Oscillator

IR RECEIVER

The LMV7239 is an ideal candidate to be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions.

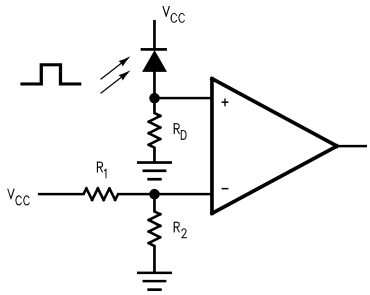


Figure 23. IR Receiver

REVISION HISTORY

Changes from Revision L (February 2013) to Revision M	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7235M5	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C21A	Samples
LMV7235M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C21A	Samples
LMV7235M5X	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	C21A	Samples
LMV7235M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C21A	Samples
LMV7235M7	ACTIVE	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C21	Samples
LMV7235M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C21	Samples
LMV7235M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C21	Samples
LMV7239M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C20A	
LMV7239M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C20A	Samples
LMV7239M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	C20A	
LMV7239M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C20A	Samples
LMV7239M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C20	
LMV7239M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C20	Samples
LMV7239M7X	NRND	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 85	C20	
LMV7239M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	C20	Samples
LMV7239QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	ZBMX	Samples
LMV7239QM7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	C42	Samples
LMV7239QM7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	C42	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMV7239, LMV7239-Q1 :

- Catalog: LMV7239
- Automotive: LMV7239-Q1

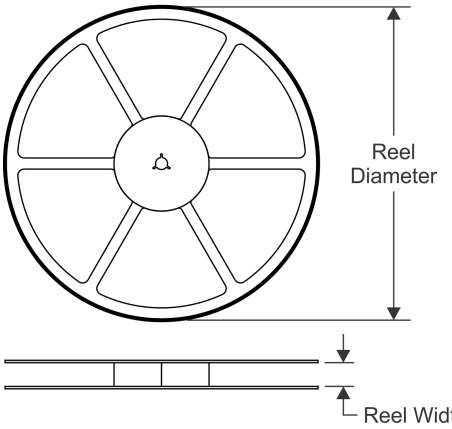
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

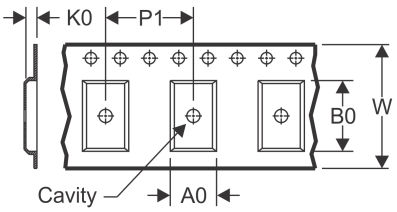
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

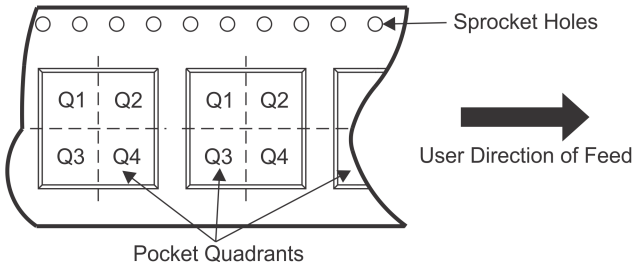


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

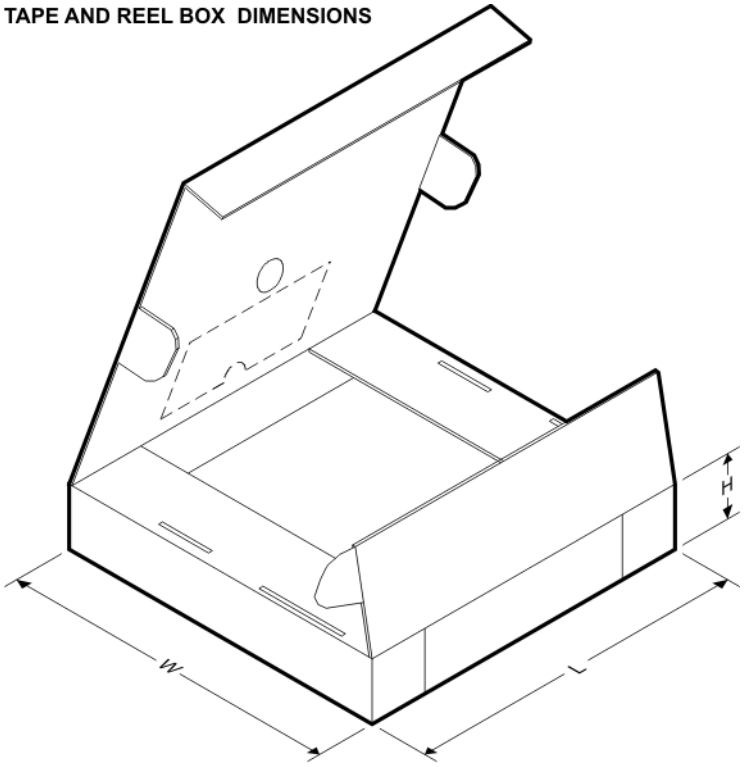
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7235M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7235M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7235M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7235M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239QDBVRQ1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7239QM7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7239QM7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

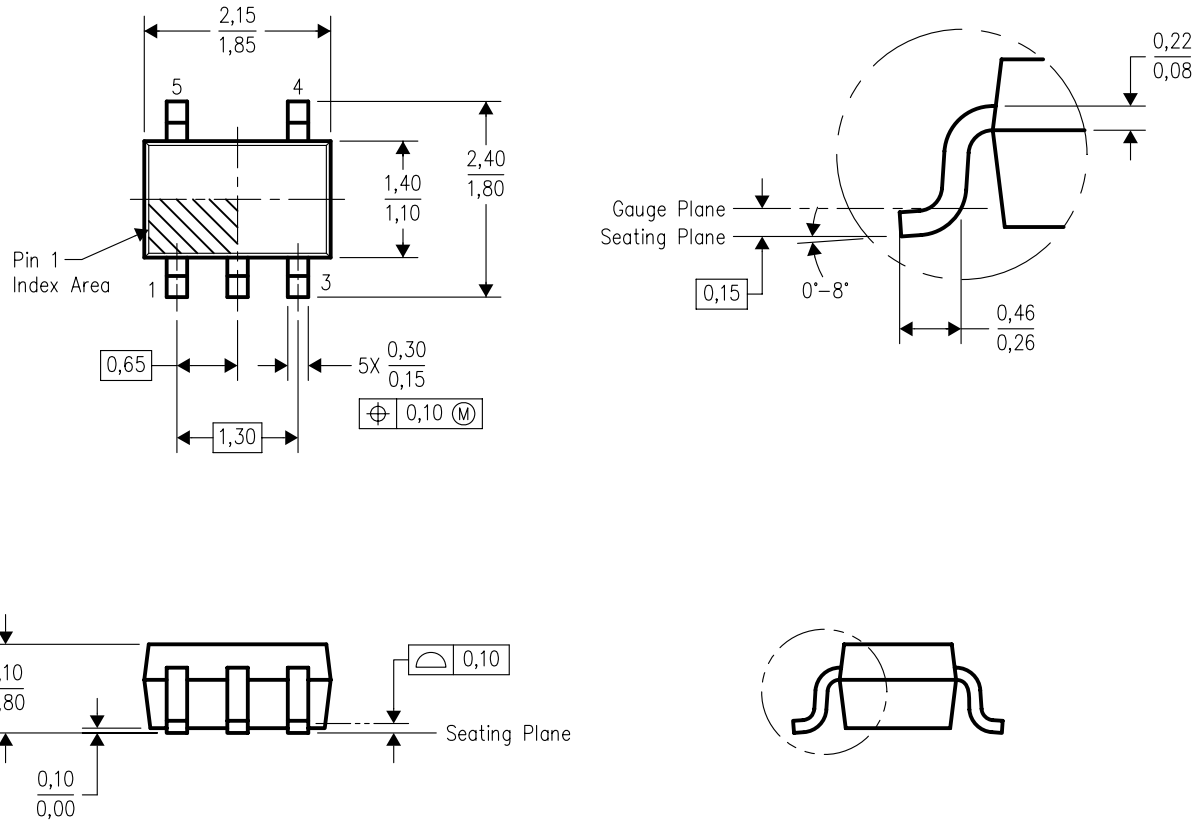
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7235M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7235M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7235M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7235M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7235M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7235M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7235M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7239M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7239M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239M7X	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7239QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7239QM7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7239QM7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

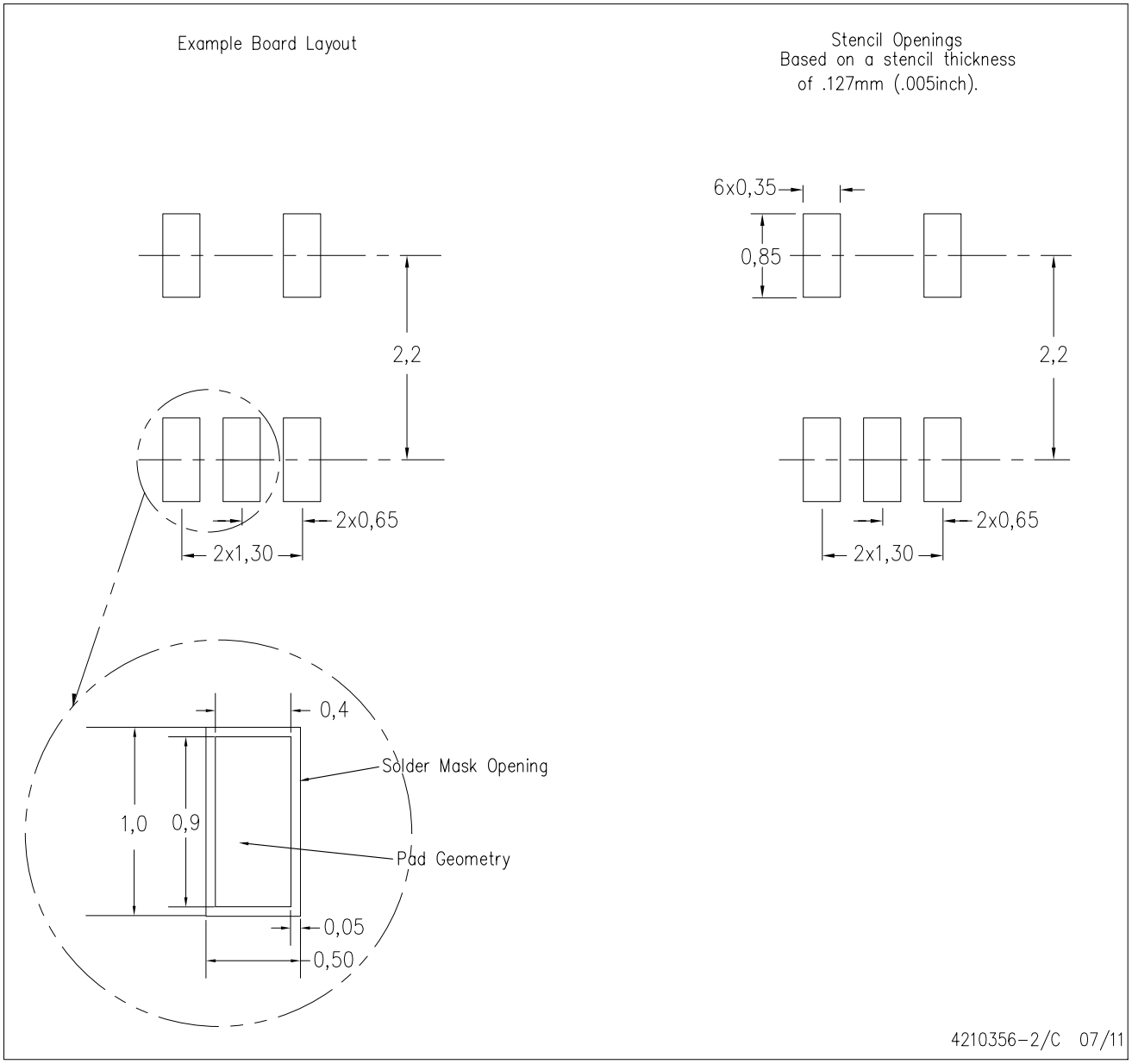
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



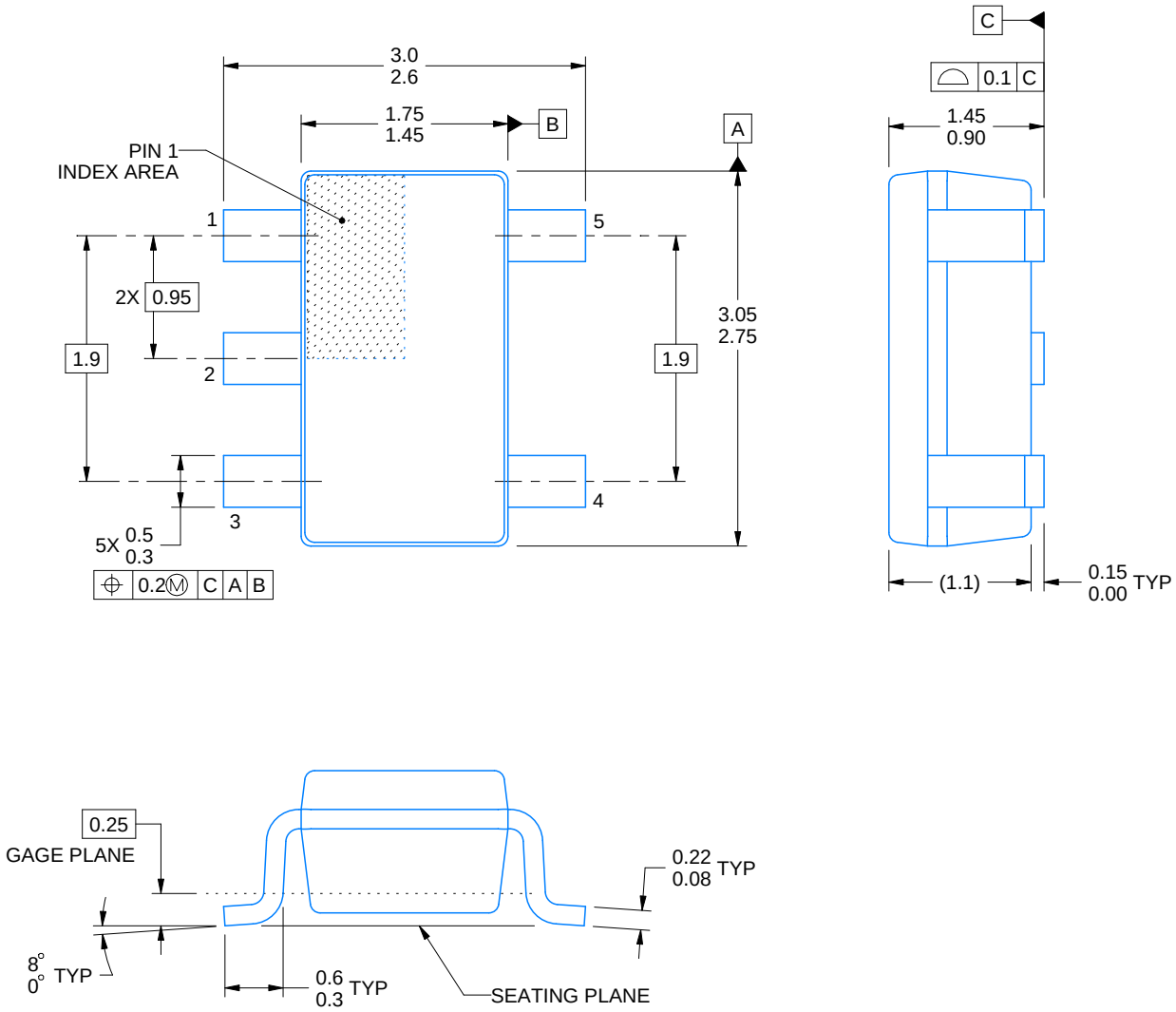
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

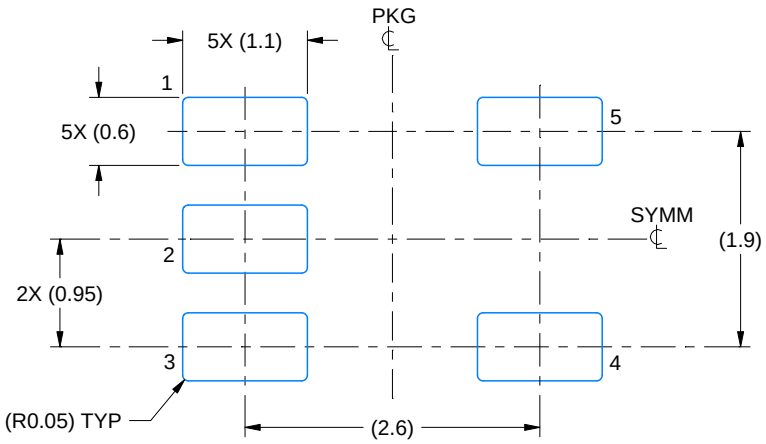
SMALL OUTLINE TRANSISTOR



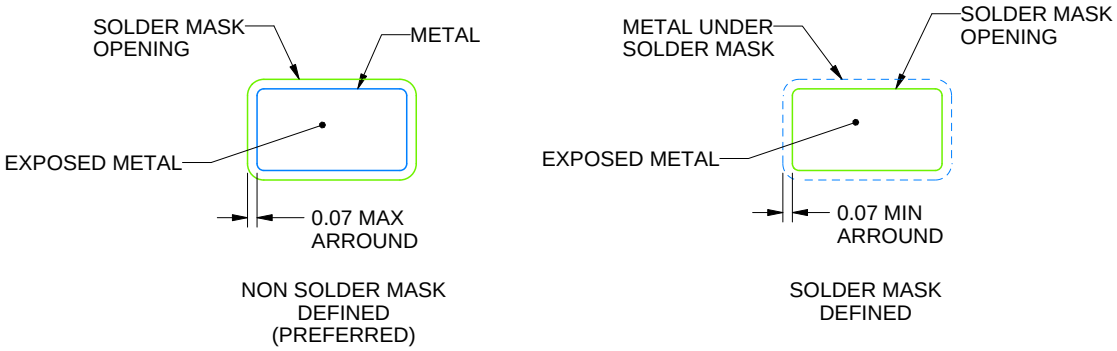
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

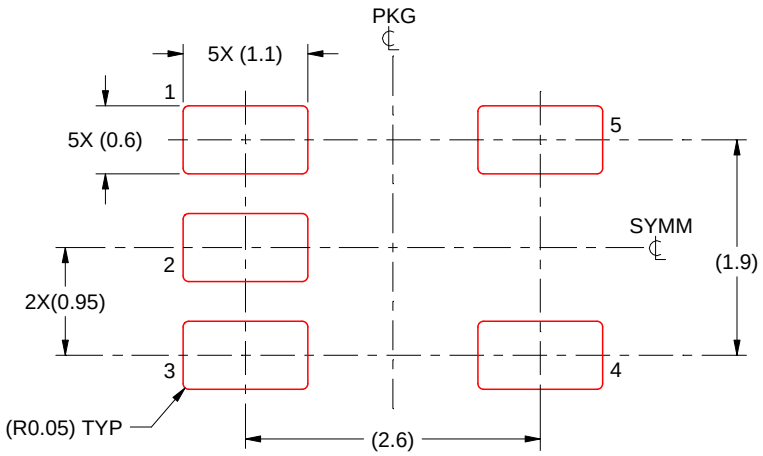


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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