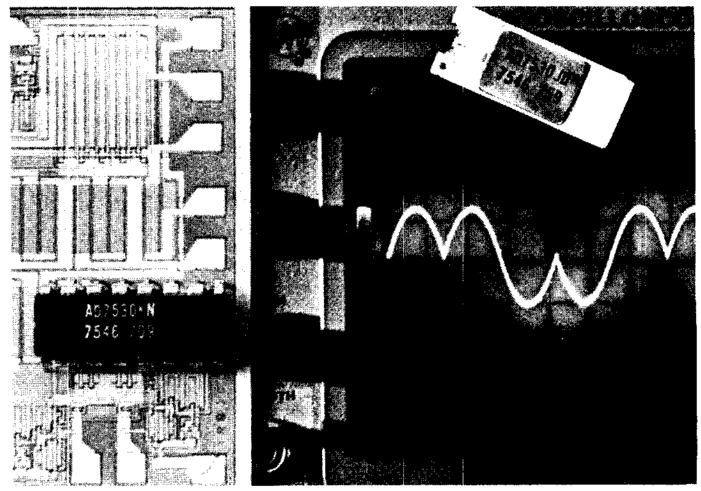
ANALOG DEVICES

CMOS 10 & 12 Bit Monolithic Multiplying D/A Converters

AD7530, AD7531

FEATURES
AD7530: 10-Bit Resolution
AD7531: 12-Bit Resolution
8, 9 and 10 Bit Linearity
DTL/TTL/CMOS Compatible
Nonlinearity Tempco: 2ppm of FSR/°C
Low Power Dissipation: 20mW
Current Settling Time: 500ns
Feedthrough Error: 10mV p-p @ 50kHz
Low Cost



GENERAL DESCRIPTION

The AD7530 (AD7531) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The device uses advanced CMOS and thin film technologies providing up to 10-bit accuracy with DTL/TTL/CMOS compatibility.

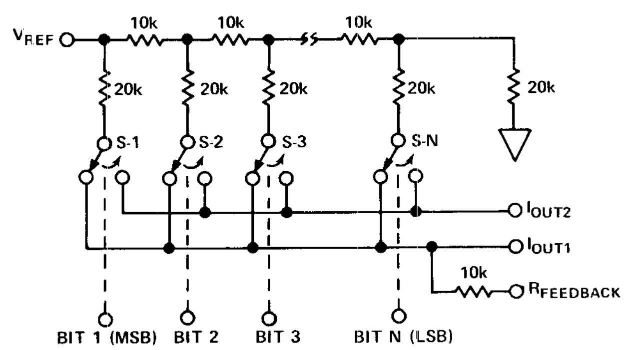
The AD7530 (AD7531) operates from a +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

ORDERING INFORMATION

Nonlinearity	Temperature Range 0 to +70°C	Temperature Range −25°C to +85°C
0.2% (8-Bit)	AD7530JN	AD7530JD
	AD7531JN	AD7531JD
0.1% (9-Bit)	AD7530KN	AD7530KD
	AD7531KN	AD7531KD
0.05% (10-Bit)	AD7530LN	AD7530LD
	AD7531LN	AD7531LD

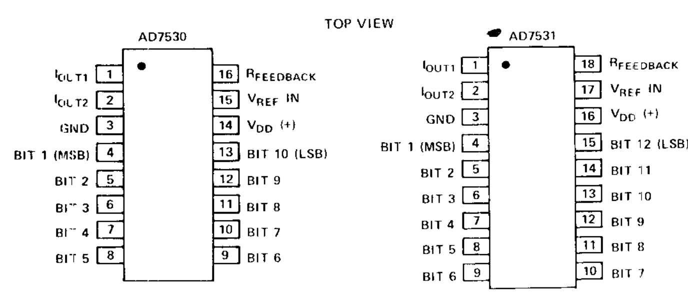
FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7530: N = 10
AD7531: N = 12
(Switches shown in "High" state)

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER		AD7530	AD7531	TEST CONDITIONS
DC ACCURACY (Note 1)				
Resolution		10 Bits	12 Bits	
Nonlinearity	AD7530J	0.2% of FSR max (8 Bit)	*	
	AD7530K	0.1% of FSR max (9 Bit)	*	
	AD7530L	0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco		2ppm of FSR/°C max	*	$-10V < V_{REF} < +10V$
Gain Error		0.3% of FSR typ	*	
Gain Error Tempco		10ppm of FSR/°C max	*	
Output Leakage Current (Either Output)		300nA max	*	Over specified temperature range.
Power Supply Rejection		50ppm of FSR/% typ	*	
AC ACCURACY				To 0.05%
Output Current Settling Time		500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error		10mV p-p max	*	V_{REF} = 20V p-p, 50kHz. All digital inputs low
REFERENCE INPUT		±10V	*	
Input Range		±1mA	*	
Input Resistance		10kΩ typ	*	
ANALOG OUTPUT				
Output Current Range (Both Outputs)		±1mA	*	
Output Capacitance	I_{OUT1}	120pF typ	*	All digital inputs high
	I_{OUT2}	37pF typ	*	
	I_{OUT1}	37pF typ	*	All digital input low
	I_{OUT2}	120pF typ	*	
Output Noise (Both Outputs)		Equivalent to 10kΩ Johnson noise typ	*	
DIGITAL INPUTS (Note 2)				
Low State Threshold		0.8V max	*	
High State Threshold		2.4V min	*	Over specified temperature range
Input Current (low to high state)		1μA typ	*	
Input Coding		Binary	*	See Tables 1 & 2
POWER REQUIREMENTS				
Power Supply Voltage Range		+5V to +15V	*	
I_{DD}		5nA typ	*	All digital inputs at GND
		2mA max	*	All digital inputs high or low
Total Dissipation		20mW typ	*	

NOTES:
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

*Same specifications as for AD7530.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to Gnd)	+17V
V_{REF} (to Gnd)	±25V
Digital Input Voltage Range	V_{DD} to Gnd
Voltage at Pin 1, Pin 2	−100mV to V_{DD}
Power Dissipation (package) up to +75°C	450mW
Operating Temperature JN, KN, LN Versions	0 to +75°C
JD, KD, LD Versions	−25°C to +85°C
Storage Temperature	−65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 1 shows the circuit connections required for unipolar operation. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1.

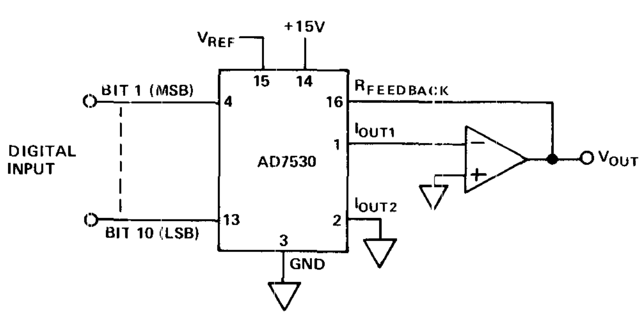


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = $2^{-10}\ V_{REF}$

Table 1. Code Table – Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 2 illustrates the AD7530 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})\ (10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal.

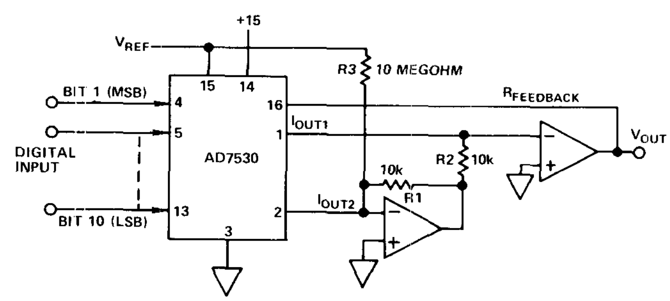


Figure 2. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = $2^{-9}\ V_{REF}$

Table 2. Code Table – Bipolar (Offset Binary) Operation

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DACs operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

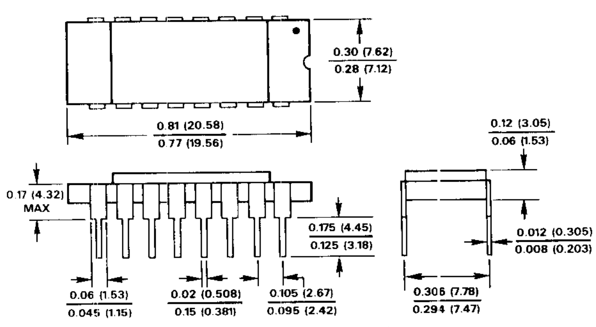
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

OUTLINE DIMENSIONS

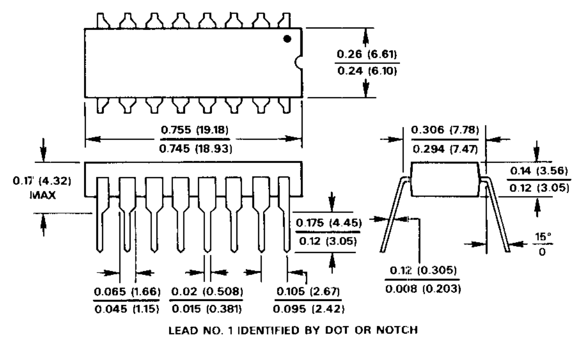
Dimensions shown in inches and (mm).

AD7530

16 PIN CERAMIC DIP

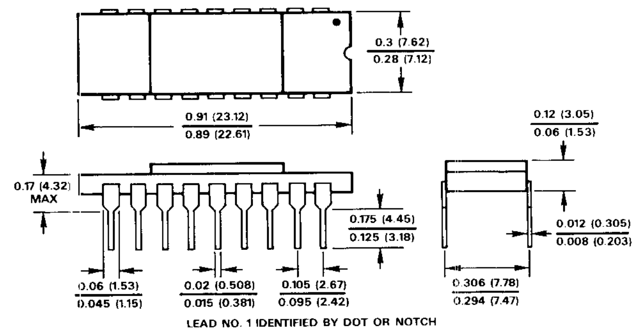


16 PIN PLASTIC DIP



AD7531

18 PIN CERAMIC DIP



18 PIN PLASTIC DIP