

# SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

SCDS031I – MAY 1996 – REVISED OCTOBER 2000

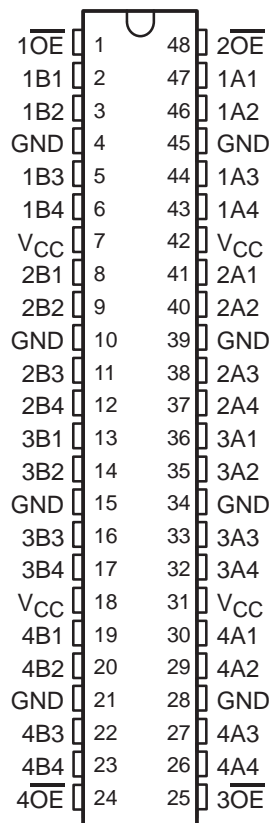
- Members of Texas Instruments' Widebus™ Family
- Standard '16244-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

## description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the switch is on, and data can flow from port A to port B, or vice versa. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

## SN54CBT16244 . . . WD PACKAGE SN74CBT16244 . . . DGG, DGV, OR DL PACKAGE (TOP VIEW)



## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16244DL	CBT16244
		Tape and reel	SN74CBT16244DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16244DGGR	CBT16244
	TVSOP – DGV	Tape and reel	SN74CBT16244DGVR	CY244
–55°C to 125°C	CFP – WD	Tube	SNJ54CBT16244WD	SNJ54CBT16244WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each 4-bit bus switch)

INPUT $\overline{OE}$	OUTPUTS A, B
L	A port = B port
H	Disconnect



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## SCDS031I – MAY 1996 – REVISED OCTOBER 2000

Supply voltage range, $V_{CC}$	−0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ )	−50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, $T_{stg}$	−65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

		SN54CBT16244		SN74CBT16244		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4	5.5	4	5.5	V
V <sub>IH</sub>	High-level control input voltage	2		2		V
V <sub>IL</sub>	Low-level control input voltage		0.8		0.8	V
T <sub>A</sub>	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54CBT16244		SN74CBT16244		UNIT
				MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA		−1.2		−1.2		V
I <sub>I</sub>		V <sub>CC</sub> = 0	V <sub>I</sub> = 5.5 V	10		10		μA
		V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V or GND	±1		±1		
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0,		3.2		3		μA
ΔI <sub>CC</sub> ‡	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		2.5		2.5		mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0		2.5		2.5		pF
C <sub>io</sub> (OFF)		V <sub>O</sub> = 3 V or 0, $\overline{\text{OE}}$ = V <sub>CC</sub>		4.5		4.5		pF
r <sub>on</sub> §		V <sub>CC</sub> = 4 V, V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA		20		20		Ω
		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0, I <sub>I</sub> = 64 mA	5	10	5	7	
			V <sub>I</sub> = 0, I <sub>I</sub> = 30 mA	5	10	5	7	
			V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA	8	14	8	12	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16244				SN74CBT16244				UNIT
			V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>¶</sup>	A or B	B or A			0.8*		0.35		0.25	ns	
t <sub>en</sub>	$\overline{OE}$	A or B		10.3	1	9.2		5.5	1	5.1	ns
t <sub>dis</sub>	$\overline{OE}$	A or B		9.7	1	8.2		5.2	1	5.4	ns

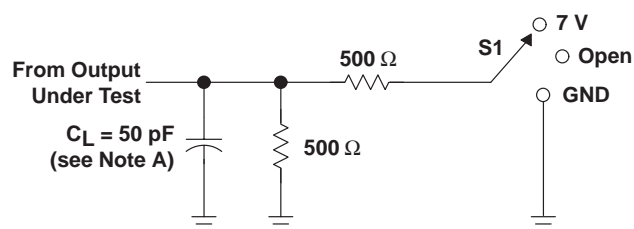
\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

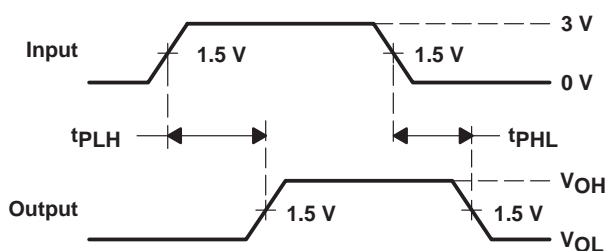
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SCDS031I – MAY 1996 – REVISED OCTOBER 2000

## PARAMETER MEASUREMENT INFORMATION

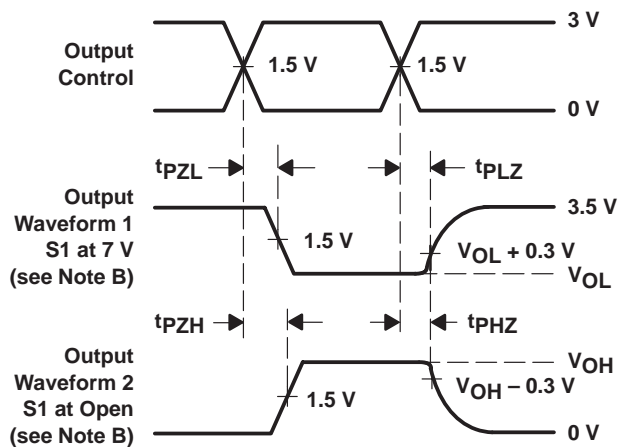


LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9855301QXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC
74CBT16244DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBT16244DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT16244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54CBT16244WD	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

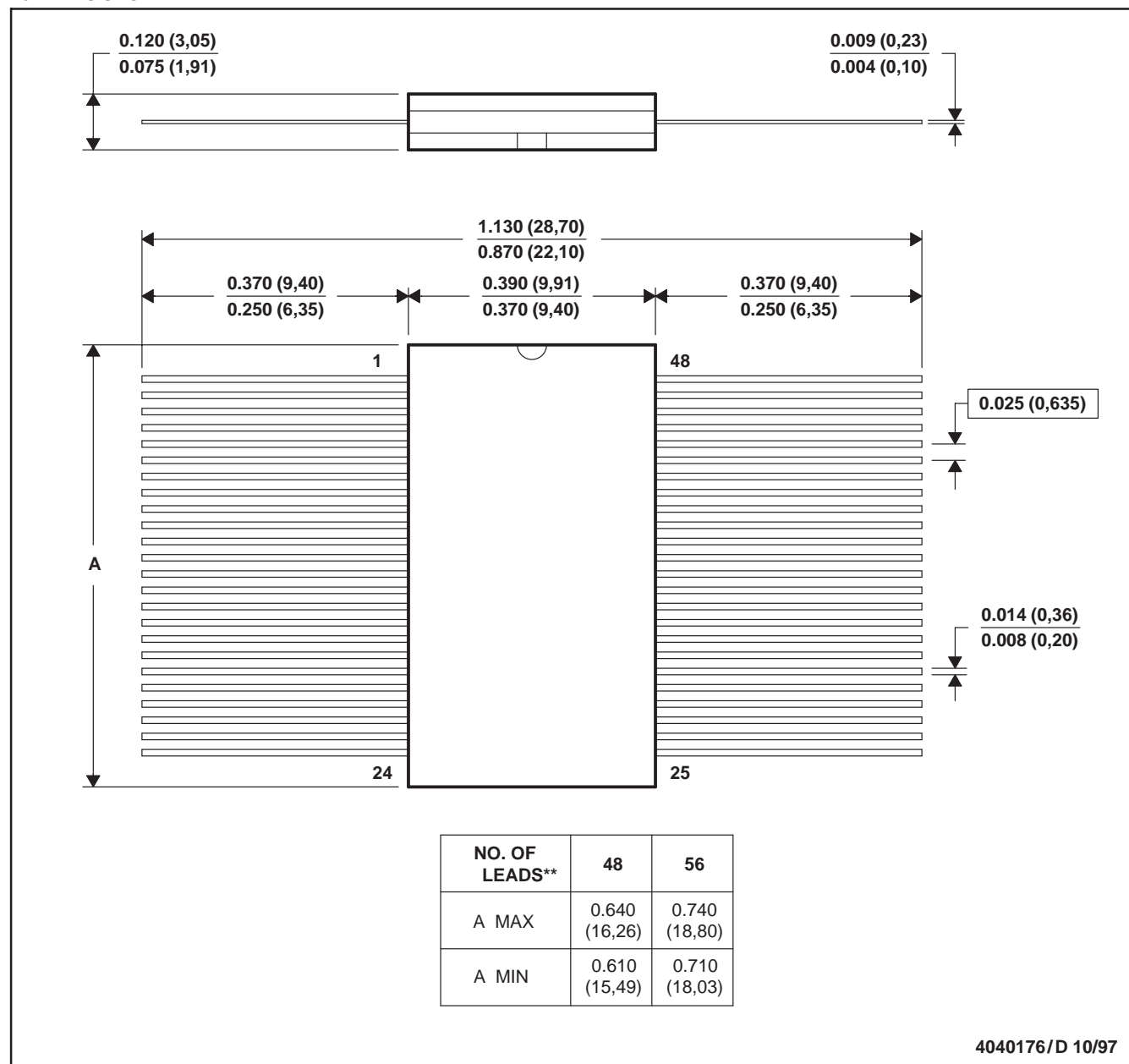
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## WD (R-GDFP-F\*\*)

## CERAMIC DUAL FLATPACK

48 LEADS SHOWN

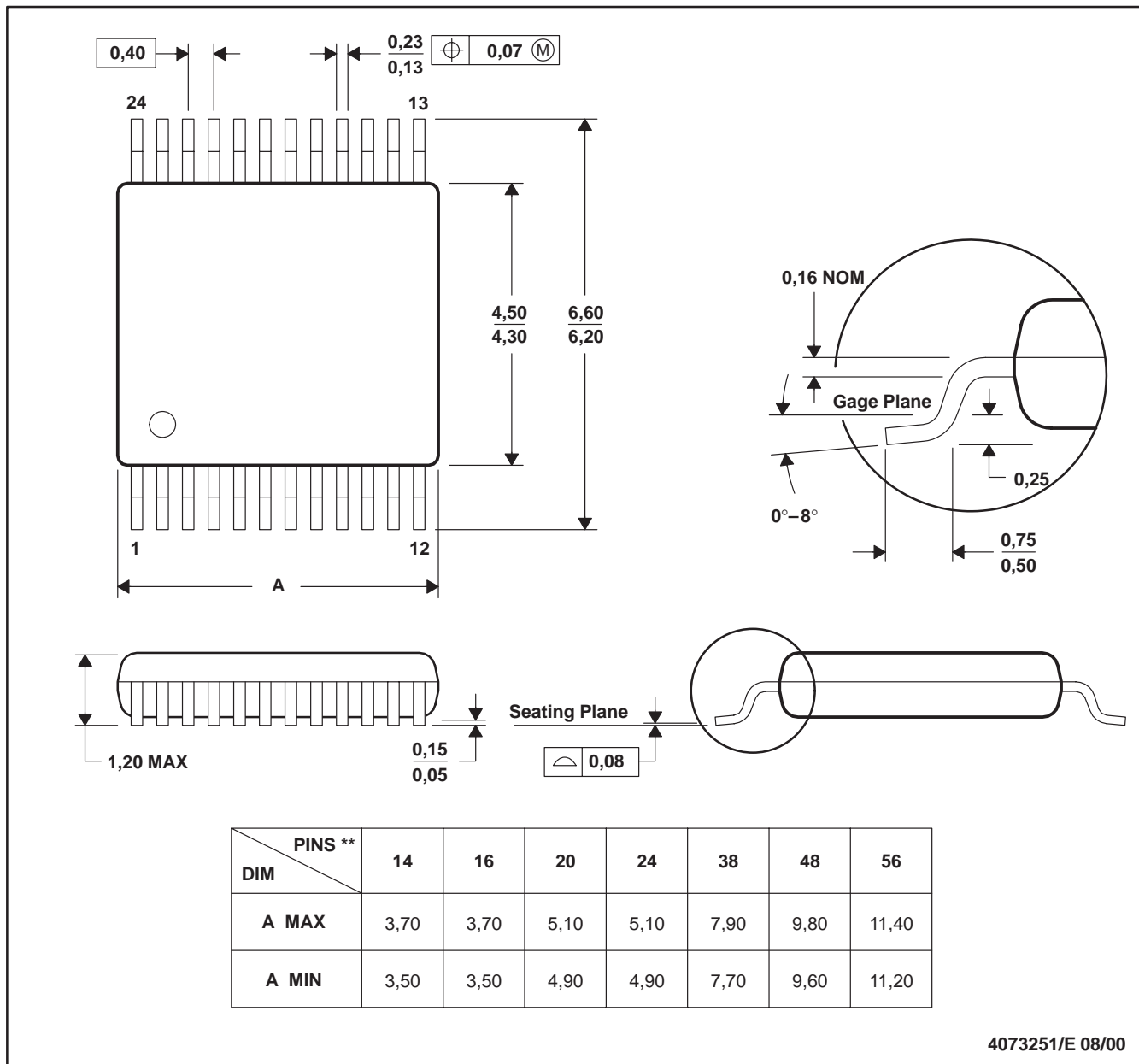


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118



## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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