

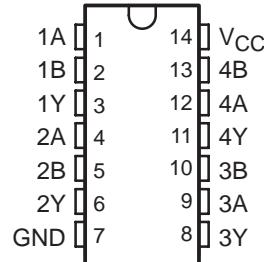
- Wide Operating Voltage Range of 2 V to 6 V
- Operation From Very Slow Input Transitions
- Same Pinouts as 'HC32
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Temperature-Compensated Threshold Levels
- High Noise Immunity

description/ordering information

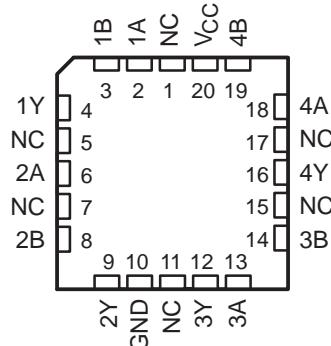
In these devices, each circuit functions as a quadruple OR gate. They perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = A + B$ in positive logic. However, because of the Schmitt action, the inputs have different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

SN54HC7032 . . . J OR W PACKAGE
SN74HC7032 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54HC7032 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	PDIP – N	Tube of 25	SN74HC7032N
			Tube of 50	SN74HC7032D
			Reel of 2500	SN74HC7032DR
			Reel of 250	SN74HC7032DT
	SOP – NS	Reel of 2000	SN74HC7032NSR	HC7032
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC7032J	SNJ54HC7032J
	CFP – W	Tube of 150	SNJ54HC7032W	SNJ54HC7032W
	LCCC – FK	Tube of 55	SNJ54HC7032FK	SNJ54HC7032FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

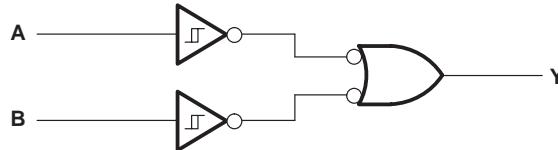
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

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SN54HC7032, SN74HC7032 QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

SCLS036E – MARCH 1984 – REVISED NOVEMBER 2004

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 3)

		SN54HC7032			SN74HC7032			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _I	Input voltage	0	V _{CC}	V _{CC}	0	V _{CC}	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V _{CC}	0	V _{CC}	V _{CC}	V
T _A	Operating free-air temperature	-55	125	125	-40	85	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54HC7032, SN74HC7032
QUADRUPLE POSITIVE-OR GATES
WITH SCHMITT-TRIGGER INPUTS
SCLS036E – MARCH 1984 – REVISED NOVEMBER 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC7032	SN74HC7032	UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+}		2 V	0.7	1.2	1.5	0.7	1.5	V
		4.5 V	1.55	2.5	3.15	1.55	3.15	
		6 V	2.1	3.3	4.2	2.1	4.2	
V _{T-}		2 V	0.3	0.6	1	0.3	1	V
		4.5 V	0.9	1.6	2.45	0.9	2.45	
		6 V	1.2	2	3.2	1.2	3.2	
V _{T+} – V _{T-}		2 V	0.2	0.6	1.2	0.2	1.2	V
		4.5 V	0.4	0.9	2.1	0.4	2.1	
		6 V	0.5	1.3	2.5	0.5	2.5	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 μA	2 V	1.9	1.998	1.9	1.9	V
			4.5 V	4.4	4.499	4.4	4.4	
			6 V	5.9	5.999	5.9	5.9	
		I _{OH} = –4 mA	4.5 V	3.98	4.3	3.7	3.84	
		I _{OH} = –5.2 mA	6 V	5.48	5.8	5.2	5.34	
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.002	0.1	0.1	0.1	V
			4.5 V	0.001	0.1	0.1	0.1	
			6 V	0.001	0.1	0.1	0.1	
		I _{OL} = 4 mA	4.5 V	0.17	0.26	0.4	0.33	
		I _{OL} = 5.2 mA	6 V	0.15	0.26	0.4	0.33	
I _I	V _I = V _{CC} or 0	6 V	±0.1	±100	±1000	±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V		2	40	20	μA	
C _i		2 V to 6 V	3	10	10	10	pF	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC7032	SN74HC7032	UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	2 V	60	130	195		163	ns
			4.5 V	18	26	39		33	
			6 V	14	22	33		28	
t _t		Any	2 V	28	75	110		95	ns
			4.5 V	8	15	22		19	
			6 V	6	13	19		16	

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	No load	20	pF

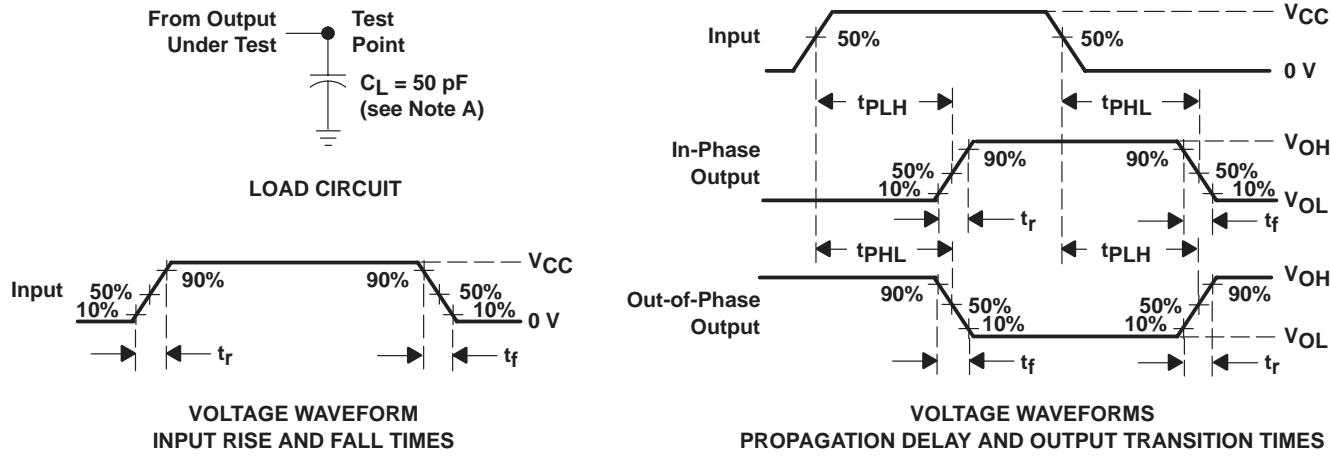
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SN54HC7032, SN74HC7032 QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time, with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74HC7032D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC7032DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC7032DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC7032DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC7032DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC7032DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC7032N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC7032NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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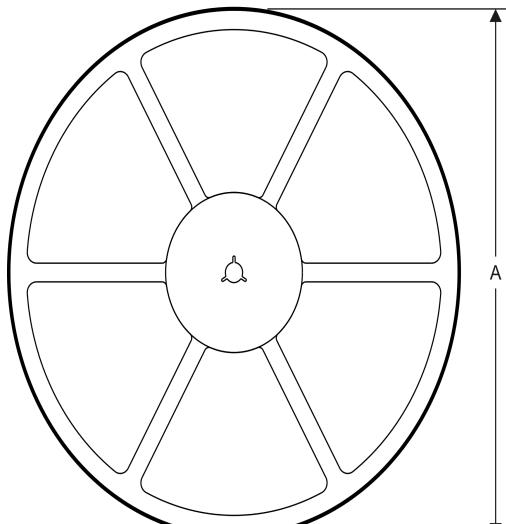
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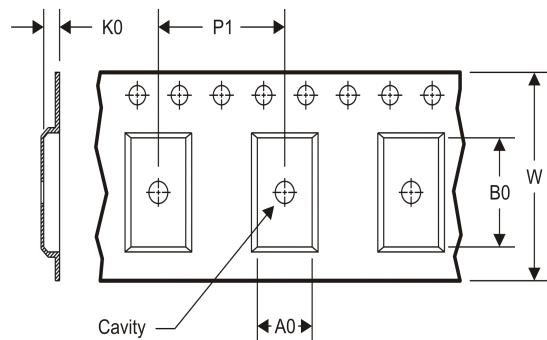
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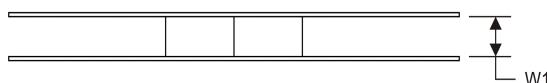
REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC7032DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

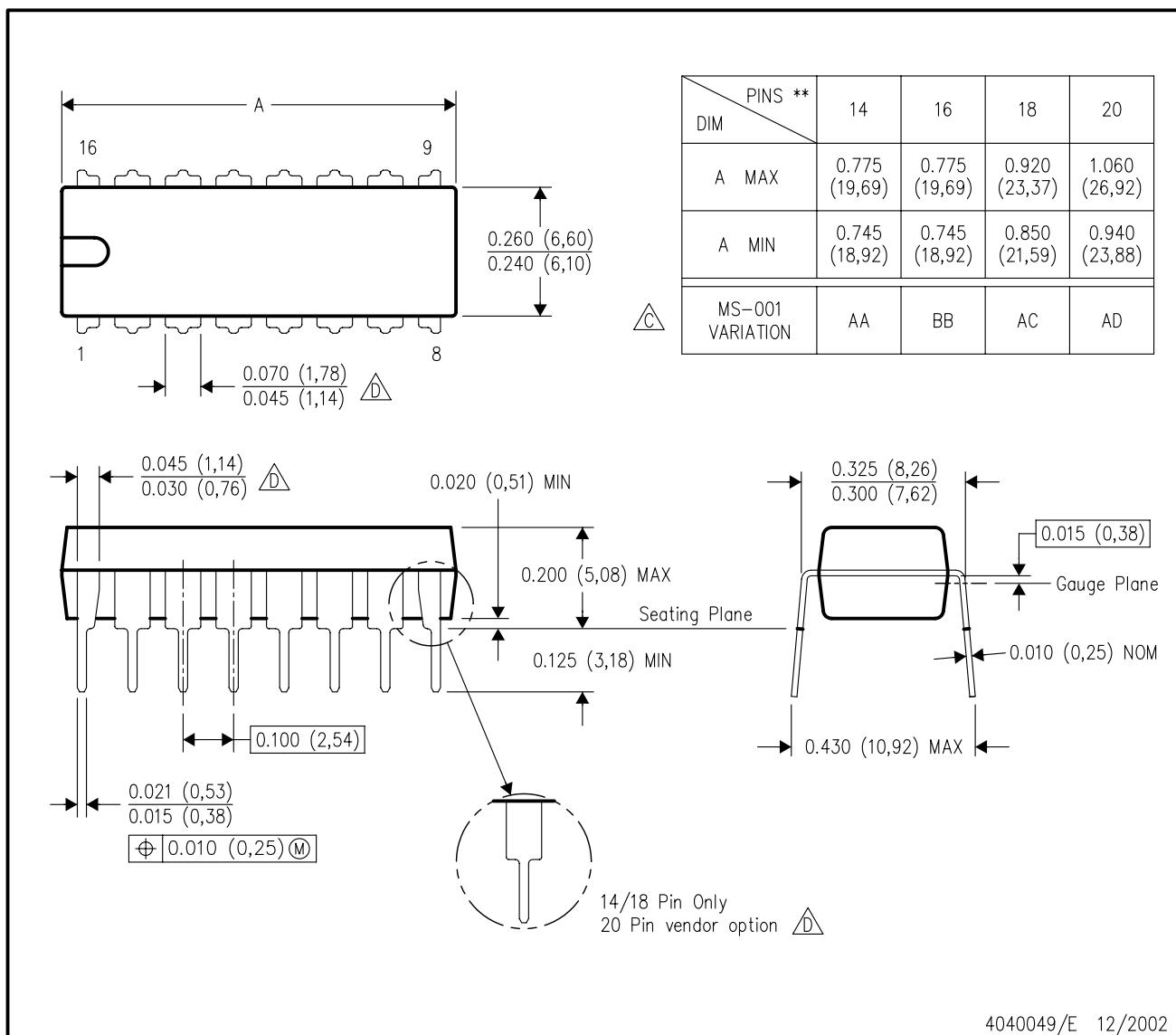
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC7032DT	SOIC	D	14	250	367.0	367.0	38.0

N (R-PDIP-T**)

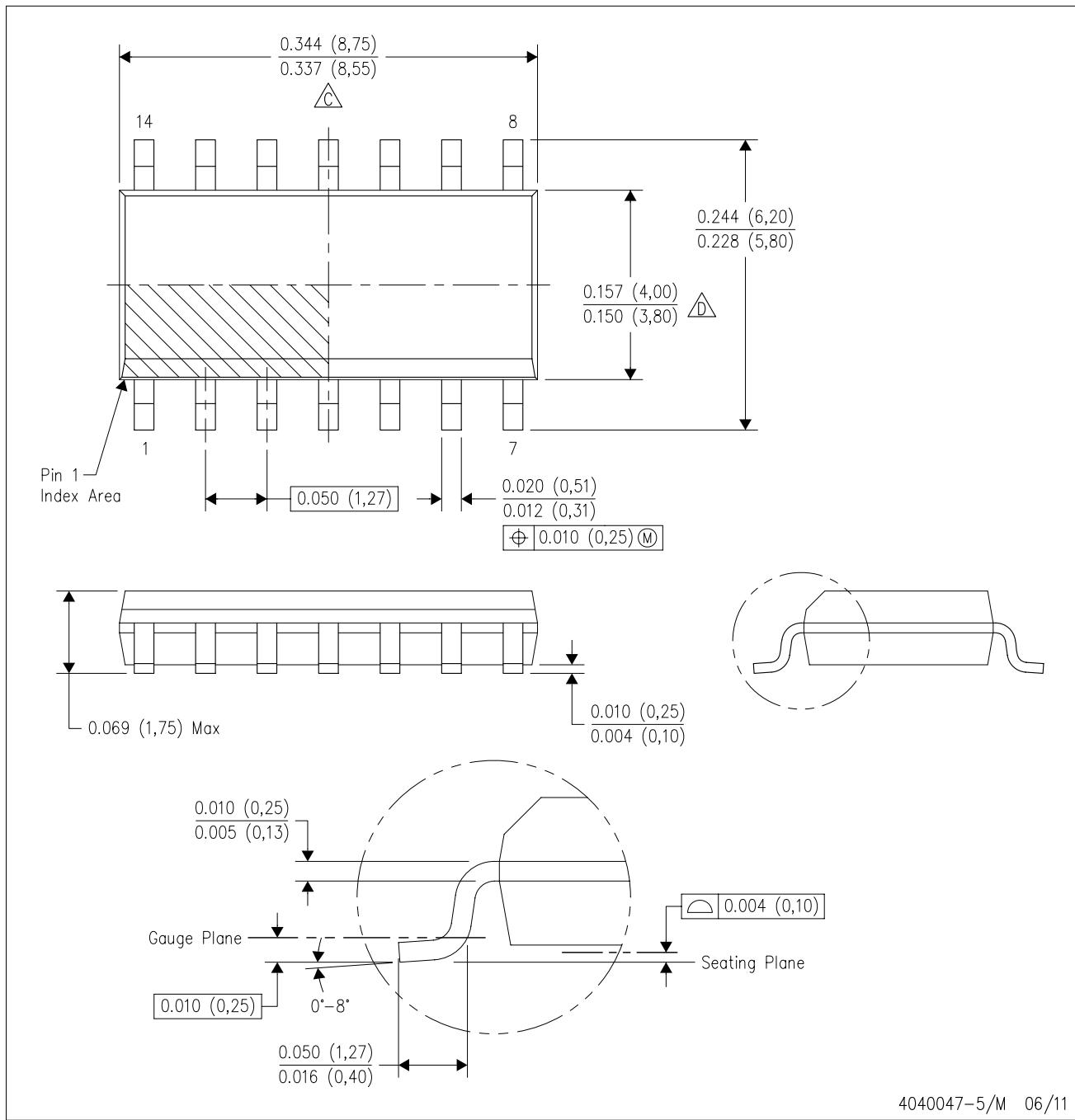
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

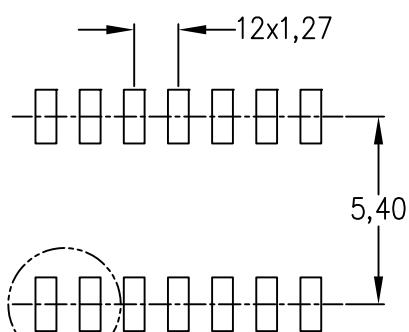
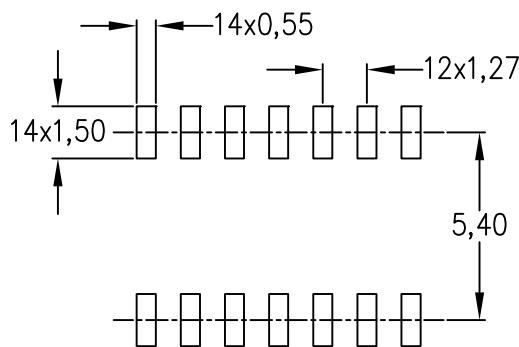
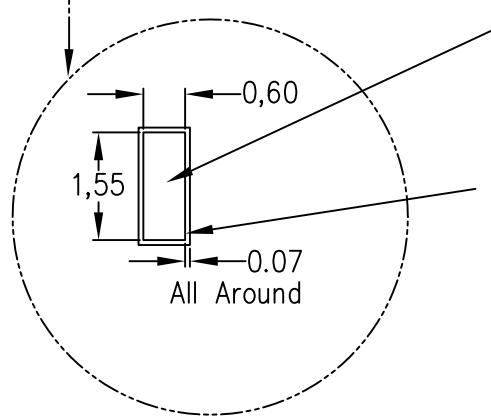
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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