National Semiconductor

MICROCIRCUIT DATA SHEET

MNLF198-X REV 3B0

Original Creation Date: 06/20/95
Last Update Date: 05/23/01
Last Major Revision Date: 02/01/01

MONOLITHIC SAMPLE AND HOLD

General Description

The LF198 is a monolithic sample-and-hold circuit which utilizes BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6us to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of 10[10] Ohms allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1uF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to ouput in the hold mode, even for input signals equal to the supply voltages.

Industry Part Number

LF198

NS Part Numbers

LF198H/883
LF198WG-QMLV
LF198WG/883

Prime Die

LF198

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Operates from ±5V to ±18V supplies.
- Less than 10 uS aquisition time.
- TTL, PMOS, CMOS compatible logic input.
- 0.5 mV typical hold step at Ch = 0.01 uF.
- Low input offset.
- 0.002% gain accuracy.
- Low output noise in hold mode.
- Input characteristics do not change during hold mode.
- High supply rejection ratio in sample or hold.
- Wide bandwidth.

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS, Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

CONTROLLING DOCUMENTS:

- LF198H/883 5962-8760801GA
- LF198WG-QMLV 5962-8760801VZA
- LF198WG/883 5962-8760801QZA

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage	±18V
Power Dissipation (Note 2)	
(Package Limitation)	500mW
Operating Ambient Temperature Range	-55 C ≤ Ta ≤ +125 C
Maximum Junction Temperature	150 C
Storage Temperature Range	-65 C to +150 C
Input Voltage	Equal to Supply Voltage
Logic to Logic Reference Differential Voltage (Note 3)	+7V, -30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec.
Lead Temperature	
(Soldering, 10 seconds)	260 C
Thermal Resistance	
ThetaJA	
Metal Can	
(Still Air @ 0.5W)	160 C/W
(500LF/Min Air flow @ 0.5W)	84 C/W
CERAMIC SOIC	
(Still Air @ 0.5W)	140 C/W
(500LF/Min Air flow @ 0.5W)	95 C/W
ThetaJC	
Metal Can	48 C/W
CERAMIC SOIC	20 C/W
Package Weight (Typical)	
Metal Can	TBD
CERAMIC SOIC	415mg
ESD Tolerance (Note 4)	500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 4: Human body model, 100pF discharged through 1.5k Ohms.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Rl = 10K, Vin = 0V, Chold = 0.01uF, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc+	Positive Supply Current	+Vcc = 15V, -Vcc = -15V				5.5	mA	1, 2
						6.5	mA	3
		+Vcc = 18V, -Vcc = -18V, Mode = "Sample"				5.5	mA	1, 2
						6.5	mA	3
		+Vcc = 18V, -Vcc = -18V, Mode = "Hold"				5.5	mA	1, 2
						6.5	mA	3
Icc-	Negative Supply Current	+Vcc = 15V, -Vcc = -15V			-5.5		mA	1, 2
					-6.5		mA	3
		+Vcc = 18V, -Vcc = -18V, Mode = "Sample"			-5.5		mA	1, 2
					-6.5		mA	3
		+Vcc = 18V, -Vcc = -18V, Mode = "Hold"			-5.5		mA	1, 2
					-6.5		mA	3
Vos	Input Offset Voltage	+Vcc = 3V, -Vcc = -7V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 15V, -Vcc = -15V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 3.5V, -Vcc = -26.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 18V, -Vcc = -18V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 3.5V, -Vcc = -32.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 26.5V, -Vcc = -3.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 32.5V, -Vcc = -3.5V, Logic = 2.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+Vcc = 7V, -Vcc = -3V			-3	3	mV	1
					-5	5	mV	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Rl = 10K, Vin = 0V, Chold = 0.01uF, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ib	Input Bias Current	+Vcc = 3V, -Vcc = -7V			-25	25	nA	1
					-75	75	nA	2, 3
		+Vcc = 15V, -Vcc = -15V			-25	25	nA	1
					-75	75	nA	2, 3
		+Vcc = 3.5V, -Vcc = -32.5V			-25	25	nA	1
					-75	75	nA	2, 3
		+Vcc = 32.5V, -Vcc = -3.5V			-25	25	nA	1
					-75	75	nA	2, 3
		+Vcc = 7V, -Vcc = -3V			-25	25	nA	1
					-75	75	nA	2, 3
Ileak(CAP)	Leakage Current into Hold Capacitor	+Vcc = 3V, -Vcc = -7V			-100	100	pA	1
		+Vcc = 3.5V, -Vcc = -32.5V			-100	100	pA	1
		+Vcc = 32.5V, -Vcc = -3.5V			-100	100	pA	1
		+Vcc = 7V, -Vcc = -3V			-100	100	pA	1
Vhs	Hold Step	+Vcc = 15V -Vcc = -15V			-2	2	mV	1
					-5.6	5.6	mV	2, 3
		+Vcc = 3.5V, -Vcc = -26.5V			-2.5	2.5	mV	1
					-5.6	5.6	mV	2, 3
		+Vcc = 26.5V, -Vcc = -3.5V			-2.5	2.5	mV	1
					-5.6	5.6	mV	2, 3
Ae	Gain Error	+Vcc = 7V, -Vcc = -3V				0.02	%	1
						0.06	%	2, 3
		+Vcc = 3.5V, -Vcc = -26.5V				0.005	%	1
						0.02	%	2, 3
		+Vcc = 32.5V, -Vcc = -3.5V				0.005	%	1
						0.06	%	2, 3
		+Vcc = 26.5V, -Vcc = -3.5V				0.005	%	1
						0.02	%	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Rl = 10K, Vin = 0V, Chold = 0.01uF, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Zi	Input Impedance	+Vcc = 8V, -Vcc = -28V			10		GOhm	1
					0.8		GOhm	2, 3
		+Vcc = 28V, -Vcc = -8V			10		GOhm	1
					0.8		GOhm	2, 3
Zo	Output Impedance	+Vcc = 18V, -Vcc = -18V				2	Ohm	1
						4	Ohm	2, 3
Icharge	Capacitor Charging Current	+Vcc = 8V, -Vcc = -28V			-25	-4.5	mA	1
					-25	-3	mA	2, 3
		+Vcc = 28V, -Vcc = -8V			4.5	25	mA	1
					3	25	mA	2, 3
Logic	Logic Pin Current	+Vcc = 18V, -Vcc = -18V, Mode = "Sample", Logic = 7V				10	uA	1, 2, 3
		+Vcc = 18V, -Vcc = -18V, Mode = "Hold", Logic = -30V				1	uA	1
						0.5	uA	2, 3
Vos	Input Offset Voltage	+Vcc = 15V, -Vcc = -15V, IDRIVE = +1mA			-3.5	3.5	mV	1
					-6	6	mV	2, 3
Delta Vos	Input Offset Voltage	+Vcc = 15V, -Vcc = -15V, IDRIVE = +1mA to -1mA			-1.1	1.1	mV	1
					-2	2	mV	2, 3
Ios+	Output Short Circuit Current	+Vcc = 18V, -Vcc = -18V			7	20	mA	1
Ios-	Output Short Circuit Current	+Vcc = 18V, -Vcc = -18V			-25	7	mA	1
Ilogicref	Logic Reference Pin Current	+Vcc = 18V, -Vcc = -18V, Mode = "Sample", Logic = 7V			-1	1	uA	1
					-0.5	5	uA	2, 3
		+Vcc = 18V, -Vcc = -18V, Mode = "Hold", Logic = -30V				10	uA	1, 2, 3
PSRR	Power Supply Rejection Ratio	+Vcc = 10V, -Vcc = -15V			80		dB	1
					74		dB	2, 3
		+Vcc = 15V, -Vcc = -10V			80		dB	1
					74		dB	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Rl = 10K, Vin = 0V, Chold = 0.01uF, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
FTRR	Feedthrough Rejection Ratio	+Vcc = 3.5V, -Vcc = -32.5V			86		dB	1
					74		dB	2, 3
		+Vcc = 32.5V, -Vcc = -3.5V			86		dB	1
					74		dB	2, 3
Vth	Differential Logic Level		1		0.8	2.4	V	1
Vos(2nd Stg)	2nd Stage Vos	+Vcc = 3.5V, -Vcc = -32.5V			-35	+35	mV	1
					-50	+50	mV	2, 3
		+Vcc = 3V, -Vcc = -7V			-35	+35	mV	1
					-50	+50	mV	2, 3
		+Vcc = 32.5V, -Vcc = -3.5V			-35	+35	mV	1
					-50	+50	mV	2, 3
		+Vcc = 7V, -Vcc = -3V			-35	+35	mV	1
					-50	+50	mV	2, 3

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±15V, Rl = 10K, Vin = 0V, Chold = 0.01uF, Logic Reference Pin = 0V, Logic Pin = 4V.

Taq	Acquisition Time	Delta Vout = 10V, Chold = 1000pF				6	uS	4
		Delta Vout = 10V, Chold = 0.01uF				25	uS	4

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Rl = 10K, Vin = 0V, Chold = 0.01uF, Logic Reference Pin = 0V, Logic Pin = 4V. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Vos	Input Offset Voltage	+Vcc = 15V, -Vcc = -15V			-0.5	0.5	mV	1
Ib	Input Bias Current	+Vcc = 15V, -Vcc = -15V			-2.5	2.5	nA	1

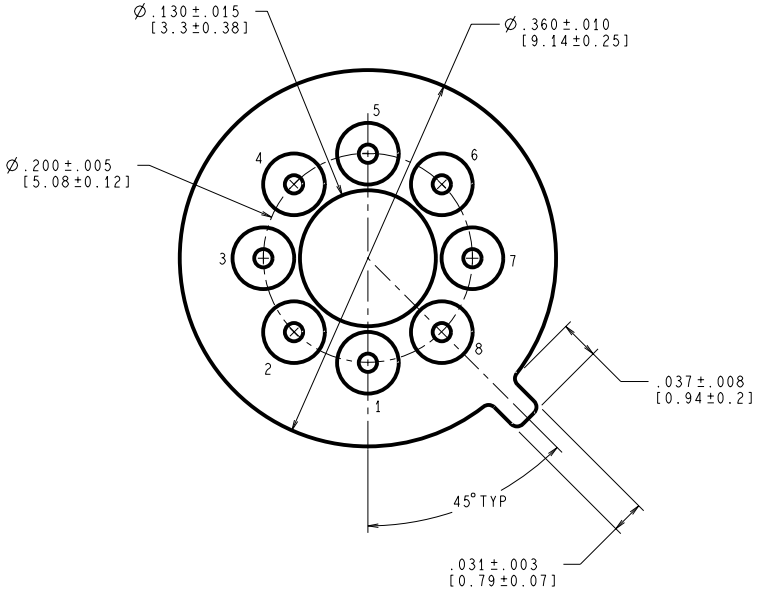
Note 1: Parameter tested go-no-go only.

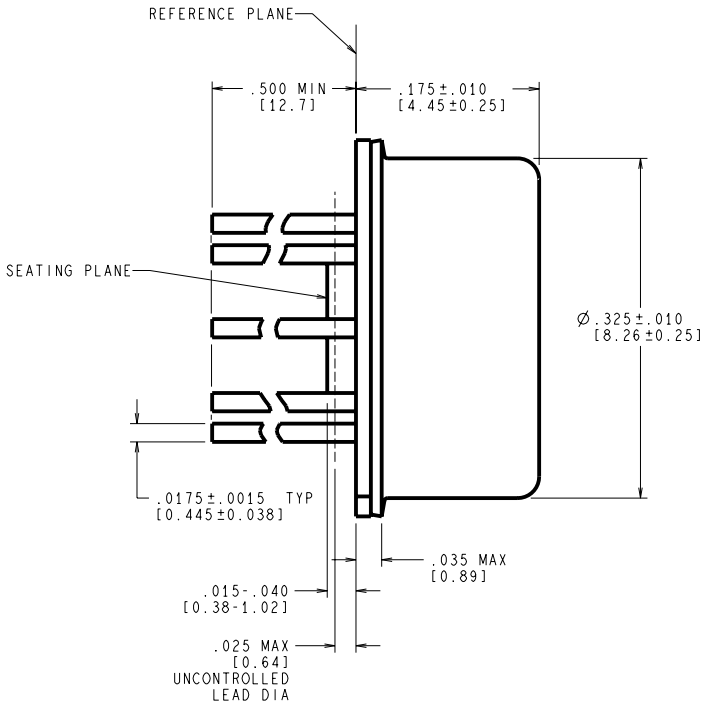
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05022HRC1	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
06068HRA2	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
06069HRA2	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
06398HRA1	CERAMIC SOIC (WG), 14LD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
P000194A	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (PINOUT)
P000476A	CERAMIC SOIC (WG), 14LD (PIN OUT)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

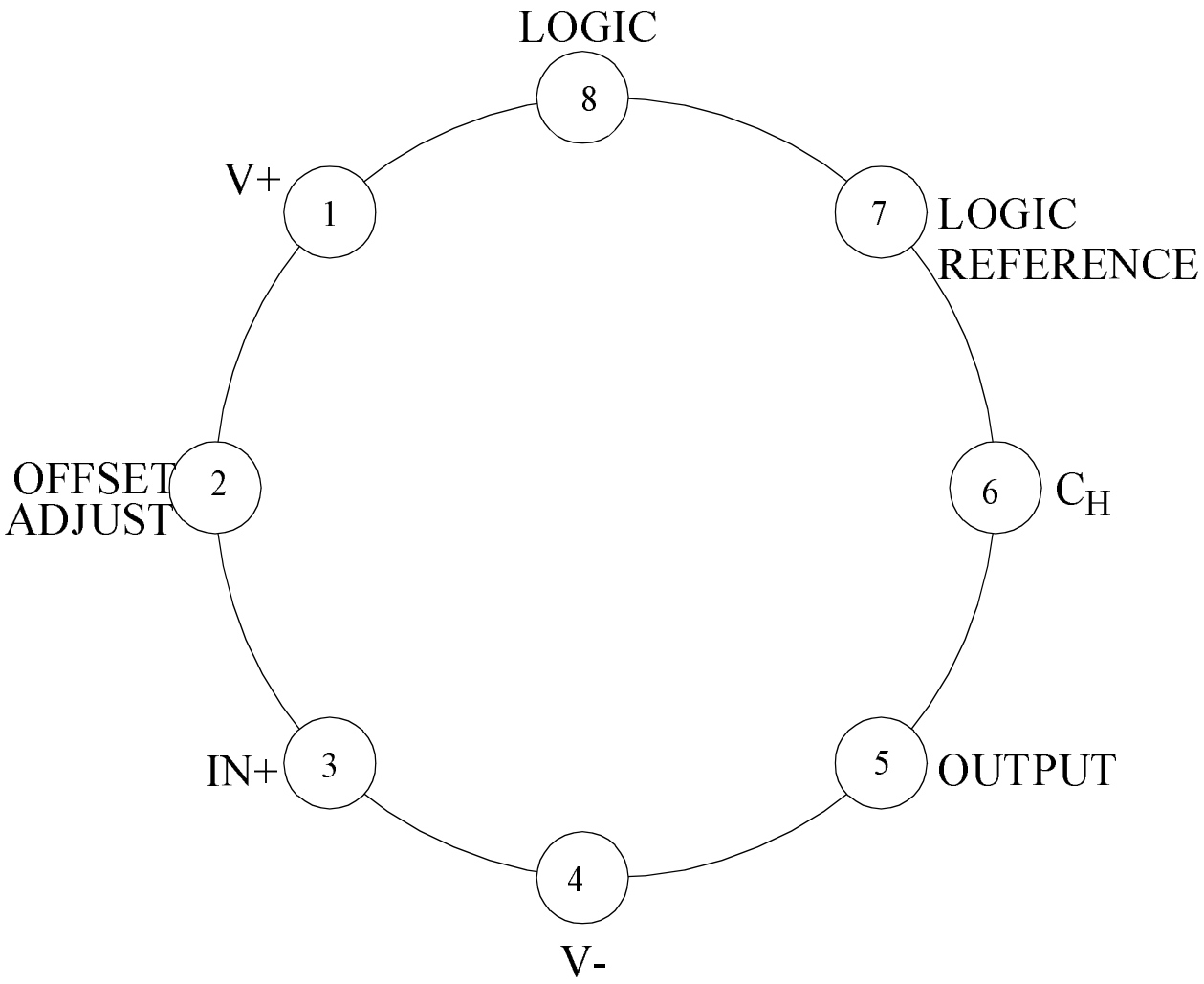
PROJECTION — INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

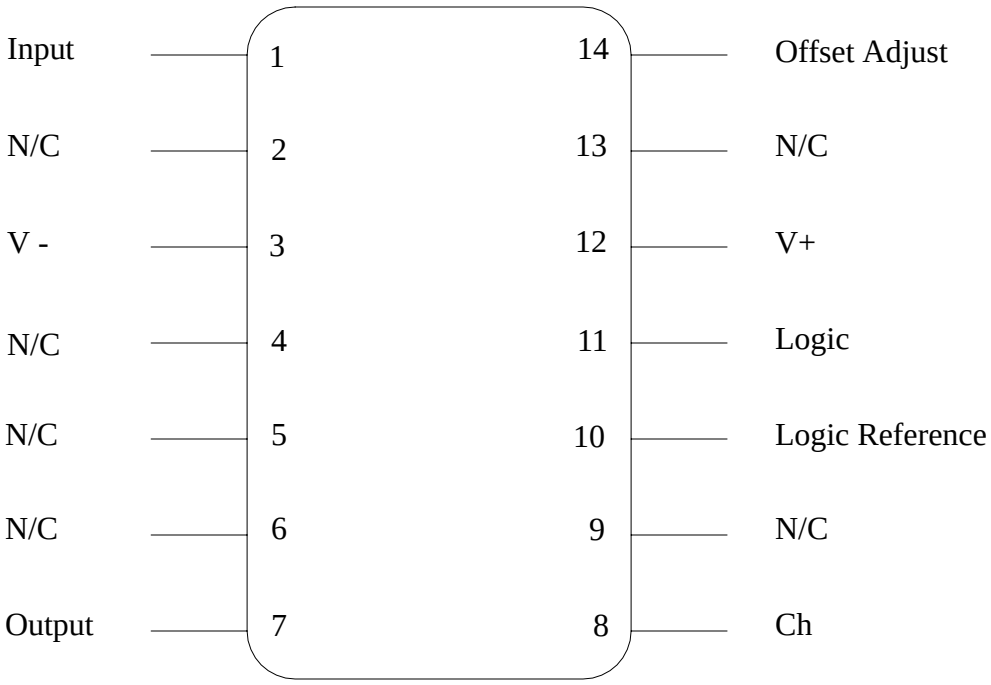
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1



LF198H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000194A

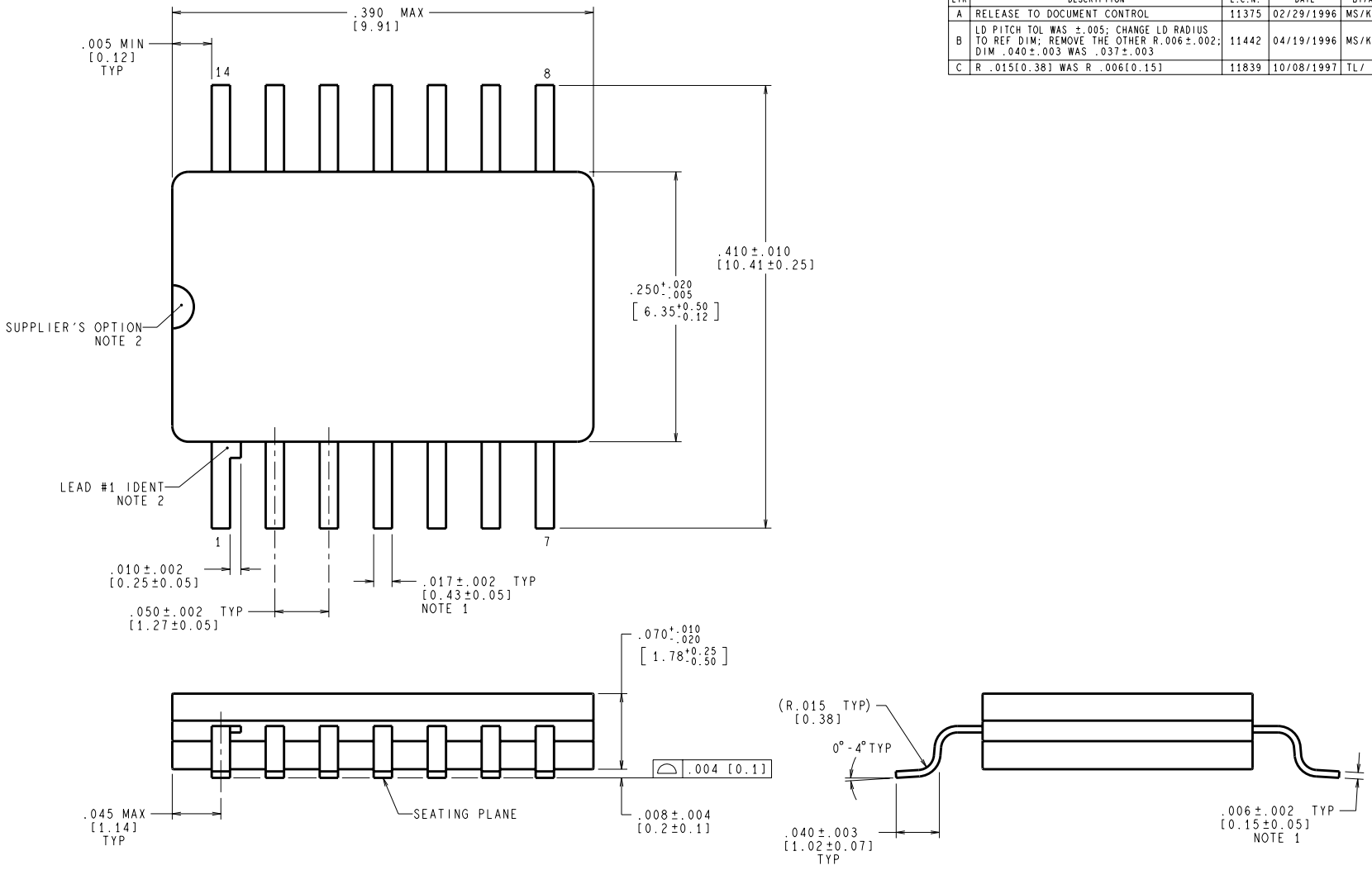
National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LF198WG
14 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000476A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11442	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11839	10/08/1997	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

PROJECTION
INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD, GULL WING

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG14A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1AL	M0002942	11/17/00	Rose Malone	Updated MDS: MNLF198-X Rev. 0BL to MNLF198-X Rev. 1AL. TYPO: Vhs, Condition +Vcc = 25.5V, -Vcc = -3.5V Changed min. from -5.5 to -5.6, typo made at the time of RETS to MDS conversion.
2A0	M0003770	02/06/01	Rose Malone	Update MDS: MNLF198-X, Rev. 1AL to MNLF198-X, Rev. 2A0. Fully Released MDS - ADDED WG pkg to Main Table and SMD numbers to Features Section, added ESD parameter, Thermal Resistance and Package Weight section to Absolute Maximum Ratings Section, Drift Values to Electrical Section, WG graphics to Graphics Section.
3A0	M0003784	05/23/01	Rose Malone	Update MDS: MNLF198-X, Rev. 2A0 to MNLF198-X, Rev. 3A0. Changed Electrical Section, DC Parameter Vos Condition from +Vcc = 26.5V, -Vcc = 3.5 to +Vcc = 26.5V, -Vcc = -3.5 and AC Parameter Taq Condition from Chold = 0.01uF to Delta Vout = 10V, Chold = 0.01uF
3B0	M0003803	05/23/01	Rose Malone	UPDATE MDS: MNLF198-X, Rev. 3A0 to MNLF198-X, Rev. 3B0. Updated Absolute Maximum Ratings Section, Thermal Resistance and Package Weight for WG Pkg.