

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For tape-and-reel order entry, the DGG package is abbreviated to GR.

## DESCRIPTION

This 10-bit flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH162820 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162820 is characterized for operation from -40°C to 85°C.

**DGG OR DL PACKAGE  
(TOP VIEW)**

1 $\overline{OE}$	1	56	CLK
1Q1	2	55	D1
1Q2	3	54	NC
GND	4	53	GND
2Q1	5	52	D2
2Q2	6	51	NC
$V_{CC}$	7	50	$V_{CC}$
3Q1	8	49	D3
3Q2	9	48	NC
4Q1	10	47	D4
GND	11	46	GND
4Q2	12	45	NC
5Q1	13	44	D5
5Q2	14	43	NC
6Q1	15	42	D6
6Q2	16	41	NC
7Q1	17	40	D7
GND	18	39	GND
7Q2	19	38	NC
8Q1	20	37	D8
8Q2	21	36	NC
$V_{CC}$	22	35	$V_{CC}$
9Q1	23	34	D9
9Q2	24	33	NC
GND	25	32	GND
10Q1	26	31	D10
10Q2	27	30	NC
2 $\overline{OE}$	28	29	NC

NC – No internal connection



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# SN74ALVCH162820

## 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

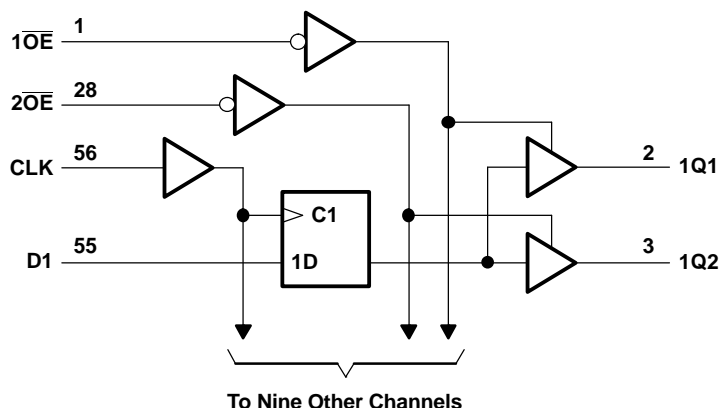
SCES012H–JULY 1995–REVISED SEPTEMBER 2004

**FUNCTION TABLE**  
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{OEn}^{(1)}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

(1)  $n = 1, 2$

**LOGIC DIAGRAM (POSITIVE LOGIC)**



### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range		-0.5	4.6	V	
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		-0.5	4.6	V	
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>		-0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0			-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0			-50	mA
I <sub>O</sub>	Continuous output current				±50	mA
Continuous current through each V <sub>CC</sub> or GND					±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package			64	°C/W
		DL package			56	
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-2		mA
		V <sub>CC</sub> = 2.3 V	-6		
		V <sub>CC</sub> = 2.7 V	-8		
		V <sub>CC</sub> = 3 V	-12		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	2		mA
		V <sub>CC</sub> = 2.3 V	6		
		V <sub>CC</sub> = 2.7 V	8		
		V <sub>CC</sub> = 3 V	12		
Δt/Δv	Input transition rise or fall rate		10		ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74ALVCH162820

## 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

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### ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
	I <sub>OH</sub> = -2 mA	1.65 V	1.2			
	I <sub>OH</sub> = -4 mA	2.3 V	1.9			
	I <sub>OH</sub> = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I <sub>OH</sub> = -8 mA	2.7 V	2			
	I <sub>OH</sub> = -12 mA	3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V	0.2			V
	I <sub>OL</sub> = 2 mA	1.65 V	0.45			
	I <sub>OL</sub> = 4 mA	2.3 V	0.4			
	I <sub>OL</sub> = 6 mA	2.3 V	0.55			
		3 V	0.55			
	I <sub>OL</sub> = 8 mA	2.7 V	0.6			
	I <sub>OL</sub> = 12 mA	3 V	0.8			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	µA
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25			µA
	V <sub>I</sub> = 1.07 V	1.65 V	-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V	2.3 V	-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	-75			
	V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V			±500	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND      I <sub>O</sub> = 0	3.6 V			40	µA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V,      Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND			3.5	pF
	Data inputs				6	
C <sub>o</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND			7	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

### TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	(1)		150		150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK↑	(1)		1.7		1.8		1.4		ns
t <sub>h</sub>	Hold time, data after CLK↑	(1)		1.1		1.1		1		ns

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			(1)		150		150		150		MHz
$t_{pd}$	CLK	Q		(1)	1	6.4		6.2	1	5.4	ns
$t_{en}$	$\overline{OE}$	Q		(1)	1	6.9		6.8	1	5.6	ns
$t_{dis}$	$\overline{OE}$	Q		(1)	1	6.2		5.5	1	5	ns

(1) This information was not available at the time of publication.

## OPERATING CHARACTERISTICS

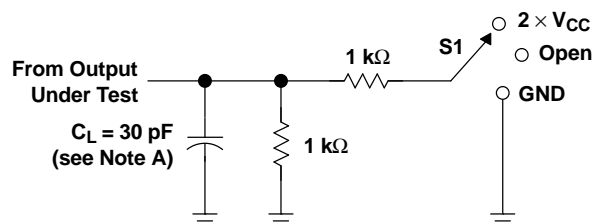
$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per flip-flop	All outputs enabled	$C_L = 50\text{ pF}, f = 10\text{ MHz}$	(1)	68	66	pF
		All outputs disabled		(1)	39	47	

(1) This information was not available at the time of publication.

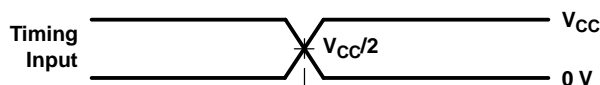
# PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8 \text{ V}$

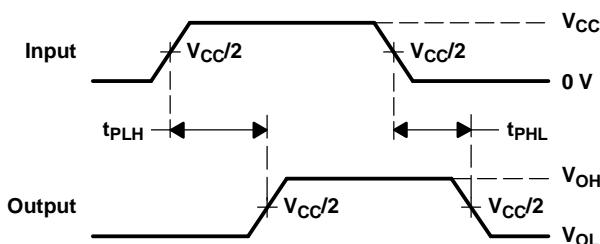


LOAD CIRCUIT

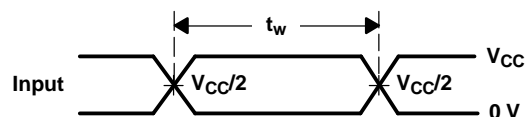
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



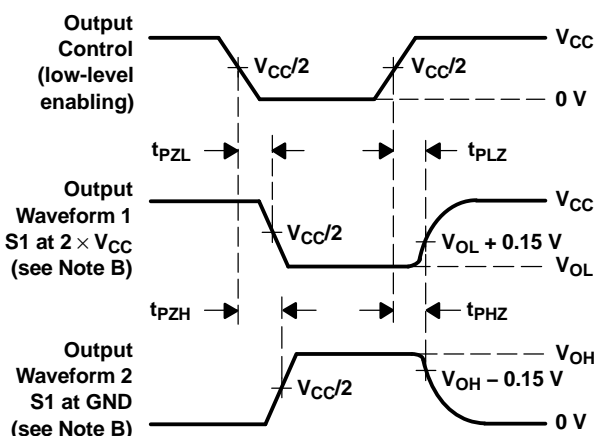
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



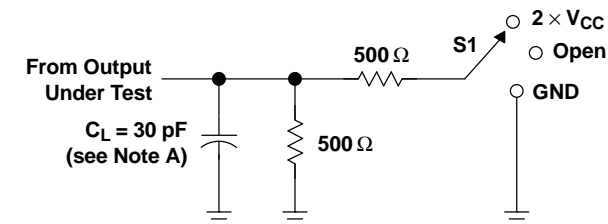
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

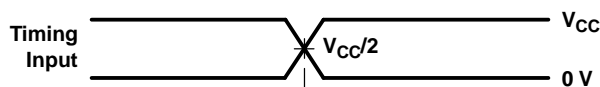
# PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

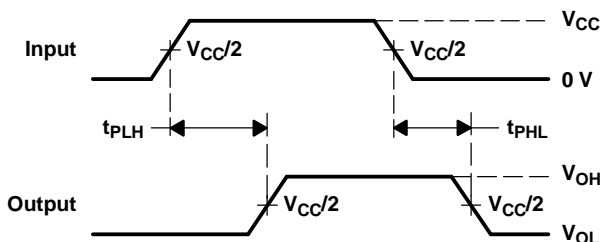


LOAD CIRCUIT

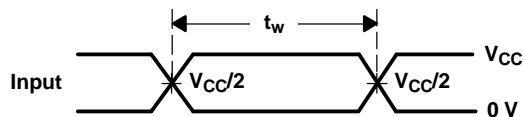
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



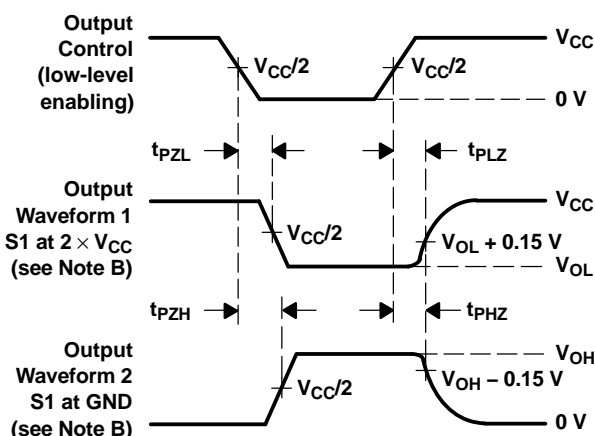
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

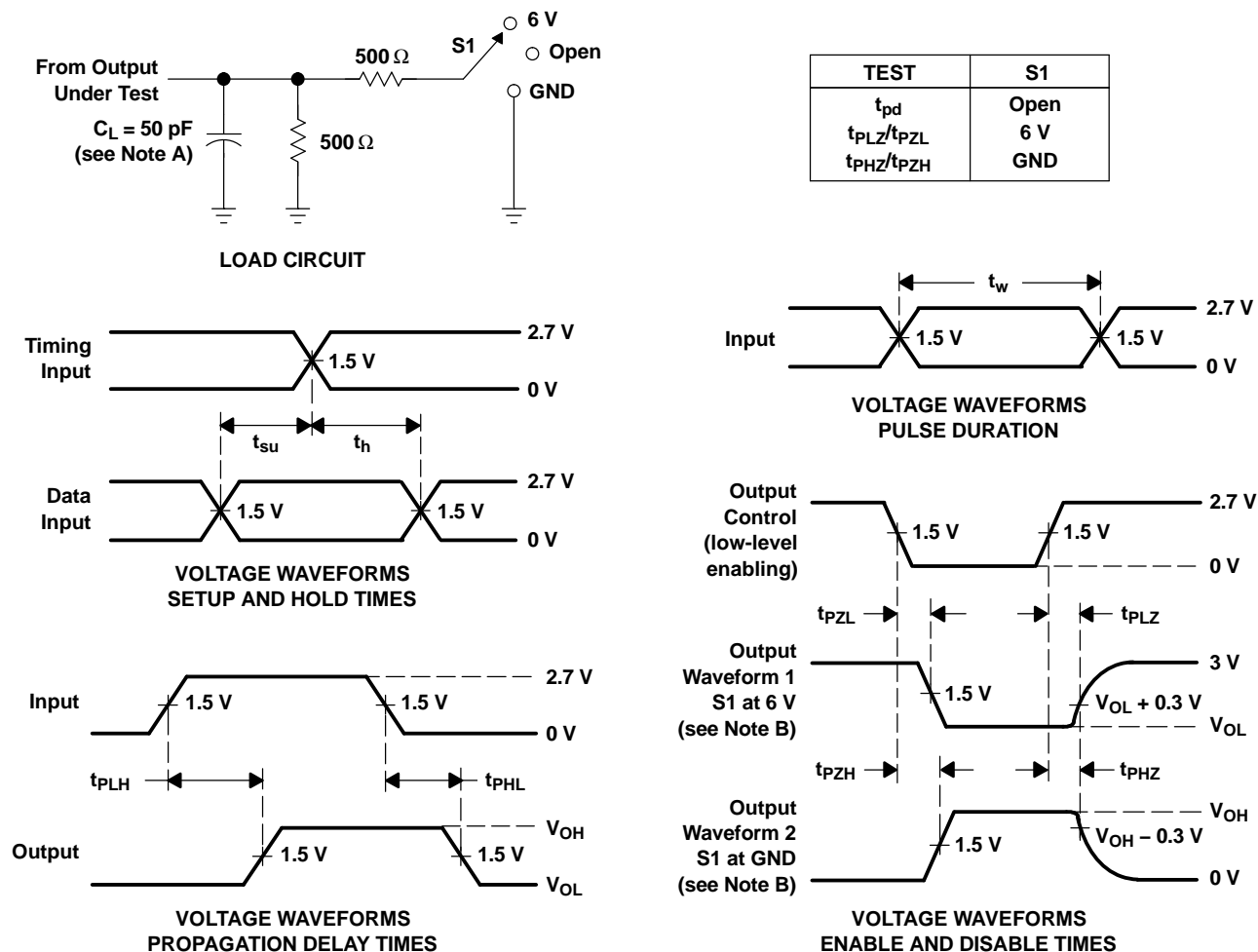
# SN74ALVCH162820

## 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

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### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V}$  AND  $3.3 \text{ V} \pm 0.3 \text{ V}$



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVCH162820DLG4	ACTIVE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85	ALVCH162820	<a href="#">Samples</a>
74ALVCH162820DLRG4	ACTIVE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85	ALVCH162820	<a href="#">Samples</a>
SN74ALVCH162820DGGR	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed  $0.006$  (0,15).
  - Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

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