

High Performance Selectable 1:4 Differential Fanout Buffer

Features

- 4 differential outputs with 2 banks
- User configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- LVCMOS reference output up to 200MHz
- Up to 1.5GHz output frequency for differential outputs
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. < 1.5ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TSSOP-28 package

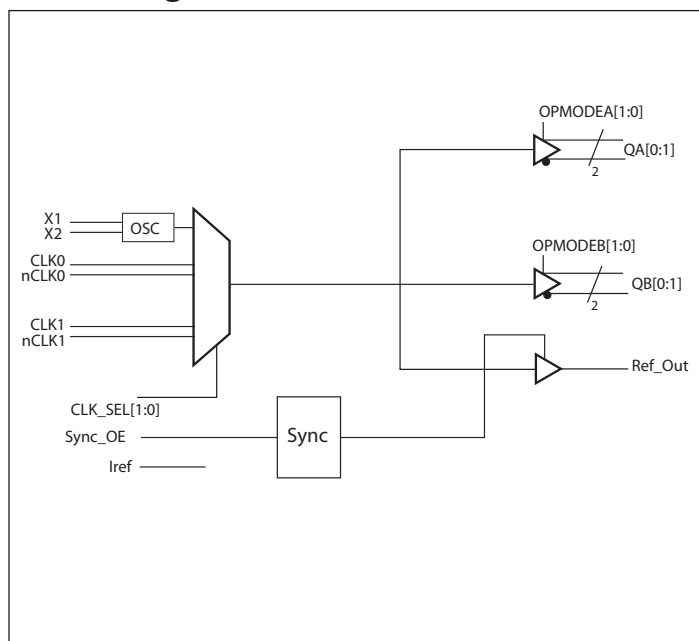
Description

The PI6C49S1504 is a high performance fanout buffer device which supports up to 1.5GHz frequency. The device also uses Pericom's proprietary input detection technique to make sure illegal input conditions will be detected and reflected by output states. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (28-Pin TSSOP)

VEE/GND	1	28	QA0
NC	2	27	nQA0
CLK_SEL0	3	26	VDDO
CLK_SEL1	4	25	OpModeA0
CLK0	5	24	OpModeA1
nCLK0	6	23	QA1
CLK1	7	22	nQA1
nCLK1	8	21	Ref_out
Xtal_In	9	20	QB0
Xtal_Out	10	19	nQB0
Sync_OE	11	18	OpModeB1
IREF	12	17	OpModeB0
VDD	13	16	VDDO
nQB1	14	15	QB1

Pinout Table

Pin #	Pin Name	Type	Description
1	V _{EE}	Power	Negative power supply
2	NC	-	No Connect
3	CLK_SEL0	Input	Clock input source selection pin
4	CLK_SEL1	Input	Clock input source selection pin
5, 6	CLK0 nCLK0	Input	Differential clock input
7, 8	CLK1 nCLK1	Input	Differential clock input
9	XTAL_In	Input	Xtal input pin
10	XTAL_Out	Output	Xtal output pin
11	Sync_OE	Input	Synchronous output enable for Ref_Out, see Table 3 for functions
12	IREF	Output	External 475Ω resistor connection to set differential output current
13	V _{DD}	Power	Power supply for core
14, 15	nQB1 QB1	Output	Differential output clock
16, 26	V _{DDO}	Power	Power supply for outputs
17	OpModeB0	Input	Bank B output clock type selection pin
18	OpModeB1	Input	Bank B output clock type selection pin
19, 20	nQB0 QB0	Output	Differential output clock
21	Ref_Out	Output	Reference output clock
22, 23	nQA1 QA1	Output	Differential output clock
24	OpModeA1	Input	Bank A output clock type selection pin
25	OpModeA0	Input	Bank A output clock type selection pin
27, 28	nQA0 QA0	Output	Differential output clock

Function Table

Table 1: Input select function

CLK_SEL [1]	CLK_SEL [0]	Function
0	0	XTAL is the selected input
0	1	CLK0 is the selected reference input
1	X	CLK1 is the selected reference input

Table 2: Output Mode select function

OPMODEA/B [1]	OPMODEA/B [0]	Output Bank A / Bank B Mode
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Table 3: Reference output enable function

Sync_OE	Ref_Out
0	Hi-Z
1	Output enabled

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
 Supply Voltage to Ground Potential (V_{DD} , V_{DDO}) . -0.5 to +4.6V
 Inputs (Referenced to GND) -0.5 to $V_{CC}+0.5V$
 Clock Output (Referenced to GND)..... -0.5 to $V_{CC}+0.5V$
 Latch up.....200mA

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375		3.465	V
V_{DDO}	Output Supply Voltage		2.375		3.465	V
I_{DD}	Core Power Supply Current				70	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded			60	
		All LVDS outputs loaded			70	
		All HCSL outputs unloaded			45	
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - Differential Inputs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
C_{IN}	Input capacitance			3		pF
V_{IH}	Input high voltage				$V_{DD}+0.3$	V
V_{IL}	Input low voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK		0.15		1.3	V
V_{CM}	Common model input voltage	$V_{ID} > 0.4V$	GND + 0.26		$V_{DD}-0.85$	V

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	μA
I_{IL}	Input Low current	Input = GND	-150			μA
V_{IH}	Input high voltage	$V_{DD}=3.3V$	2.0		$V_{DD}+0.3$	V
V_{IL}	Input low voltage	$V_{DD}=3.3V$	-0.3		0.8	V
V_{IH}	Input high voltage	$V_{DD}=2.5V$	1.7		$V_{DD}+0.3$	V
V_{IL}	Input low voltage	$V_{DD}=2.5V$	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	$V_{DD}=3.3V$	2.1		2.6	V
		$V_{DD}=2.5V$	1.3		1.6	
V_{OL}	Output Low voltage	$V_{DD}=3.3V$	1.2		1.8	V
		$V_{DD}=2.5V$	0.4		0.8	

DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage		0.35		0.55	V
V_{ocm}	Output commode voltage		1.1	1.2	1.3	V
DV_{Ocm}	Change in V_{ocm} between completely output states				50	mV
R_o	Output impedance		85		140	Ω

DC Electrical Specifications- HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V _{OH}	Output High voltage		520		900	mV
V _{OL}	Output Low voltage		0		150	mV

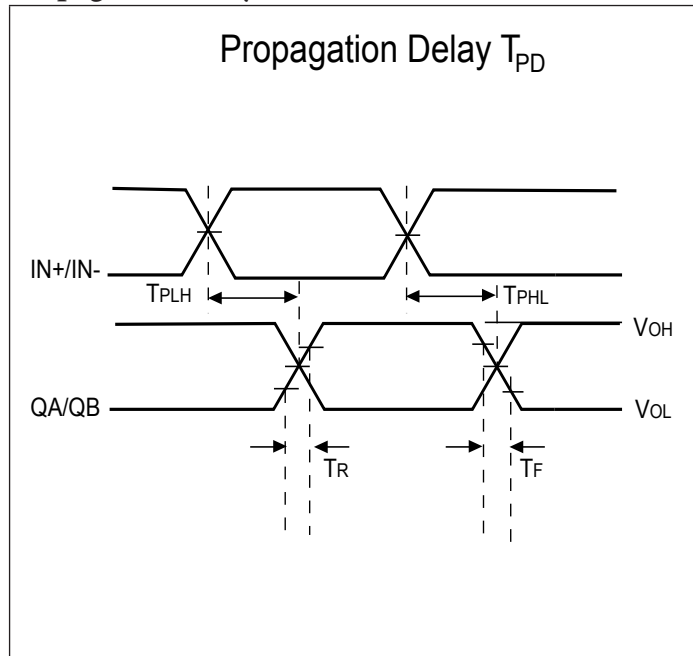
AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F _{OUT}	Clock output frequency	LVPECL, LVDS			1500	MHz
		HCSL			250	
T _r	Output rise time	From 20% to 80%, LVPECL, LVDS	120	150	300	ps
		From 20% to 80%, HCSL	350	460	650	ps
T _f	Output fall time	From 80% to 20%, LVPECL, LVDS	120	150	300	ps
		From 80% to 20%, HCSL	350	460	650	ps
T _{ODC}	Output duty cycle	Frequency<650MHz, LVPECL	48		52	%
		Frequency<650MHz, LVDS	47		53	%
V _{PP}	Output swing Single-ended	LVPECL outputs	400			mV
		LVDS outputs, <650MHz	250			mV
		HCSL outputs	480			mV
T _j	Buffer additive jitter RMS			0.03		ps
V _{CROSS}	Absolute crossing voltage	HCSL	160		460	mV
DV _{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T _{SK}	Output Skew	10 outputs devices, outputs in same tank, with same load, at DUT.		40		ps
T _{PD}	Propagation Delay			1500		ps
T _{OD}	Valid to HiZ		200			ns
T _{OE}	HiZ to valid		200			ns

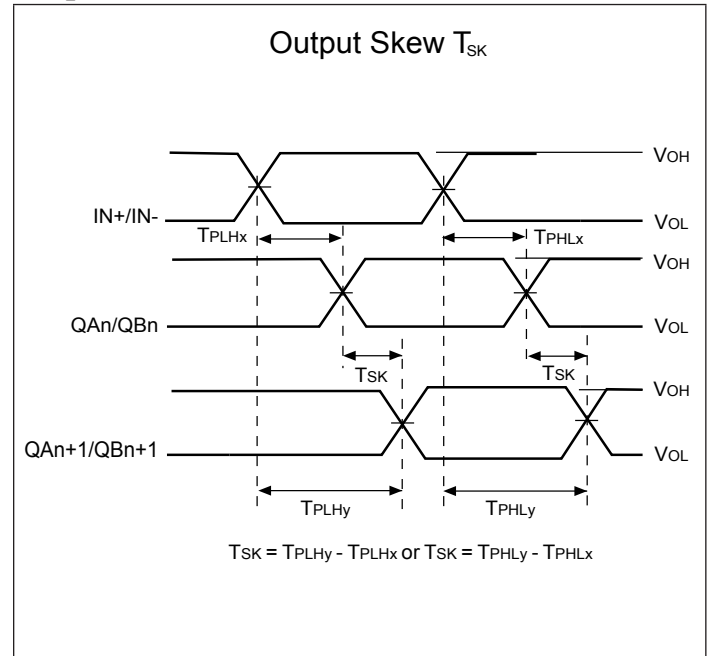
Notes:

1. This parameter is guaranteed by design

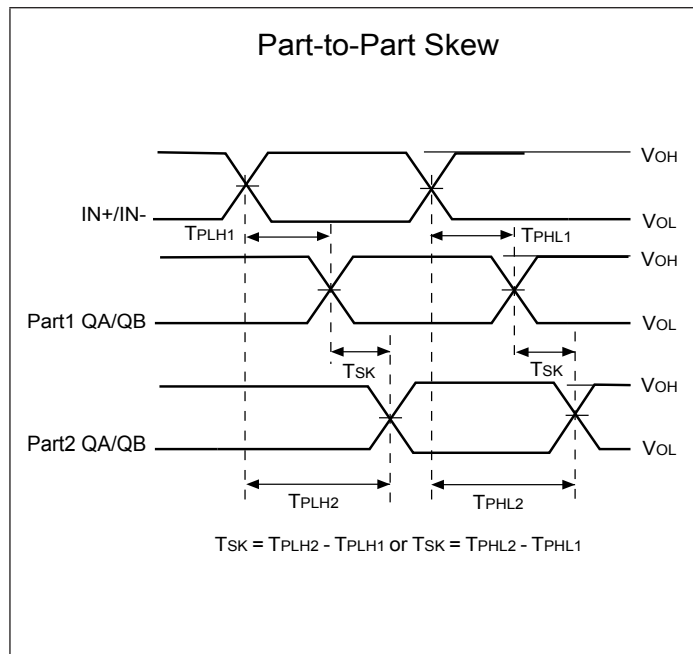
Propagation Delay



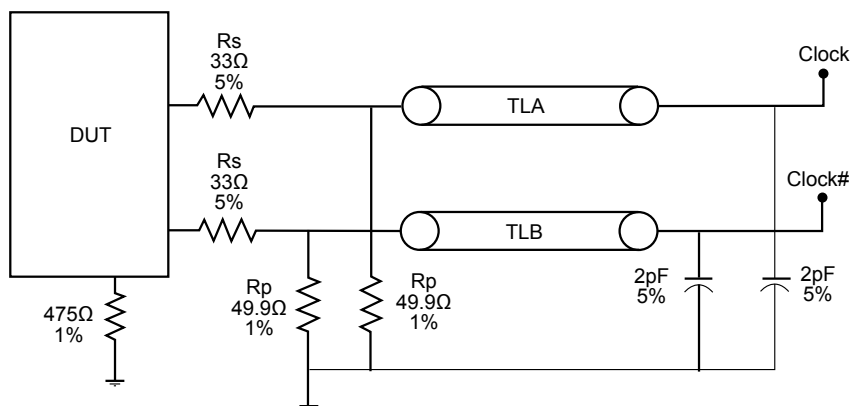
Output Skew



Part to Part Skew

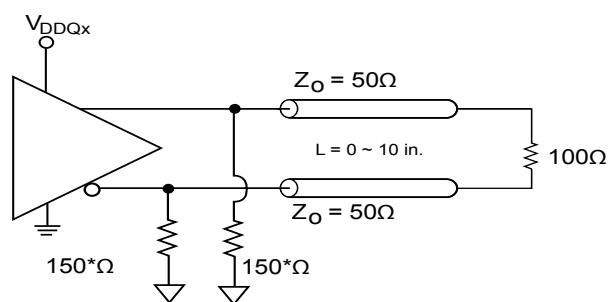


Configuration Test Load Board Termination for HCSL Outputs



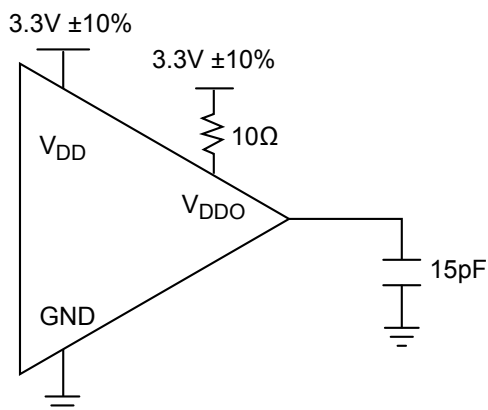
Configuration Test Load Board Termination for LVPECL/ LVDS Outputs

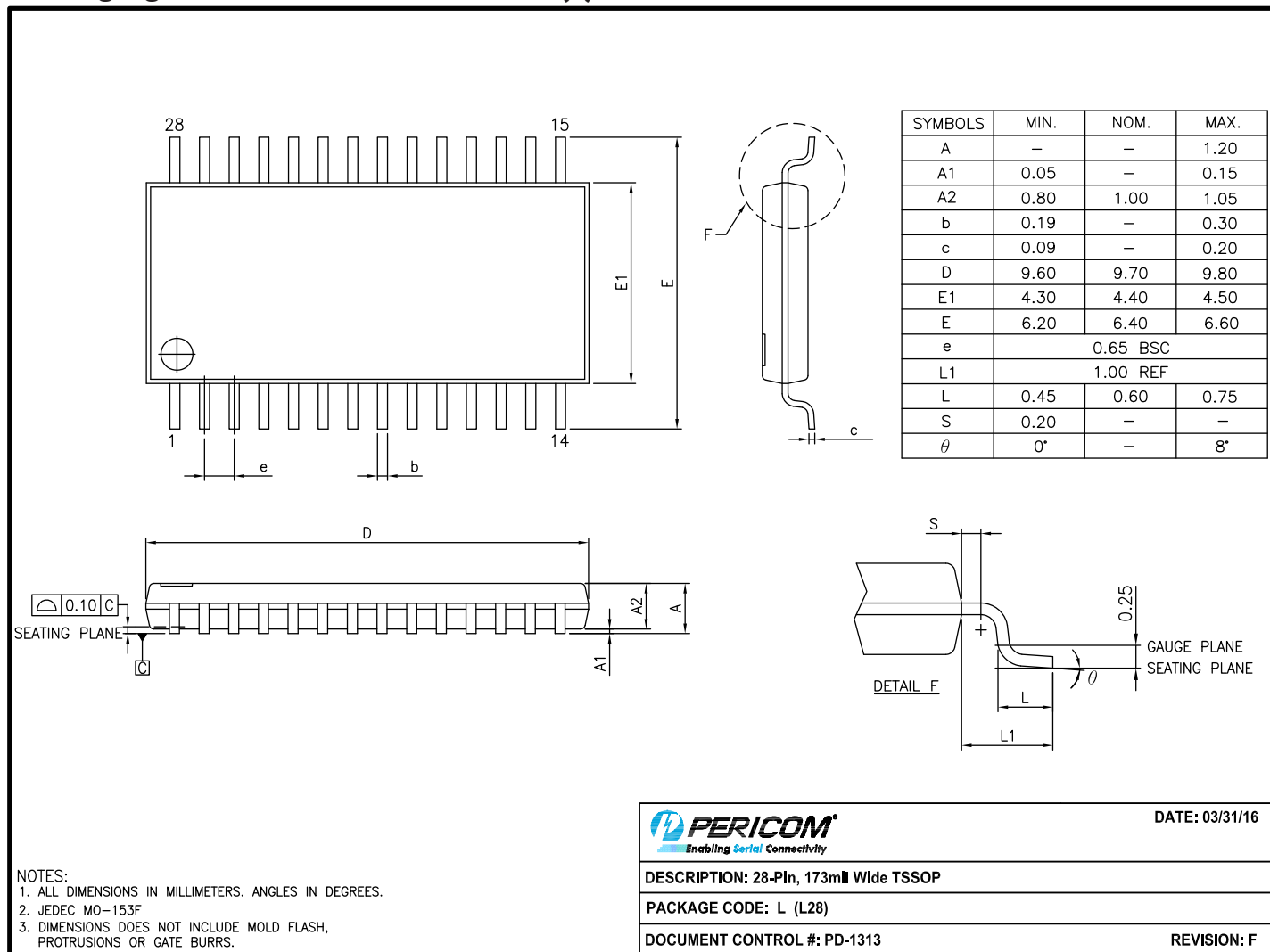
LVPECL Buffer



* remove for LVDS

Configuration Test Load Board Termination for LVC MOS Outputs



PI6C49S1504
Packaging Mechanical: 28-Pin TSSOP (L)


16-0076

 Note: For latest package info, please check: <http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/>
Ordering Information⁽¹⁻³⁾

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C49S1504LIE	L	28-pin, 173mil Wide (TSSOP)	-40 °C to 85 °C
PI6C49S1504LIEEX	L	28-pin, 173mil Wide (TSSOP), Tape & Reel	-40 °C to 85 °C

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. "E" denotes Pb-free and Green
3. Adding an "X" at the end of the ordering code denotes tape and Reel packaging