

2N6400 Series

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

Features

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 V
- These are Pb-Free Devices

MAXIMUM RATINGS* ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($T_J = -40$ to 125°C , Sine Wave 50 to 60 Hz; Gate Open)	V_{DRM} , V_{RRM}	50 100 200 400 600 800	V
On-State Current RMS (180° Conduction Angles; $T_C = 100^\circ\text{C}$)	$I_{\text{T(RMS)}}$	16	A
Average On-State Current (180° Conduction Angles; $T_C = 100^\circ\text{C}$)	$I_{\text{T(AV)}}$	10	A
Peak Non-repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, $T_J = 25^\circ\text{C}$)	I_{TSM}	160	A
Circuit Fusing Considerations ($t = 8.3$ ms)	I^2t	145	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1.0 μs , $T_C = 100^\circ\text{C}$)	P_{GM}	20	W
Forward Average Gate Power ($t = 8.3$ ms, $T_C = 100^\circ\text{C}$)	$P_{\text{G(AV)}}$	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs , $T_C = 100^\circ\text{C}$)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	-40 to $+125$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to $+150$	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

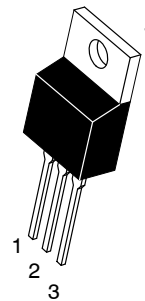
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



ON Semiconductor®

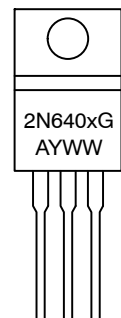
<http://onsemi.com>

SCRs
16 AMPERES RMS
50 thru 800 VOLTS



TO-220AB
CASE 221A
STYLE 3

MARKING DIAGRAM



x = 0, 1, 2, 3, 4 or 5
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

PIN ASSIGNMENT

	PIN ASSIGNMENT
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

2N6400 Series

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.5	$^{\circ}\text{C/W}$
Maximum Lead Temperature for Soldering Purposes 1/8 in from Case for 10 Seconds	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

*Peak Repetitive Forward or Reverse Blocking Current ($V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$, Gate Open) $T_J = 25^{\circ}\text{C}$ $T_J = 125^{\circ}\text{C}$	I_{DRM} , I_{RRM}	–	–	10 2.0	μA mA
--	--------------------------	---	---	-----------	---------------------

ON CHARACTERISTICS

*Peak Forward On-State Voltage ($I_{TM} = 32 \text{ A Peak}$, Pulse Width $\leq 1 \text{ ms}$, Duty Cycle $\leq 2\%$)	V_{TM}	–	–	1.7	V
*Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 100 \Omega$) $T_C = 25^{\circ}\text{C}$ $T_C = -40^{\circ}\text{C}$	I_{GT}	–	9.0 –	30 60	mA
*Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 100 \Omega$) $T_C = 25^{\circ}\text{C}$ $T_C = -40^{\circ}\text{C}$	V_{GT}	–	0.7 –	1.5 2.5	V
Gate Non-Trigger Voltage ($V_D = 12 \text{ Vdc}$, $R_L = 100 \Omega$), $T_C = +125^{\circ}\text{C}$	V_{GD}	0.2	–	–	V
*Holding Current ($V_D = 12 \text{ Vdc}$, Initiating Current = 200 mA, Gate Open) $T_C = 25^{\circ}\text{C}$ * $T_C = -40^{\circ}\text{C}$	I_H	–	18 –	40 60	mA
Turn-On Time ($I_{TM} = 16 \text{ A}$, $I_{GT} = 40 \text{ mAdc}$, $V_D = \text{Rated } V_{DRM}$)	t_{gt}	–	1.0	–	μs
Turn-Off Time ($I_{TM} = 16 \text{ A}$, $I_R = 16 \text{ A}$, $V_D = \text{Rated } V_{DRM}$) $T_C = 25^{\circ}\text{C}$ $T_J = +125^{\circ}\text{C}$	t_q	–	15 35	– –	μs

DYNAMIC CHARACTERISTICS

Critical Rate-of-Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}$, Exponential Waveform) $T_J = +125^{\circ}\text{C}$	dv/dt	–	50	–	V/ μs
--	---------	---	----	---	------------------

*Indicates JEDEC Registered Data.

2N6400 Series

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current

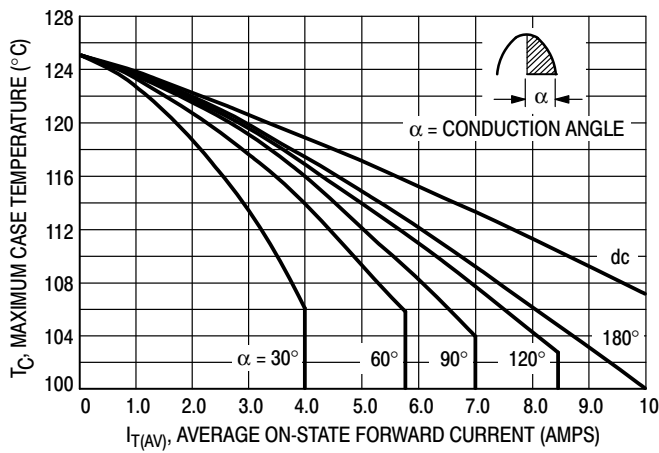
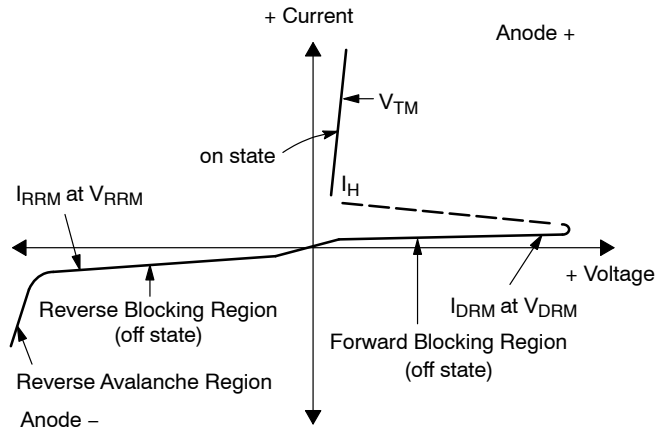


Figure 1. Average Current Derating

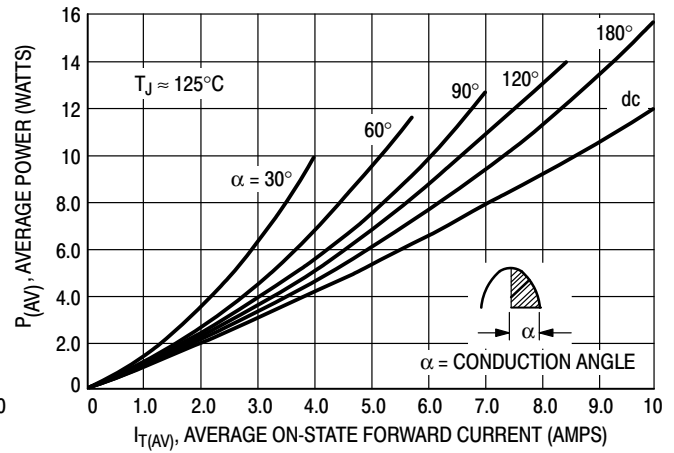


Figure 2. Maximum On-State Power Dissipation

2N6400 Series

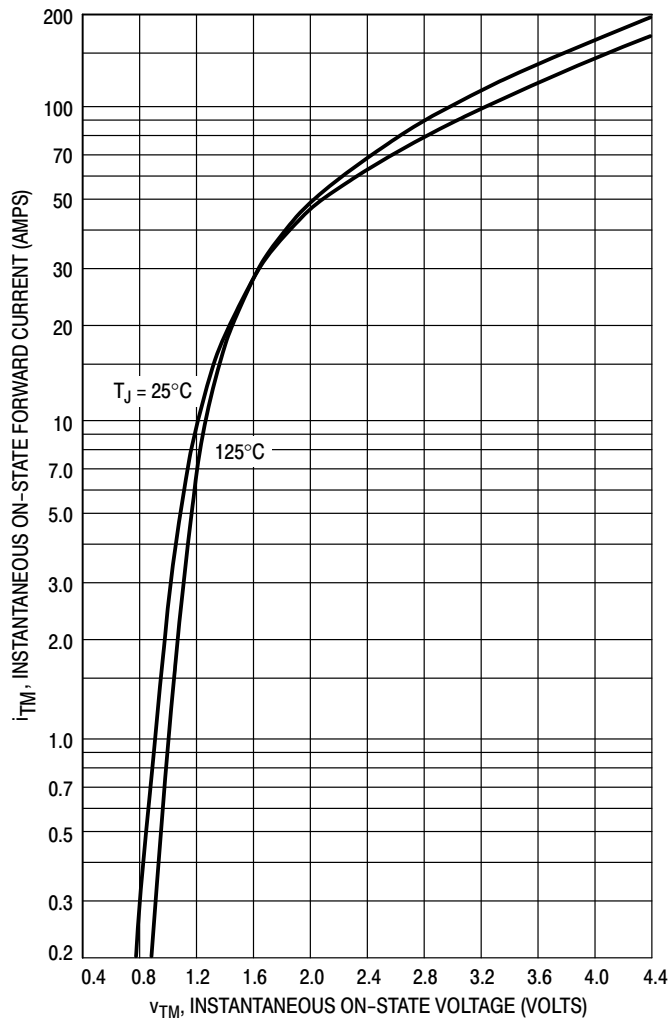


Figure 3. On-State Characteristics

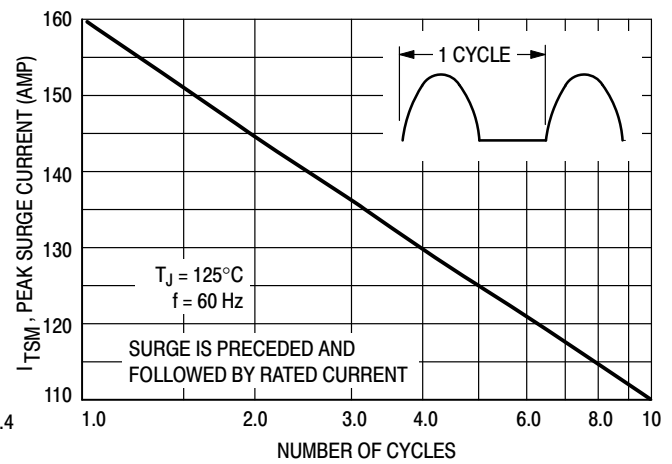


Figure 4. Maximum Non-Repetitive Surge Current

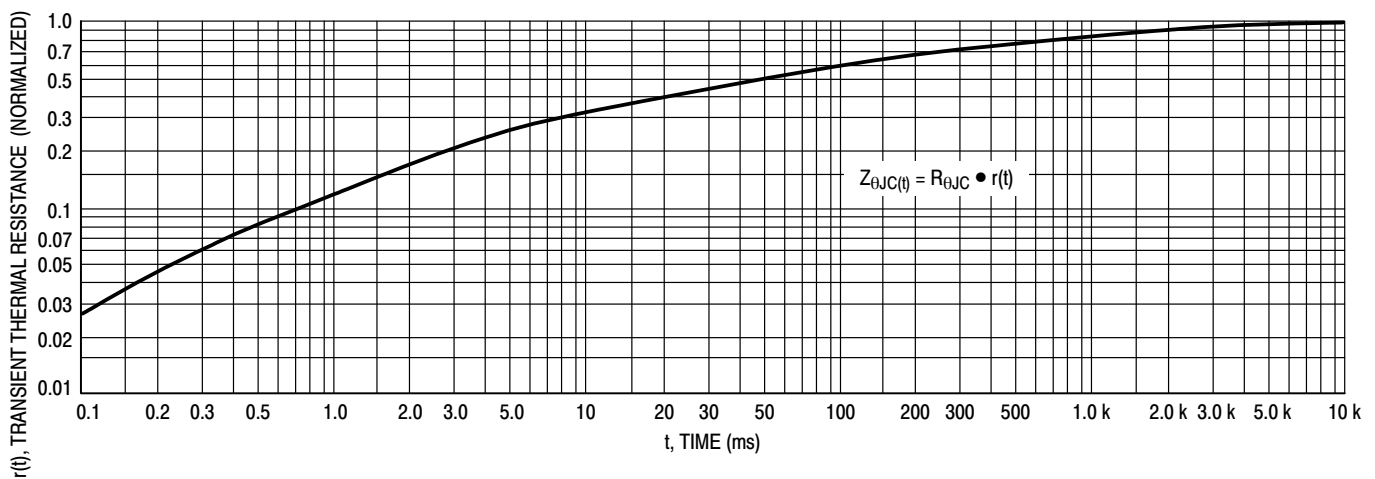


Figure 5. Thermal Response

2N6400 Series

TYPICAL CHARACTERISTICS

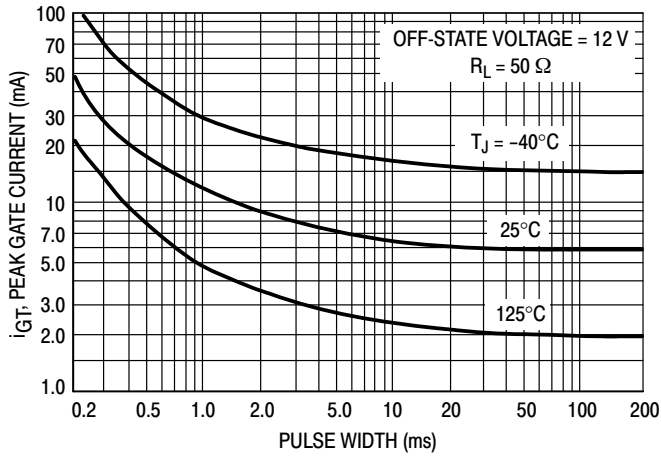


Figure 6. Typical Gate Trigger Current versus Pulse Width

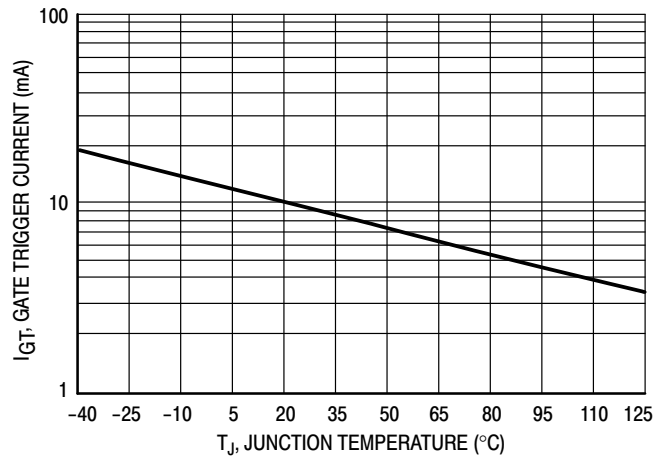


Figure 7. Typical Gate Trigger Current versus Junction Temperature

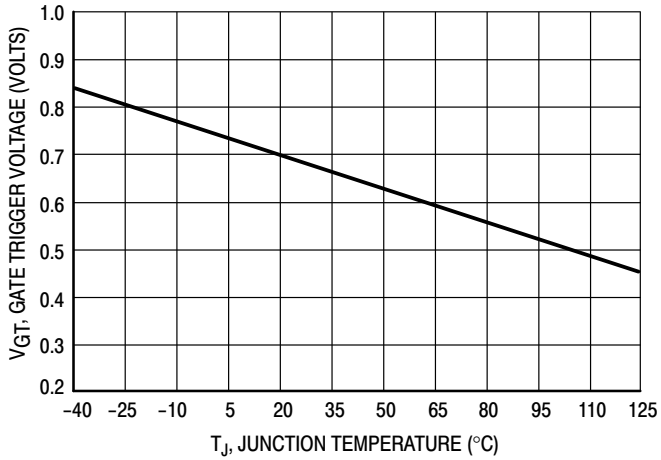


Figure 8. Typical Gate Trigger Voltage versus Junction Temperature

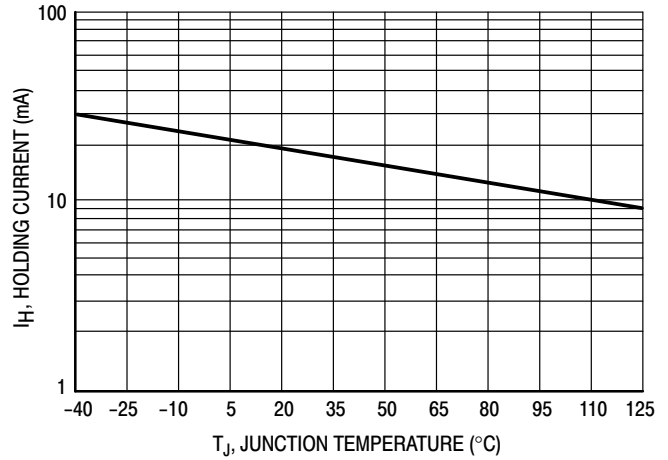


Figure 9. Typical Holding Current versus Junction Temperature

2N6400 Series

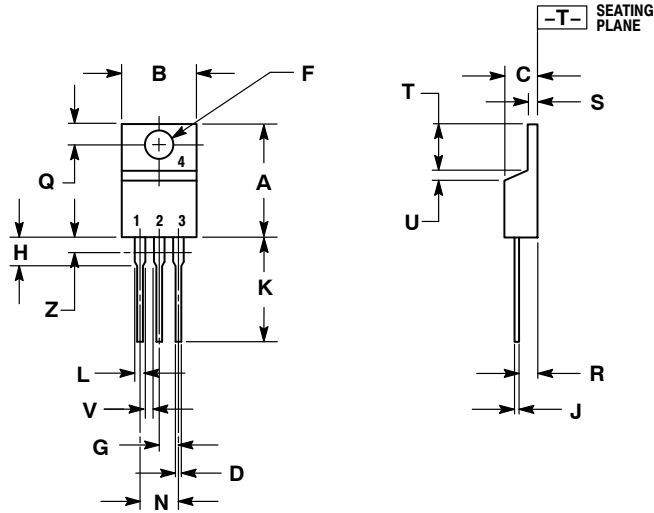
ORDERING INFORMATION

Device	Package	Shipping [†]
2N6400G	TO-220AB (Pb-Free)	500 Units / Box
2N6401G	TO-220AB (Pb-Free)	
2N6402G	TO-220AB (Pb-Free)	
2N6403G	TO-220AB (Pb-Free)	
2N6403TG	TO-220AB (Pb-Free)	50 Units / Rail
2N6404G	TO-220AB (Pb-Free)	500 Units / Box
2N6405G	TO-220AB (Pb-Free)	

2N6400 Series

PACKAGE DIMENSIONS

TO-220 CASE 221A-07 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 3:

- PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative