

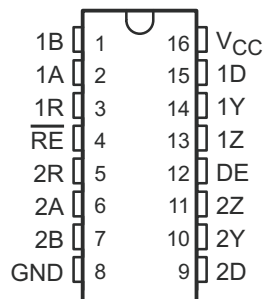
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

Check for Samples: [SN65C1167](#) [SN75C1167](#) [SN65C1168](#) [SN75C1168](#)

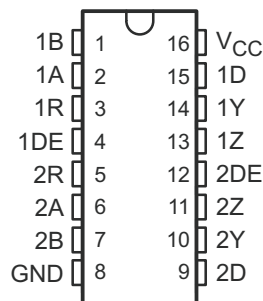
FEATURES

- Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11
- BiCMOS Process Technology
- Low Supply-Current Requirements: 9 mA Max
- Low Pulse Skew
- Receiver Input Impedance . . . 17 k Ω Typ
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Common-Mode Input Voltage Range of -7 V to 7 V
- Operate From Single 5-V Power Supply
- Glitch-Free Power-Up/Power-Down Protection
- Receiver 3-State Outputs Active-Low Enable for SN65C1167 and SN75C1167 Only
- Improved Replacements for the MC34050 and MC34051

SN65C1167 . . . DB OR NS PACKAGE
SN75C1167 . . . DB, N, OR NS PACKAGE
(TOP VIEW)



SN65C1168 . . . N, NS, OR PW PACKAGE
SN75C1168 . . . DB, N, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION

The SN65C1167, SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾ (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN75C1167N	SN75C1167N
			SN75C1168N	SN75C1168N
	SOP – NS	Tape and reel	SN75C1167NSR	75C1167
			SN75C1168NSR	75C1168
	SSOP – DB	Tape and reel	SN75C1167DBR	CA1167
			SN75C1168DBR	CA1168
	TSSOP – PW	Tube	SN75C1168PW	CA1168
		Tape and reel	SN75C1168PWR	
–40°C to 85°C	PDIP – N	Tube	SN65C1168N	SN65C1168N
	SOP – NS	Tape and reel	SN65C1167NSR	65C1167
			SN65C1168NSR	65C1168
	SSOP – DB	Tape and reel	SN65C1167DBR	CB1167
	TSSOP – PW	Tube	SN65C1168PW	CB1168
		Tape and reel	SN65C1168PWR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/sc/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

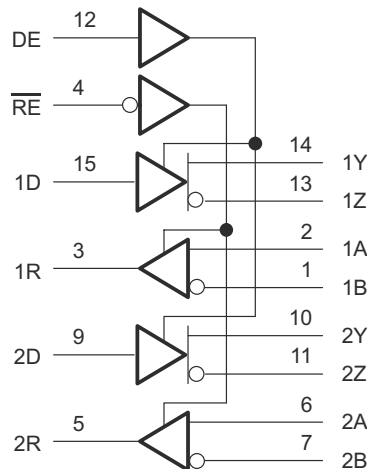
Each Receiver⁽¹⁾

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

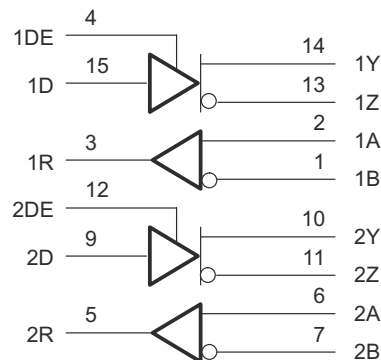
(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)

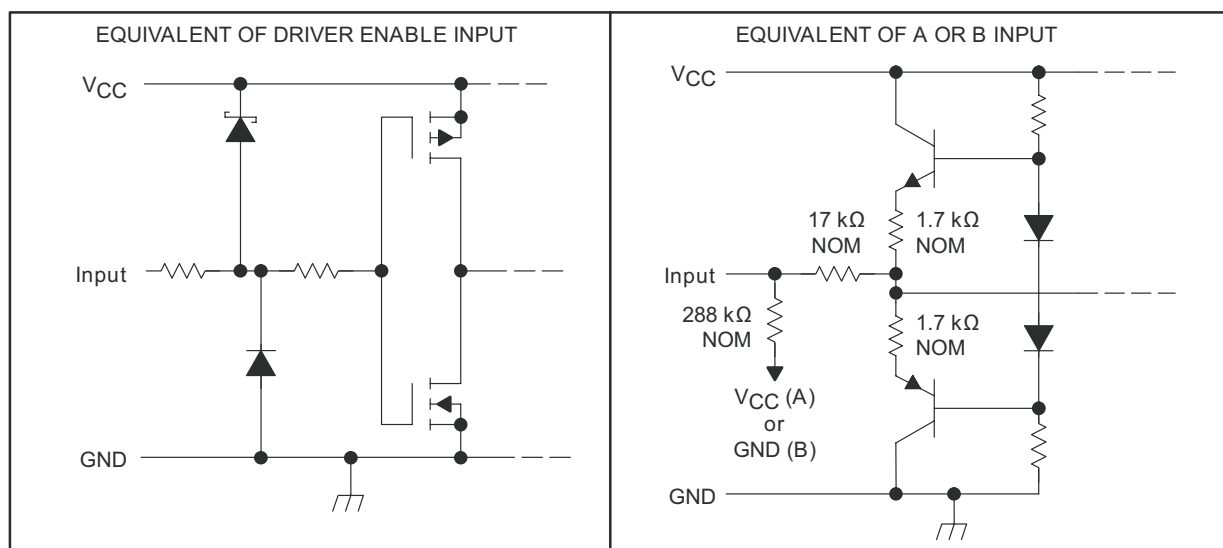
SN65C1167/SN75C1167



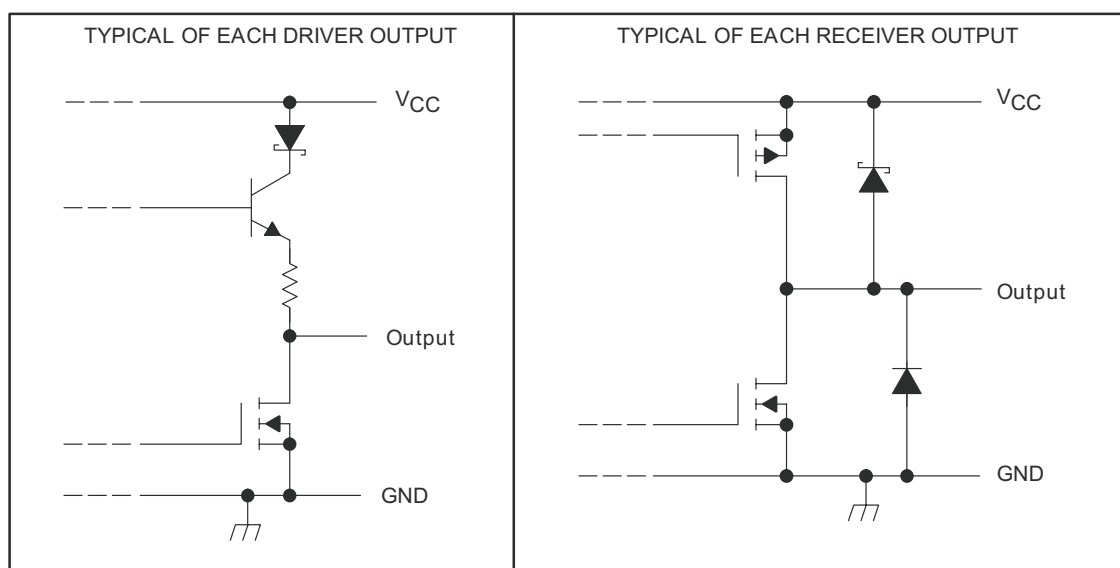
SN65C1168, SN75C1168



SCHEMATIC OF INPUTS



SCHEMATIC OF OUTPUTS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		–0.5	7	V
V _I	Input voltage range	Driver	–0.5	V _{CC} + 0.5	V
		A or B, Receiver	–11	14	
V _{ID}	Differential input voltage range ⁽³⁾	Receiver	–14	14	V
V _O	Output voltage range	Driver	–0.5	7	V
I _{IK} or I _{OK}	Clamp current range	Driver		±20	mA
I _O	Output current range	Driver		±150	mA
		Receiver		±25	
I _{CC}	Supply current			200	mA
	GND current			–200	mA
T _J	Operating virtual junction temperature			150	°C
θ _{JA}	Package thermal impedance ^{(4) (5)}	DB package		82	°C/W
		N package		67	
		NS package		64	
		PW package		108	
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages values except differential input voltage are with respect to the network GND.
- (3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
- (4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IC}	Common-mode input voltage ⁽¹⁾	Receiver			±7	V
V _{ID}	Differential input voltage	Receiver			±7	V
V _{IH}	High-level input voltage	Except A, B	2			V
V _{IL}	Low-level input voltage	Except A, B			0.8	V
I _{OH}	High-level output current	Receiver			–6	mA
		Driver			–20	
I _{OL}	Low-level output current	Receiver			6	mA
		Driver			20	
T _A	Operating free-air temperature	SN75C1167, SN75C1168	0		70	°C
		SN65C1167, SN65C1168	–40		85	

- (1) Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -20 \text{ mA}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 20 \text{ mA}$		0.2	0.4	V
$ V_{OD1} $ Differential output voltage	$I_O = 0 \text{ mA}$	2		6	V
$ V_{OD2} $ Differential output voltage ⁽¹⁾	$R_L = 100 \Omega$, See Figure 1	2	3.1		V
$\Delta V_{OD} $ Change in magnitude of differential output voltage				± 0.4	V
V_{OC} Common-mode output voltage				± 3	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage				± 0.4	V
$I_{O(OFF)}$ Output current with power off	$V_{CC} = 0 \text{ V}$			100	μA
	$V_O = 6 \text{ V}$			-100	
	$V_O = -0.25 \text{ V}$				
I_{OZ} High-impedance-state output current	$V_O = 2.5 \text{ V}$			20	μA
	$V_O = 5 \text{ V}$			-20	
I_{IH} High-level input current	$V_I = V_{CC}$ or V_{IH}			1	μA
I_{IL} Low-level input current	$V_I = \text{GND}$ or V_{IL}			-1	μA
I_{OS} Short-circuit output current ⁽³⁾	$V_O = V_{CC}$ or GND ,	-30		-150	mA
I_{CC} Supply current (total package) ⁽⁴⁾	No load, Enabled		$V_I = V_{CC}$ or GND	4	6
			$V_I = 2.4$ or 0.5 V	5	3
C_i Input capacitance			6		pF

(1) Refer to TIA/EIA-422-B for exact conditions.

(2) All typical values are at $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND .

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PHL} Propagation delay time, high- to low-level output	$R1 = R2 = 50 \Omega$, $R3 = 500 \Omega$, $C1 = C2 = C3 = 40 \text{ pF}$, S1 is open, See Figure 2		7	12	ns
t_{PLH} Propagation delay time, low- to high-level output			7	12	ns
$t_{sk(p)}$ Pulse skew			0.5	4	ns
t_r Rise time	$R1 = R2 = 50 \Omega$, $R3 = 500 \Omega$, $C1 = C2 = C3 = 40 \text{ pF}$, S1 is open, See Figure 3		5	10	ns
t_f Fall time			5	10	ns
t_{PZH} Output enable time to high level	$R1 = R2 = 50 \Omega$, $R3 = 500 \Omega$, $C1 = C2 = C3 = 40 \text{ pF}$, S1 is closed, See Figure 4		10	19	ns
t_{PZL} Output enable time to low level			10	19	ns
t_{PHZ} Output disable time from low level	$R1 = R2 = 50 \Omega$, $R3 = 500 \Omega$, $C1 = C2 = C3 = 40 \text{ pF}$, S1 is closed, See Figure 4		7	16	ns
t_{PLZ} Output disable time from high level			7	16	ns

(1) All typical values are at $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

RECEIVER SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage, differential input					0.2	V
V _{IT-}	Negative-going input threshold voltage, differential input			-0.2 ⁽²⁾			V
V _{hys}	Input hysteresis (V _{IT+} – V _{IT-})				60		mV
V _{IK}	Input clamp voltage, $\overline{RE}$	SN75C1167	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage		V _{ID} = 200 mV, I _{OH} = -6 mA	3.8	4.2		V
V _{OL}	Low-level output voltage		V _{ID} = -200 mV, I _{OL} = 6 mA		0.1	0.3	V
I _{OZ}	High-impedance-state output current	SN75C1167	V _O = V _{CC} or GND		±0.5	±5	μA
I _I	Line input current		Other input at 0 V			1.5	mA
			V _I = 10 V V _I = -10 V			-2.5	
I _I	Enable input current, $\overline{RE}$	SN75C1167	V _I = V _{CC} or GND			±1	μA
r _i	Input resistance		V _{IC} = -7 V to 7 V, Other input at 0 V	4	17		kΩ
I _{CC}	Supply current (total package)		No load, Enabled			4	mA
			V _I = V _{CC} or GND V _{IH} = 2.4 V or 0.5 V ⁽³⁾			5	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) Refer to TIA/EIA-422-B for exact conditions.

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	See Figure 5	9	17	27	ns
t _{PHL}	Propagation delay time, high- to low-level output		9	17	27	ns
t _{TLH}	Transition time, low- to high-level output	V _{IC} = 0 V, See Figure 5		4	9	ns
t _{THL}	Transition time, high- to low-level output			4	9	ns
t _{PZH}	Output enable time to high level	R _L = 1 kW, See Figure 6		13	22	ns
t _{PZL}	Output enable time to low level			13	22	ns
t _{PHZ}	Output disable time from high level			13	22	ns
t _{PLZ}	Output disable time from low level			13	22	ns

(1) Measured per input while the other inputs are at V_{CC} or GND

(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

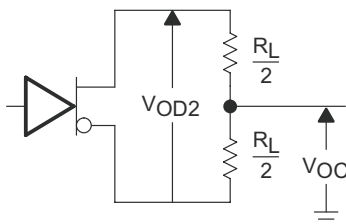


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

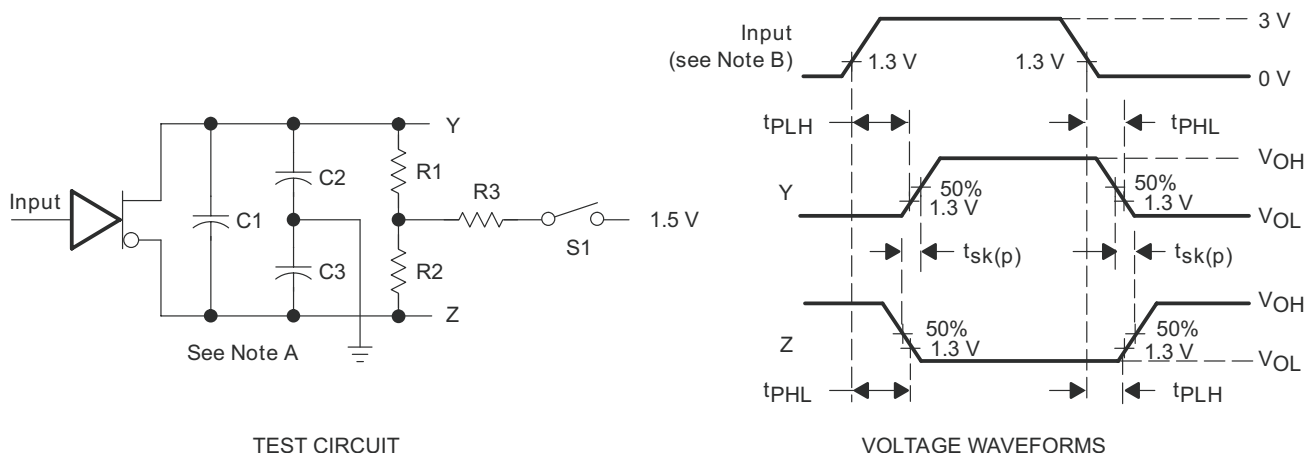


Figure 2. Driver Test Circuit and Voltage Waveforms

- C. C1, C2, and C3 include probe and jig capacitance.
- D. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

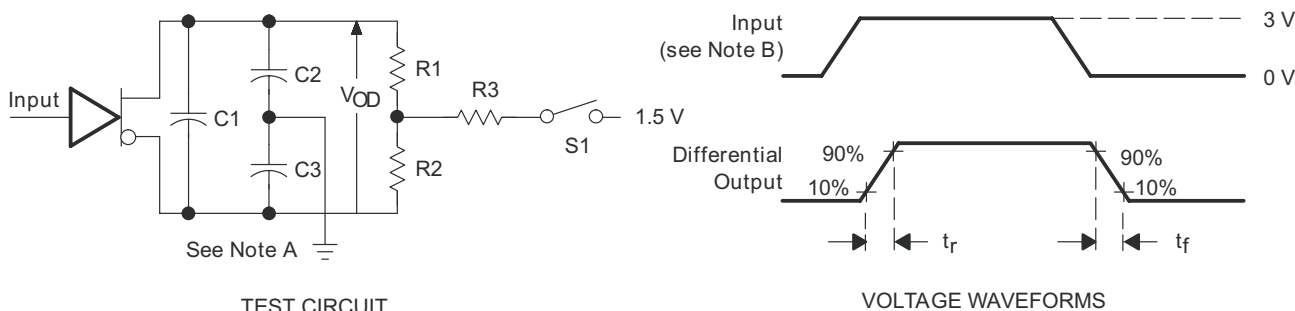


Figure 3. Driver Test Circuit and Voltage Waveforms

- E. C1, C2, and C3 include probe and jig capacitance.
- F. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

PARAMETER MEASUREMENT INFORMATION (continued)

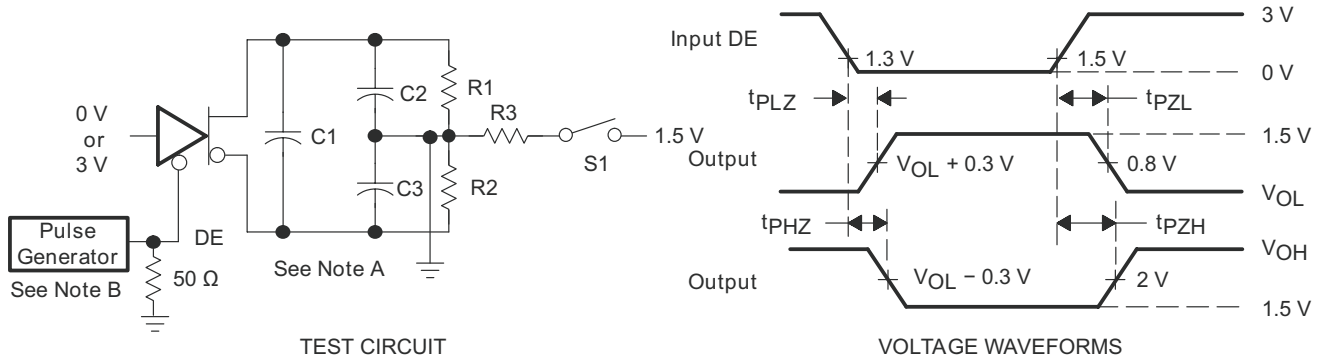


Figure 4. Driver Test Circuit and Voltage Waveforms

- G. C_L includes probe and jig capacitance.
H. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

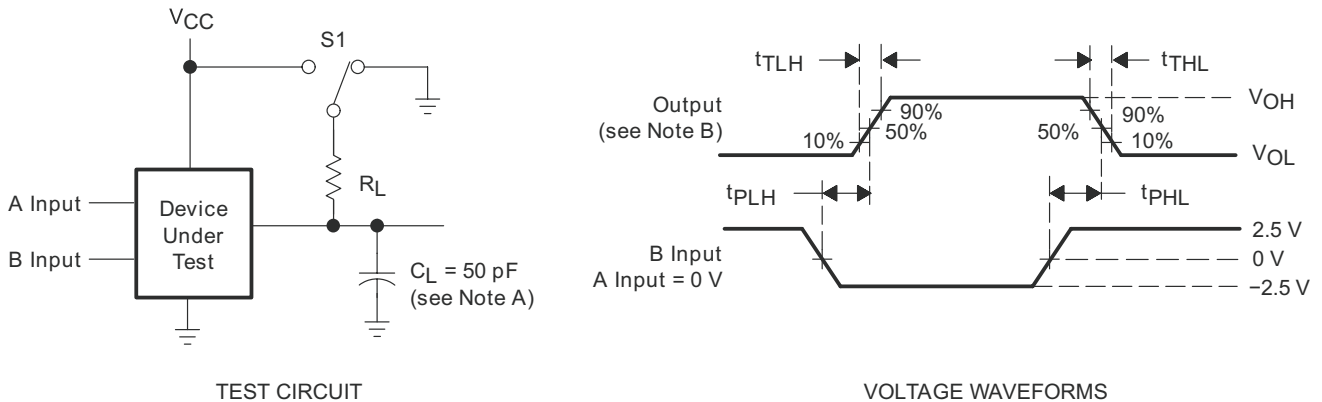


Figure 5. Receiver Test Circuit and Voltage Waveforms

- I. C_L includes probe and jig capacitance.
J. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

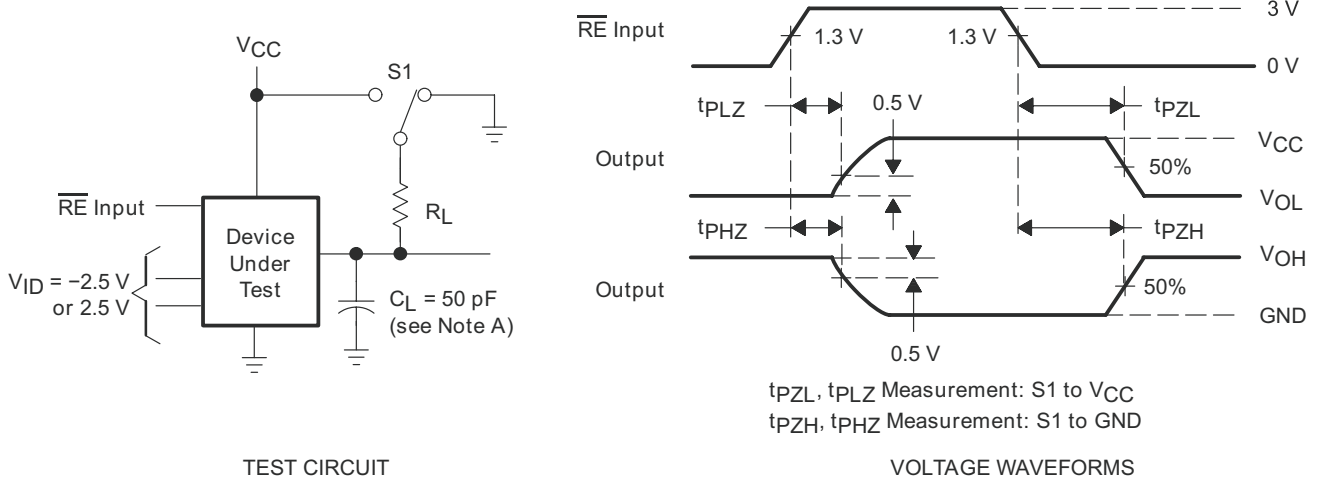


Figure 6. Receiver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65C1167NSLE	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI			
SN65C1167NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	Samples
SN65C1167NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	Samples
SN65C1167NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	Samples
SN65C1168N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN65C1168N	Samples
SN65C1168NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN65C1168N	Samples
SN65C1168NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168	Samples
SN65C1168NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168	Samples
SN65C1168PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN75C1167DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167	Samples
SN75C1167DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167	Samples
SN75C1167DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75C1167N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C1167N	Samples
SN75C1167NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C1167N	Samples
SN75C1167NSLE	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		
SN75C1167NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	Samples
SN75C1167NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	Samples
SN75C1168DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C1168N	Samples
SN75C1168NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C1168N	Samples
SN75C1168NSLE	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		
SN75C1168NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	Samples
SN75C1168NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	Samples
SN75C1168NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	Samples
SN75C1168PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75C1168PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1167NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C1167DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75C1168DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1167NSR	SO	NS	16	2000	367.0	367.0	38.0
SN65C1168NSR	SO	NS	16	2000	367.0	367.0	38.0
SN65C1168PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN75C1167DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN75C1168DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN75C1168PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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