IS31FL3193D

3-CHANNEL FUN LED DRIVER

May 2015

GENERAL DESCRIPTION

IS31FL3193D is a 3-channel fun LED driver which features two-dimensional auto breathing mode. It has One Shot Programming mode and PWM Control mode for RGB lighting effects. The maximum output current can be adjusted in 5 levels (5mA~42mA).

In PWM Control mode, the PWM duty cycle of each output can be independently programmed and controlled in 256 steps to simplify color mixing. In One Shot Programming mode, the timing characteristics for output current - current rising, holding, falling and off time, can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single color breathing without requiring any additional interface activity, thus saving valuable system resources.

IS31FL3193D is available in WLCSP-8 (1.6mm×1.0mm×0.46mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- One group RGB, single color LED breathing system-free pre-established pattern
- 3 independently controlled automatic and semiautomatic breathing system-free pre-established pattern
- I2C interface, automatic address increment function
- 3 independently controlled outputs of 256 PWM steps
- 2.7V to 5.5V supply voltage
- 5 levels programmable output current
- Over-temperature protection
- Operating temperature T_A = −40°C ~ +85°C
- WLCSP-8 (1.6mm×1.0mm×0.46mm) package

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

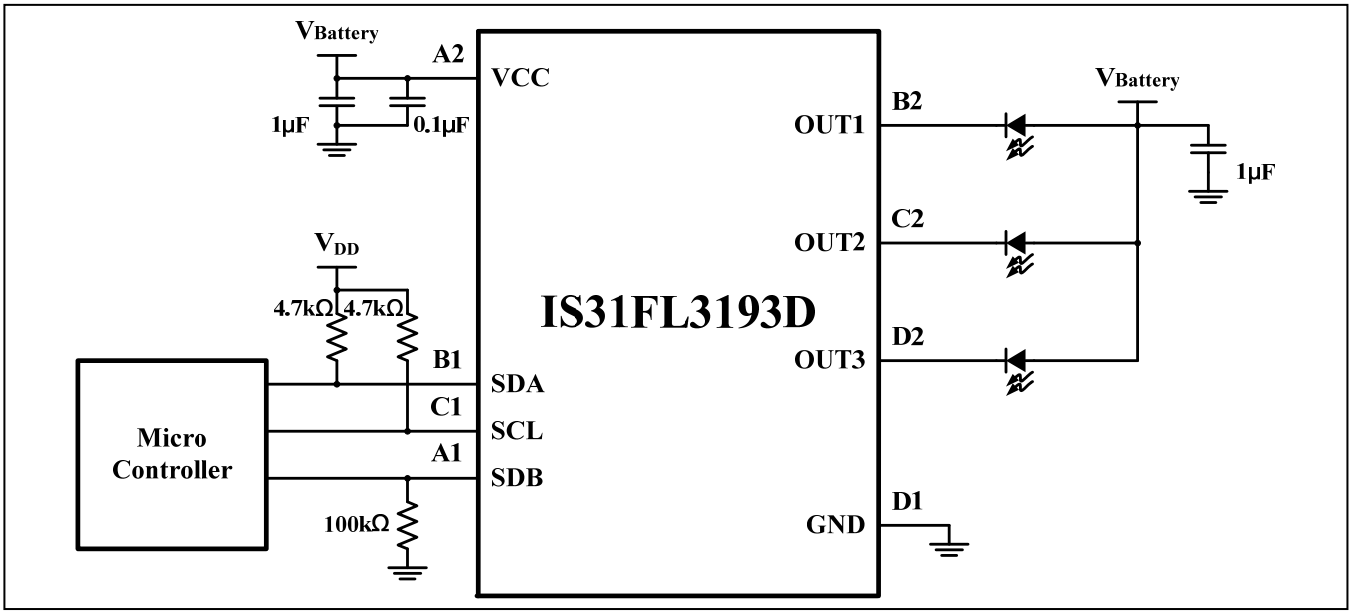
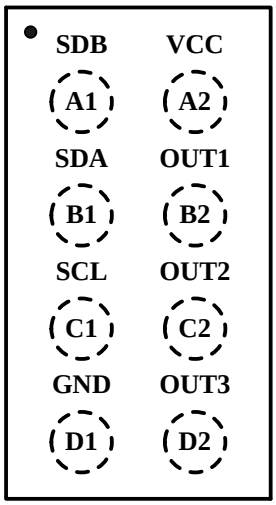


Figure 1 Typical Application Circuit

Note: The IC should be placed far away from the mobile antenna in order to prevent the EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WLCSP-8	

PIN DESCRIPTION

No.	Pin	Description
A1	SDB	Shutdown the chip when pulled to low.
A2	VCC	Power supply.
B1	SDA	I2C serial data.
B2	OUT1	Current source output 1.
C1	SCL	I2C serial clock.
C2	OUT2	Current source output 2.
D1	GND	Ground.
D2	OUT3	Current source output 3.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3193D-CLS2-TR	WLCSP-8, Lead-free	3000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	−0.3V ~ +6.0V
Voltage at any input pin	−0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	150°C
Operating temperature range, T_A	−40°C ~ +85°C
Storage temperature range, T_{STG}	−65°C ~ +150°C
ESD (HBM) ESD (CDM)	7kV 1kV

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.7V~5.5V, unless otherwise noted. Typical value are T_A = 25°C, V_{CC} = 5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB} = V_{CC}		0.8		mA
I_{SD}	Shutdown current	V_{SDB} = 0V			2.5	μA
		V_{SDB} = V_{CC}, software shutdown			3.5	
I_{OUT}	Output current	PWM Control mode, V_{DS} = 0.5V PWM Register(04h~06h) = 0xFF Current Register(03h) = 0x00		42 (Note 1)		mA
V_{HR}	Current sink headroom voltage	I_{OUT} = 42mA		500		mV
Logic Electrical Characteristics (SDA, SCL, SDB)						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V		5 (Note 2)		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC}		5 (Note 2)		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 3)		$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 3)		$20+0.1C_b$	300	ns

Note 1: I_{OUT} represents the average output current of each individual output. See PWM Register, Table 7.

Note 2: Guaranteed by design.

Note 3: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3193D uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3193D has a constant 7-bit slave address "1101 011" (A7:A1), followed by the R/W bit, A0. Since IS31FL3193D only supports write operations, A0 must always be "0".

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3193D.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3193D's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3193D has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3193D, the register address byte is sent, most significant bit first. IS31FL3193D must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3193D must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3193D, load the address of the data register that the first data byte is intended for. During the IS31FL3193D acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3193D will be placed in the new address, and so on (Figure 5).

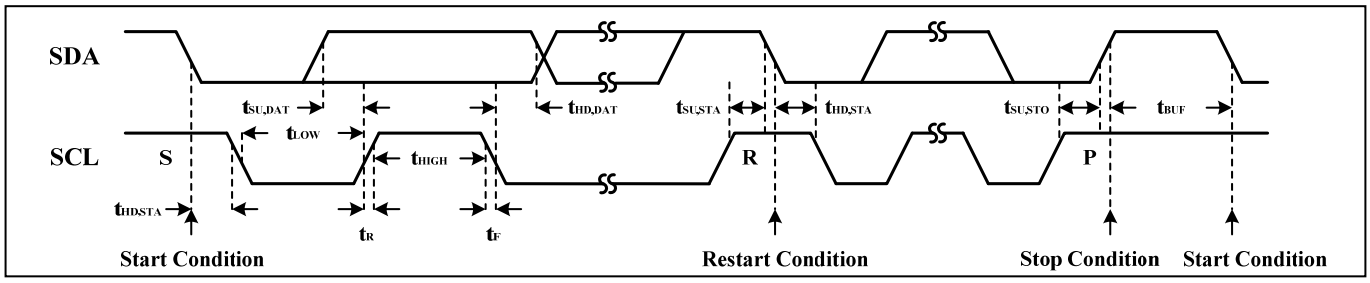


Figure 2 Interface Timing

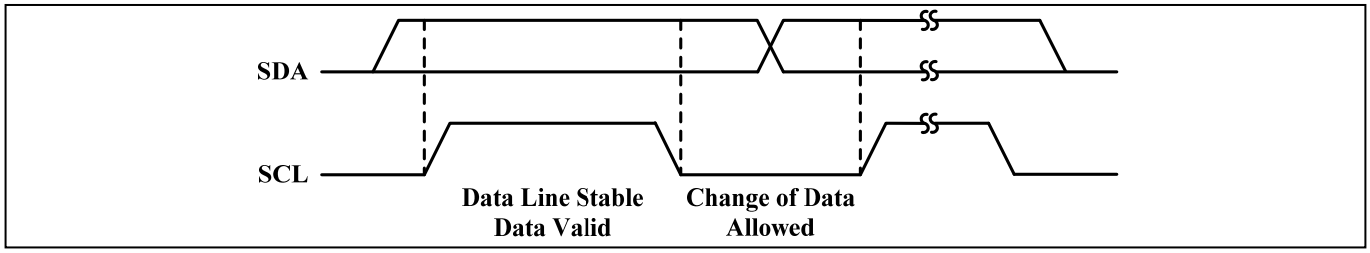


Figure 3 Bit Transfer

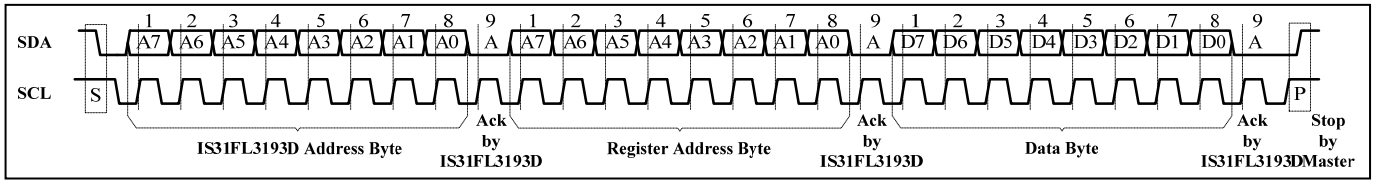


Figure 4 Writing to IS31FL3193D (Typical)

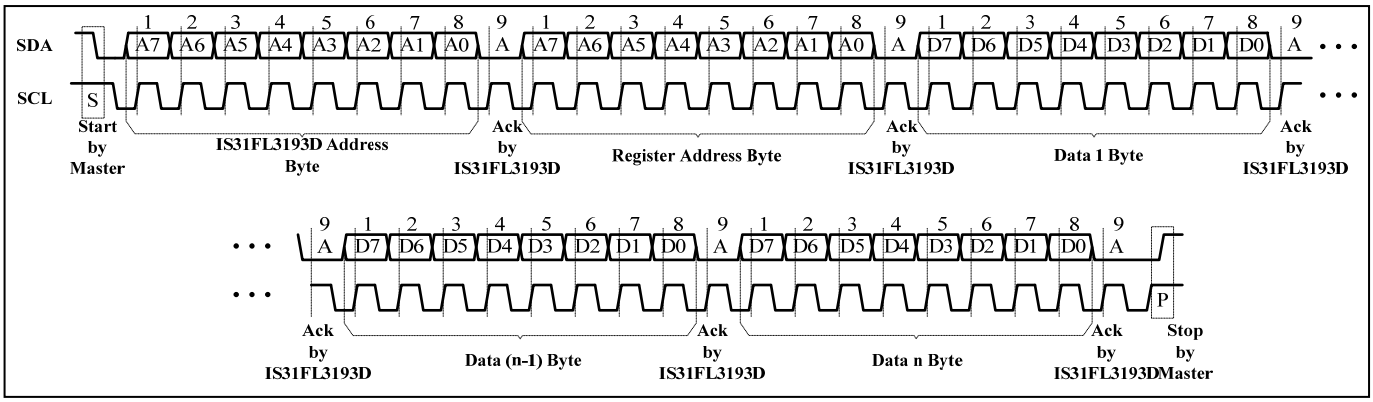


Figure 5 Writing to IS31FL3193D (Automatic Address Increment)

REGISTERS DEFINITIONS

Table 2 Register Function

Address	Name	Function	Table	Default
00h	Shutdown Register	Set software shutdown mode	3	0000 0001
01h	Breathing Control Register	Set the breathing function	4	0000 0000
02h	LED Mode Register	Set operation mode	5	
03h	Current Setting Register	Set output current	6	
04h~06h	PWM Register	3 channels PWM duty cycle data registers	7	
07h	Data Update Register	Load PWM Registers and LED Control Register' data	-	xxxx xxxx
0Ah ~ 0Ch	T0 Register	Set the T0 time	8	0000 0000
10h ~ 12h	T1&T2 Register	Set the T1&T2 time	9	
16h ~18h	T3&T4 Register	Set the T3&T4 time	10	
1Ch	Time Update Register	Load time registers' data	-	xxxx xxxx
1Dh	LED Control Register	OUT1~ OUT3 enable bit	11	0000 0111
2Fh	Reset Register	Reset all registers to default value	-	xxxx xxxx

Table 3 00h Shutdown Register

Bit	D7:D6	D5	D4:D1	D0
Name	-	EN	-	SSD
Default	00	0	0000	1

The Shutdown Register sets software shutdown mode of IS31FL3193D.

EN Channel Control
0 All channel disable
1 All channel enable

SSD Software Shutdown Enable
0 Normal operation
1 Software shutdown mode

Table 4 01h Breathing Control Register

Bit	D7:D6	D5	D4	D3:D0
Name	-	RM	HT	-
Default	00	0	0	0000

The Breathing Control Register sets the breathing function.

RM Ramping Mode Enable
0 Disable
1 Enable

HT Hold Time Selection
0 Hold on T2
1 Hold on T4

Table 5 02h LED Mode Register

Bit	D7:D6	D5	D4:D0
Name	-	RGB	-
Default	00	0	00000

The LED Mode Register sets operation mode of IS31FL3193D.

RGB	RGB Mode Selection
0	PWM Control Mode
1	One Shot Programming Mode

Table 6 03h Current Setting Register

Bit	D7:D5	D4:D2	D1:D0
Name	-	CS	-
Default	000	000	00

The Current Setting Register stores the maximum current setting, I_{MAX}, for all of the LED output channels.

CS	Current Setting
000	42mA
001	10mA
010	5mA
011	30mA
1xx	17.5mA

Table 7 04h~06h PWM Register(OUT1~OUT3)

Bit	D7:D0
Name	PWM
Default	0000 0000

The value in the PWM Registers modulate the RGB LEDs in 256 steps.

The value of the PWM Registers decide the average output current of OUT1~OUT3. The average output current may be computed using the Formula (1):

$$I_{OUT} = \frac{I_{MAX}}{256} \cdot \sum_{n=0}^{7} D[n] * 2^n \qquad (1)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

$I_{OUT} = I_{MAX} (2^0+2^2+2^4+2^5+2^7)/256$

I_{MAX} is set by Current Setting Register.

07h PWM Update Register

The data sent to the PWM Registers and the LED Control Registers will be stored in temporary registers. A write operation of “0000 0000” to the Update Register is required to update the registers (04h~06h, 1Dh).

Table 8 0Ah~0Ch T0 Register (OUT1~OUT3)

Bit	D7:D4	D3:D0
Name	T0	-
Default	0000	0000

The T0 Registers set the T0 time in One Shot Programming mode.

T0	T0 Setting
0000	0s
0001	0.13s
0010	0.26s
0011	0.52s
0100	1.04s
0101	2.08s
0110	4.16s
0111	8.32s
1000	16.64s
1001	33.28s
1010	66.56s
Others	Unavailable

Table 9 10h~12h T1&T2 Register (OUT1~OUT3)

Bit	D7:D5	D4:D1	D0
Name	T1	T2	-
Default	000	0000	0

The T1&T2 Registers set the T1&T2 time in One Shot Programming mode.

T1	T1 Setting
000	0.13s
001	0.26s
010	0.52s
011	1.04s
100	2.08s
101	4.16s
110	8.32s
111	16.64s

T2	T2 Setting
0000	0s
0001	0.13s
0010	0.26s
0011	0.52s
0100	1.04s
0101	2.08s
0110	4.16s
0111	8.32s
1000	16.64s
Others	Unavailable

Table 10 16h~18h T3&T4 Register (OUT1~OUT3)

Bit	D7:D5	D4:D1	D0
Name	T3	T4	-
Default	000	0000	0

The T3&T4 Registers set the T3&T4 time in One Shot Programming mode.

T3	T3 Setting
000	0.13s
001	0.26s
010	0.52s
011	1.04s
100	2.08s
101	4.16s
110	8.32s
111	16.64s

T4	T4 Setting
0000	0s
0001	0.13s
0010	0.26s
0011	0.52s
0100	1.04s
0101	2.08s
0110	4.16s
0111	8.32s
1000	16.64s
1001	33.28s
1010	66.56s
Others	Unavailable

1Ch Time Update Register

The data sent to the PWM Registers and the LED Control Register will be stored in temporary registers. A write operation of “0000 0000” to the Update Register is required to update the registers (0Ah~0Ch, 10h~12h, 16h~18h).

Table 11 1Dh LED Control Register (OUT1~OUT3)

Bit	D7:D3	D2:D0
Name	-	OUT3:OUT1
Default	00000	111

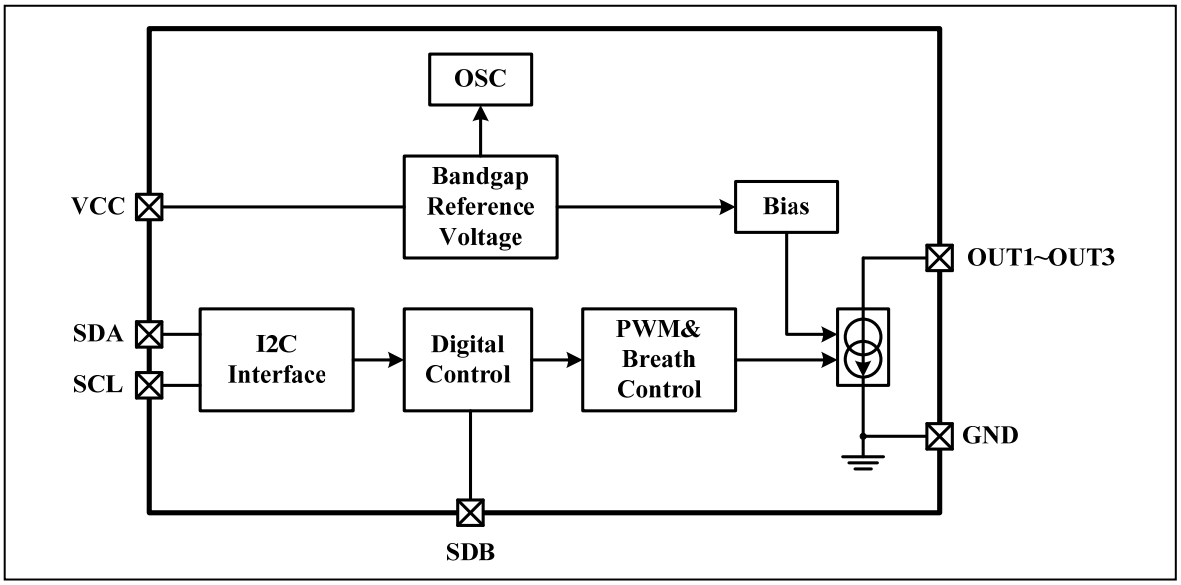
The LED Control Registers store the on or off state of each channel LED.

OUTx	LED State
0	LED off
1	LED on

2Fh Reset Register

Once user writes “0000 0000” to the Reset Register, IS31FL3193D will reset all registers to their default value. On initial power-up, the IS31FL3193D registers are reset to their default values for a blank display.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION

GENERAL DESCRIPTION

IS31FL3193D is a 3-channel LED driver with two-dimensional auto breathing and PWM Control mode. It can drive three individual LEDs or one group of RGB.

PWM CONTROL

By setting the RGB bit of the LED Mode Register (02h) to “0”, the IS31FL3193D will operate in PWM Control mode. The PWM Registers (04h~06h) can modulate LED brightness of 3 channels with 256 steps. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step, with a duty cycle of 4/256.

In PWM control mode, a new value must be written to the PWM registers to change the output PWM duty cycle. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect, blinking, or any other effects that the user defines.

RGB BREATHING CONTROL WITH AUTO COLOR CHANGING

By setting the RGB bit of the LED Mode Register (02h) to “1”, the IS31FL3193D will operate in One Shot Programming mode. In this mode, the RGB intensity is automatically modulated in a breathing cycle, independently controlled by T0~T4. T0 is an offset time period which runs only once at the start of the cycle. The full cycle is T1 to T4 (Figure 6). Setting different T0~T4 can achieve RGB breathing with auto color changing. The maximum intensity of each RGB is adjusted independently by the PWM Registers (04h~06h).

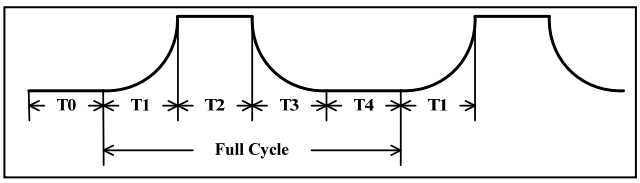


Figure 6 Breathing Timing

RGB AUTO BREATHING CONTROL WITH COLOR SETTING

IS31FL3193D can pre-establish pattern achieving mixing color breathing. There is one group RGB. The RGB consists of three channels. Every channel has an 8-bit PWM data register. The color can be set by the PWM data register. By adjusting the individual intensity of the red, green and blue LED, different colors are perceived. For example, the three PWM data: 20h, 80h, C8h, will determine one particular color.

After setting the color, T0~T4 time register will be set to control the LED breathing panel. And T0~T4 time should be same for each of the RGB LEDs, otherwise the pre-established color will change.

SEMIAUTOMATIC BREATHING

By setting the RGB bit of the LED Mode Register (02h) to “1” and the RM bit of the Breathing Control Register (01h) to “1”, the ramping function is enabled. HT is the time select bit. When HT bit is set to “0”, T2 will be held forever, and the LED will remain at the programmed maximum intensity. When HT bit is set to “1”, T3 will continue and T4 will be held, causing the LED to complete one breathing cycle and then remain off.

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

SOFTWARE SHUTDOWN

By setting SSD bit of the Shutdown Register (00h) to “1”, the IS31FL3193D will operate in software shutdown mode, wherein they consume only 2μA (typ.) current. When the IS31FL3193D is in software shutdown mode, all current sources are switched off.

HARDWARE SHUTDOWN

The chip enters hardware shutdown mode when the SDB pin is pulled low.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

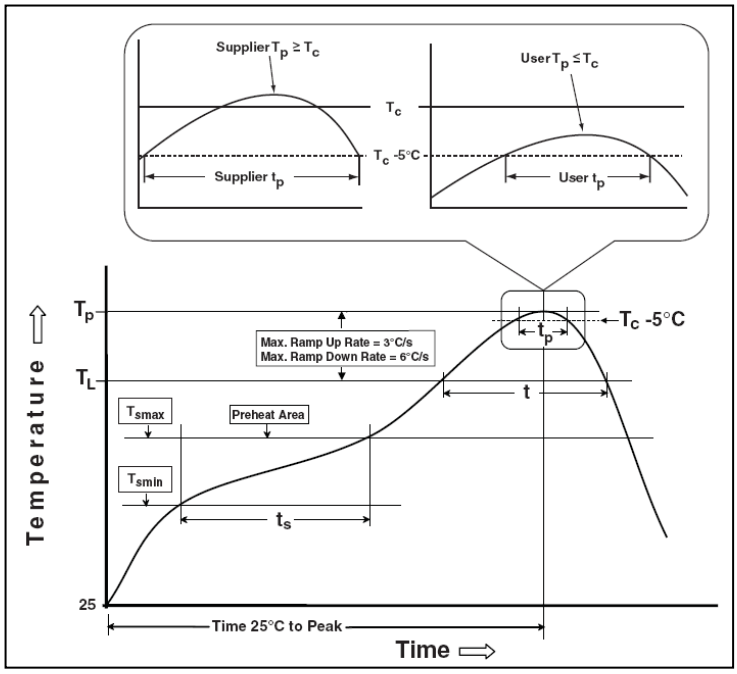
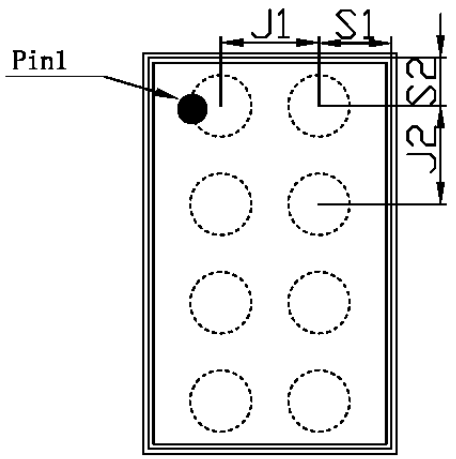


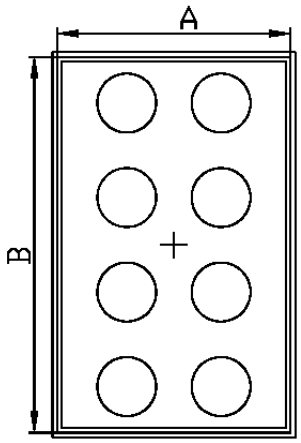
Figure 7 Classification Profile

PACKAGE INFORMATION

WLCSP-8

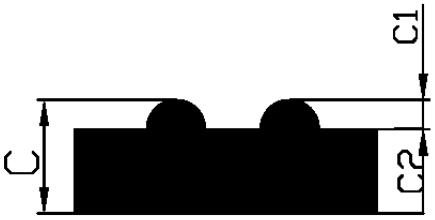


Top View



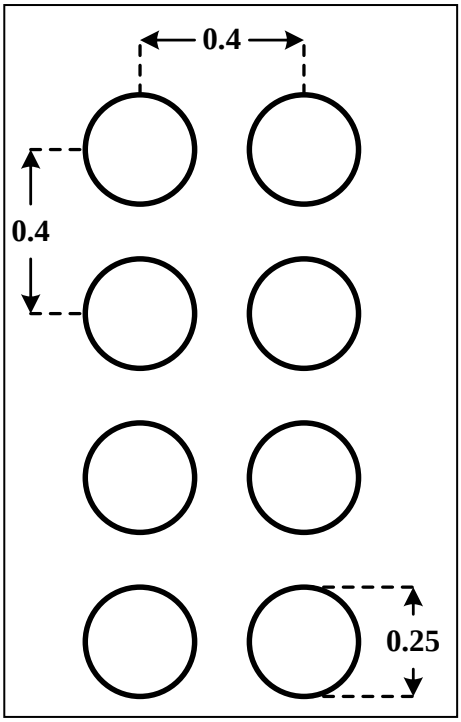
Bottom View (BGA side)

Parameter	Symbol	Nominal	Min	Max
		Millimeters		
Package Body Dimension X	A	0.9900	0.9650	1.0150
Package Body Dimension Y	B	1.5900	1.5650	1.6150
Package Height	C	0.4600	0.4150	0.5050
Silicon +Back cover Thickness	C2	0.4000	0.3850	0.4150
Ball Height	C1	0.0600	0.0500	0.0700
Ball Diameter	D1	0.2500	0.2200	0.2800
Total Ball Count	N	8		
Ball Count X axis	N1	2		
Ball Count Yaxis	N2	4		
Pins Pitch X axis	J1	0.4000		
Pins Pitch Y axis	J2	0.4000		
BGA ball center to package center offset in X-direction	X	0.0000	-0.0250	0.0250
BGA ball center to package center offset in Y-direction	Y	0.0000	-0.0250	0.0250
BGA ball center to chip center offset in X-direction	X1	0.0000	-0.0140	0.0140
BGA ball center to chip center offset in Y-direction	Y1	0.0000	-0.0140	0.0140
Edge to Ball Center Distance along X	S1	0.2950	0.2650	0.3250
Edge to Ball Center Distance along Y	S2	0.1950	0.1650	0.2250



Cross Section

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2015.05.20