

CD4007A Types

CMOS Dual Complementary Pair Plus Inverter

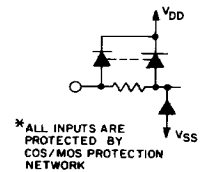
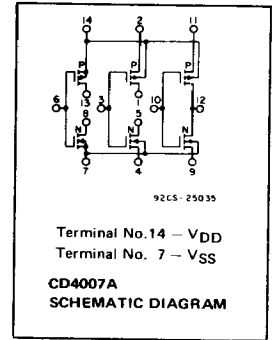
The RCA-CD4007A types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation.
 $t_{PHL} = t_{PLH} = 20 \text{ ns (typ.) at } C_L = 15 \text{ pF, } +V_{DD} = 10 \text{ V}$
- Low "high" and "low" output impedance. $500 \Omega \text{ (typ.) at } V_{DD} - V_{SS} = 10 \text{ V}$
- Quiescent current specified to 15 V
- Maximum input leakage current of $1 \mu\text{A}$ at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)



MAXIMUM RATINGS, Absolute Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE TEMPERATURE RANGE (ALL PACKAGE TYPES)}$	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	0.5 to $V_{DD} + 0.5 \text{ V}$
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	D, F, K, H Packages		E Package		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T _A = Full Package Temperature Range)	3	12	3	12	V

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$, $C_L = 15 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS							UNITS
		VDD (V)	D, F, K, H Packages			E Package			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; tPLH, tPHL		5		35	60		35	75	ns
		10		20	40		20	50	
Transition Time; tTHL, tTLH		5		50	75		50	100	ns
		10		30	40		30	50	
Average Input Capacitance, CI	Any Input			5			5		pF

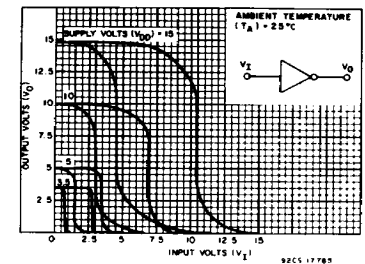


Fig. 1 - Minimum and maximum voltage-transfer characteristics for inverter.

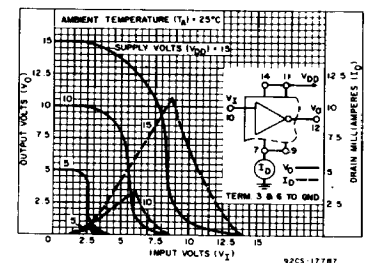


Fig. 2 - Typical current and voltage-transfer characteristics for inverter.

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STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85	
					Typ.	Limit			Typ.	Limit		
Quiescent Device Current: I _L Max.	—	—	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	—	—	10	0.1	0.001	0.1	6	1	0.005	1	30	
	—	—	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage Low Level V _{OL}	—	5	5	0 Typ.; 0.05 Max.								V
	—	10	10	0 Typ.; 0.05 Max.								
High Level V _{OH}	—	0	5	4.95 Min.; 5 Typ.								V
	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low V _{NL}	3.6	—	5	1.5 Min.; 2.25 Typ.								V
	7.2	—	10	3 Min.; 4.5 Typ.								
Inputs High V _{NH}	1.4	—	5	1.5 Min.; 2.25 Typ.								V
	2.8	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low V _{NML}	4.5	—	5	1 Min.								V
	9	—	10	1 Min.								
Inputs High V _{NMH}	0.5	—	5	1 Min.								V
	1	—	10	1 Min.								
Output Drive Current: N-Channel (Sink) I _{DN} Min.	0.4*	V _I =	5	0.75	1	0.6	0.4	0.35	1	0.3	0.24	mA
	0.5	V _{DD}	10	1.6	2.5	1.3	0.95	1.2	2.5	1	0.8	
P-Channel (Source): I _{DP} Min.	2.5†	V _I =	5	-1.75	-4	-1.4	-1	-1.3	-4	-1.1	-0.9	mA
	9.5	V _{DD}	10	-1.35	-2.5	-1.1	-0.75	-0.65	-2.5	-0.55	-0.45	
Input Leakage Current: I _{IL} , I _{IH}	Any Input											μA
	—	—	15	±10 ⁻⁵ Typ., ±1 Max.								

*Maximum noise-free low-level bipolar output voltage. †Minimum noise-free high-level bipolar output voltage.

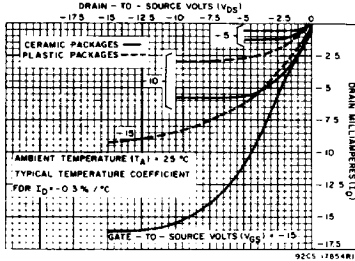


Fig. 5 - Minimum output p-channel drain characteristics.

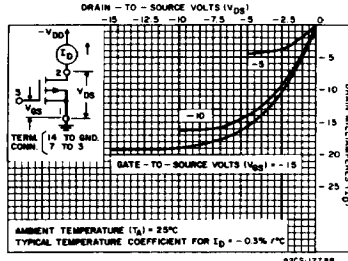


Fig. 6 - Typical output p-channel drain characteristics.

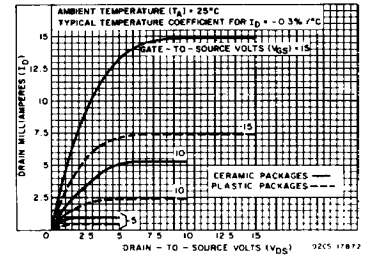


Fig. 7 - Minimum output n-channel drain characteristics.

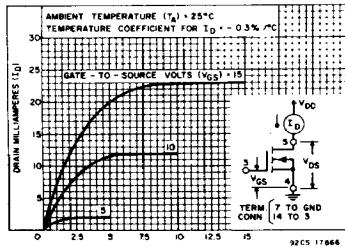


Fig. 8 - Typical output n-channel drain characteristics.

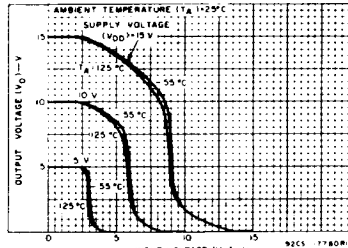


Fig. 9 - Typical voltage-transfer characteristics as a function of temperature.

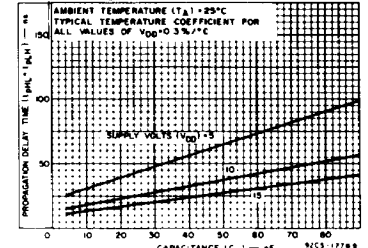


Fig. 10 - Typical propagation-delay time vs. load capacitance.

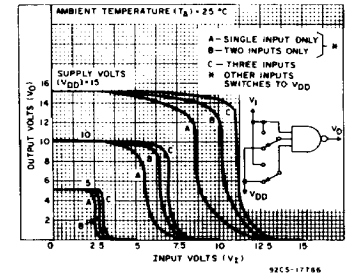


Fig. 3 - Typical voltage-transfer characteristics for NAND gate.

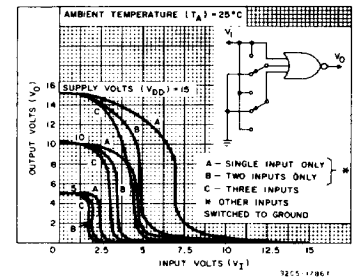


Fig. 4 - Typical voltage-transfer characteristics for NOR gate.

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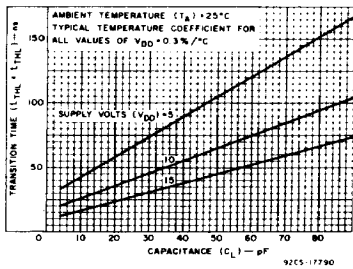


Fig. 11 - Typical transition time vs. load capacitance.

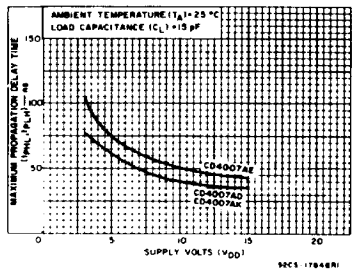


Fig. 12 - Maximum propagation delay time vs. supply voltage.

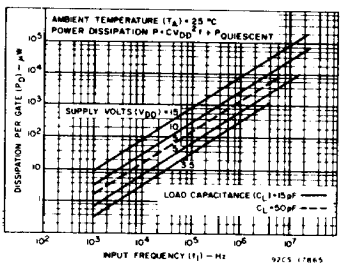
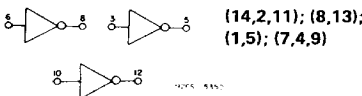
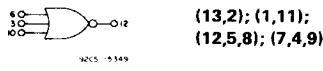


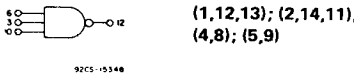
Fig. 13 - Typical dissipation characteristics.



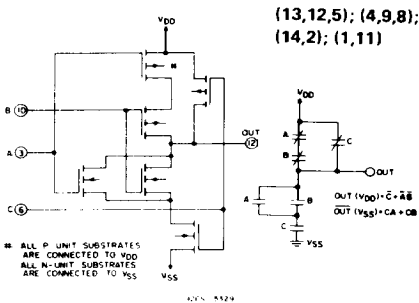
a) Triple Inverters



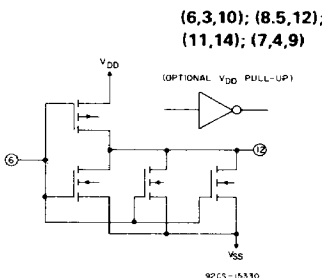
b) 3-Input NOR Gate



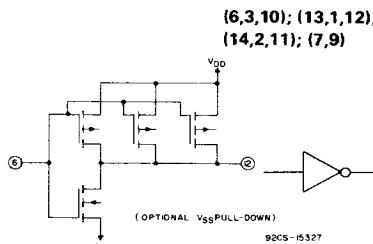
c) 3-Input NAND Gate



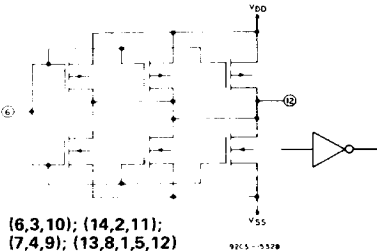
d) Tree (Relay) Logic



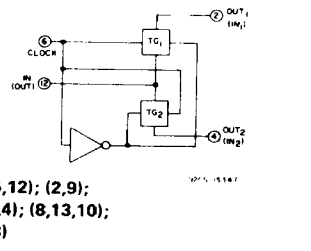
e) High Sink-Current Driver



f) High Source-Current Driver



g) High Sink- and Source-Current Driver



h) Dual Bi-Directional Transmission Gating

Fig. 14 - Sample COS/MOS logic circuit arrangements using type CD4007A.

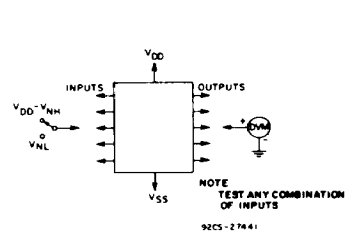


Fig. 15 - Noise-immunity test circuit.

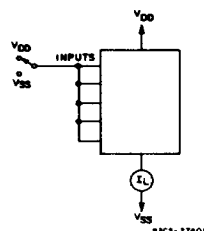


Fig. 16 - Quiescent-device-current test circuit.

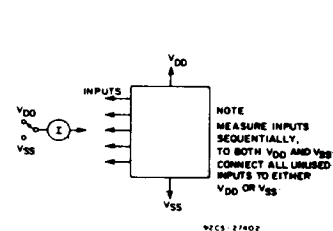


Fig. 17 - Input-leakage-current test circuit.